Fremont Micro Devices

FT32F103xC/D/E

Data Sheet

Key Feature

Arm® Cortex® -M3 based 32-bit MCU (72 MHz)

Flash: up to 512 Kbytes, SRAM: up to 64 Kbytes

Supports muxed NOR flash, muxed PSRAM, NAND flash

64/100 pins , up to 80 fast I/Os

Low power modes : Sleep, Stop, Standby

3 x 12-bit ADCs, 2 x 12-bit DACs

12-channel DMA controller

Up to 11 timers

2 x I2Cs, 3 x USARTs, 2 x UARTs, 3 x SPIs (2 x I2Ss)

CAN interface

USB 2.0 full-speed interface

SDIO interface

CRC calculation unit

LCD parallel interface

Rev 1.03
www.fremontmicro.com

Features

Core

- ✓ 32-bit Arm® Cortex®-M3 Core
- ✓ Up to 72MHz working frequency, 1.25 DMIPS / MHz (Dhrystone 2.1) performance at 0 wait state memory access
- ✓ Single-cycle multiplication and hardware division

Memories

- ✓ Up to 512 Kbytes of Flash memory
- ✓ Up to 64 Kbytes of SRAM
- ✓ Flexible static memory controller. Supports muxed NOR flash, muxed PSRAM, NAND flash
- ✓ LCD parallel interface, 8080 / 6800 modes

Reset and power management

- ✓ 1.8 to 5.0 V application supply and I/Os
- ✓ POR, PDR, and programmable voltage detector (PVD)
- ✓ Low power modes: Sleep, Stop, Standby
  V_{BAT} supply for RTC and backup registers

Clock management

- ✓ 4 to 16 MHz crystal oscillator
- ✓ Internal 8 MHz factory-trimmed RC
- ✓ Internal 40 kHz RC with calibration
- ✓ 32 kHz oscillator for RTC with calibration

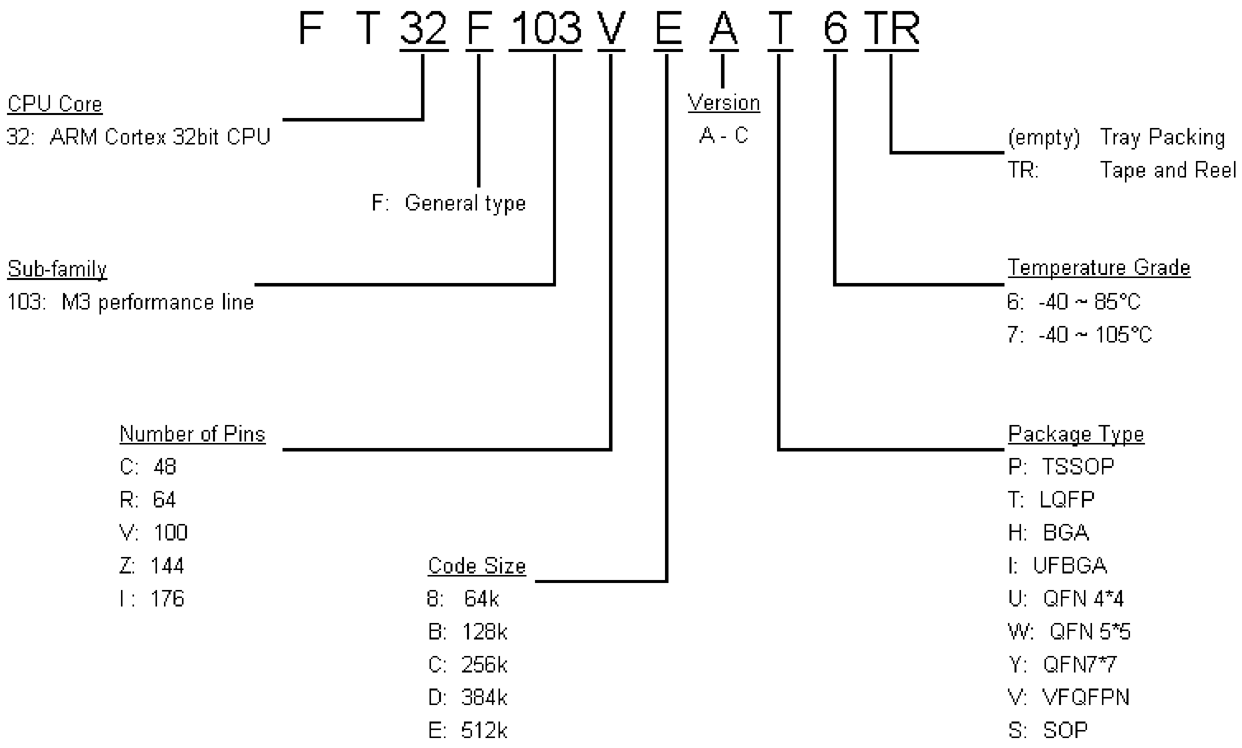
Peripheral features

- ■ 3 x 12-bit, 1μs ADC (up to 16 channels)
  - ✓ Conversion range: 0 to 5.0 V
  - ✓ Triple-sample and hold capability
  - ✓ Temperature sensor
- ■ 2 x 12-bit DAC
- ■ DMA：12-channel DMA controller
  - ✓ Supported peripherals: timers, ADCs, DAC, SDIO, I2Ss, SPIs, I2Cs and USARTs
- ■ Debug mode
  - ✓ Serial wire debug (SWD) & JTAG interfaces
  - ✓ Cortex® -M3 Embedded Trace Macrocell™
- ■ Up to 80 fast I/O ports
  - ✓ 51/80 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant
- ■ Up to 11 timers
  - ✓ Up to four 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - ✓ 2 x 16-bit motor control PWM timers with deadtime generation and emergency stop
  - ✓ 2 x watchdog timers (Independent and Window)
  - ✓ SysTick timer: a 24-bit downcounter
  - ✓ 2 x 16-bit basic timers to drive the DAC
- ■ Up to 13 communication Interfaces
  - ✓ Up to 2 x I2C interfaces
  - ✓ Up to 5 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - ✓ Up to 3 SPIs (18 Mbit/s), 2 with I2S interface multiplexed
  - ✓ CAN interface (2.0B Active)
  - ✓ USB 2.0 full speed interface
  - ✓ SDIO interface
- ■ CRC calculation unit, 96-bit unique ID
- ■ Packages : LQFP64, LQFP100

Part Information and Selection

Peripherals		FT32F103Rx			FT32F103Vx		
Flash memory in Kbytes		256	384	512	256	384	512
SRAM in Kbytes		48	64		48	64	
FSMC		No			Yes(1)		
Timers	General-purpose	4					
	Advanced-control	2					
	Basic	2					
Comm	SPI(I2S)(2)	3(2)					
	I2C	2					
	USART	5					
	USB	1					
	CAN	1					
	SDIO	1					
GPIOs		51			80		
12-bit ADC Number of channels		3 16					
12-bit DAC Number of channels		2					
CPU frequency		72 MHz					
Operating voltage		1.8 to 5.0 V					
Operating temperatures (see **Table 4-4**)		Ambient temperatures: -40 to +85 °C / -40 to +105 °C Junction temperatures: -40 to +105 °C / -40 to +125 °C					
Package		LQFP64			LQFP100		

1. For the LQFP100 package, only FSMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.



MCU Product Ordering Information

Revision History

Revision	Date	Description
1.00	2023-03-30	Initial release
1.01	2023-07-04	Updated R_{PU} of NRST pin; updated ADC accuracy characteristics; typo correction
1.02	2023-09-15	Updated the power consumption per ADC for the analog part
1.03	2024-03-21	Updated Table 4-1 and Table 4-3; Updated EMI standard; Typo correction

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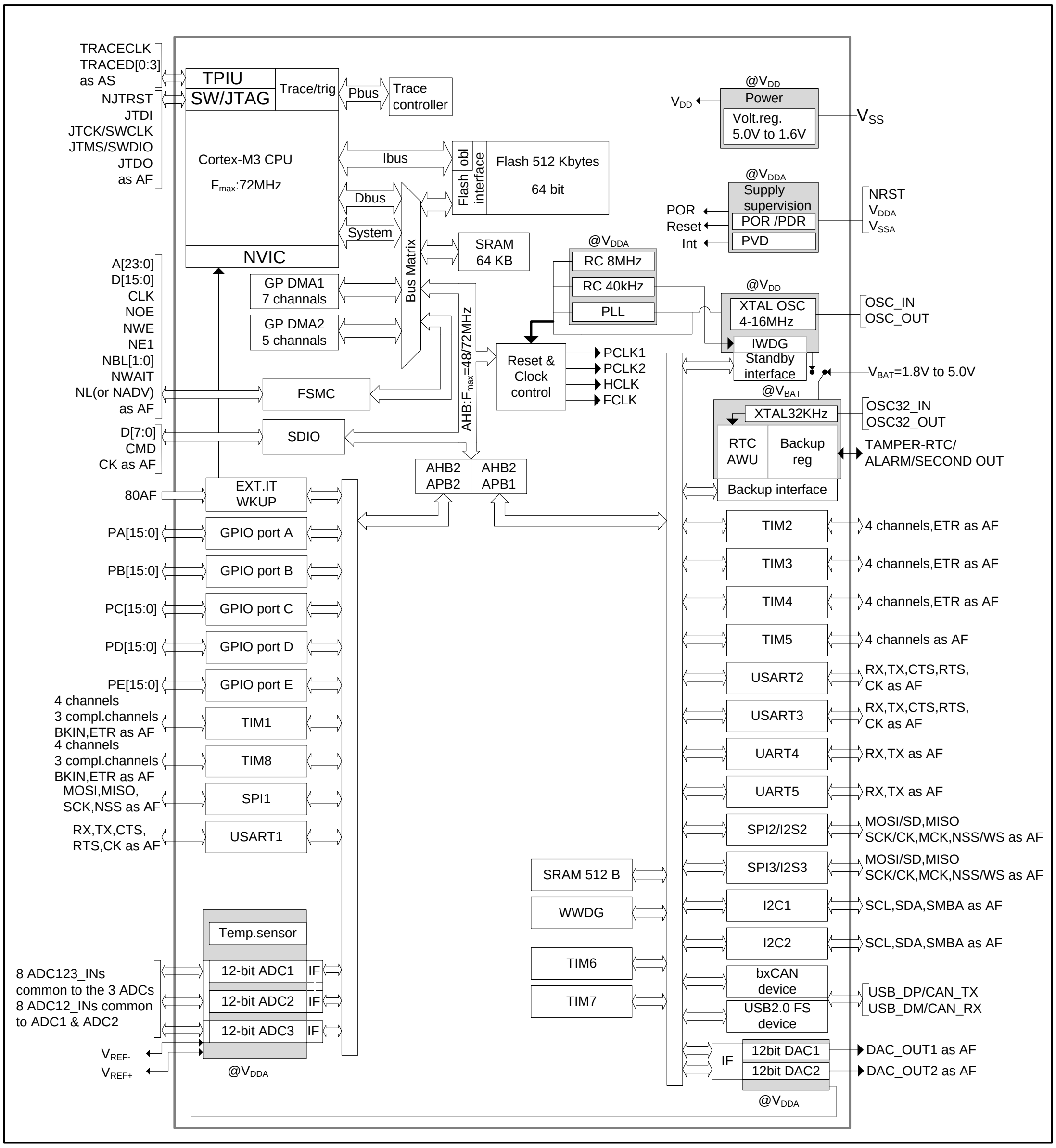
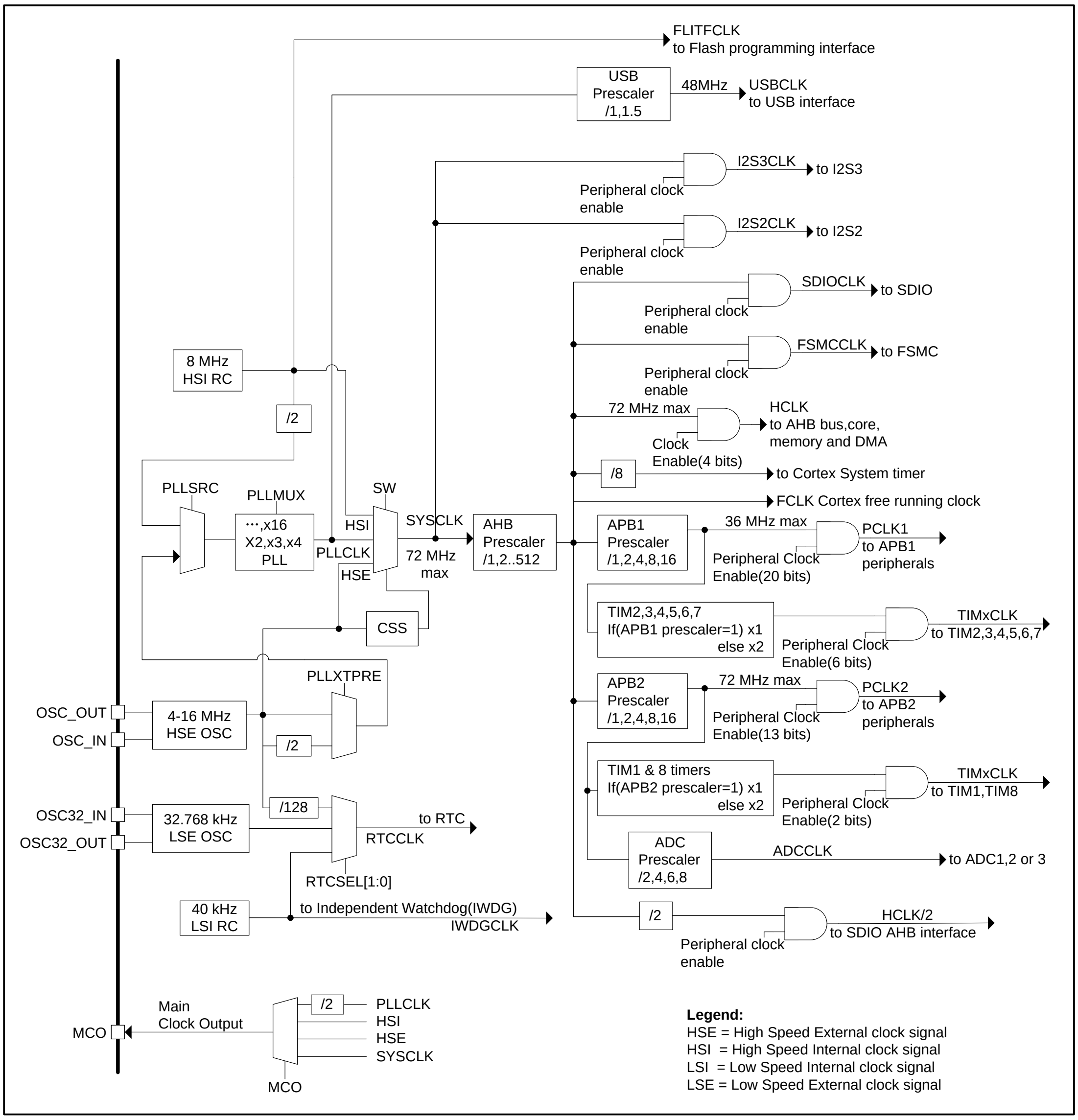
1. Block Diagram and Pinouts

Figure 1-1 FT32F103xC/D/E microcontroller block diagram



1. T_A = -40 °C to +85 °C (suffix 6) or -40 °C to +105 °C (suffix 7), junction temperature up to 105 °C or 125 °C, respectively.
2. AF = alternate function on I/O port pin.

Figure 1-2 Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the USBCLK at 48 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 28 MHz or 56 MHz.

1.1 Pinouts

Figure 1-3 FT32F103Rx LQFP64 pinout

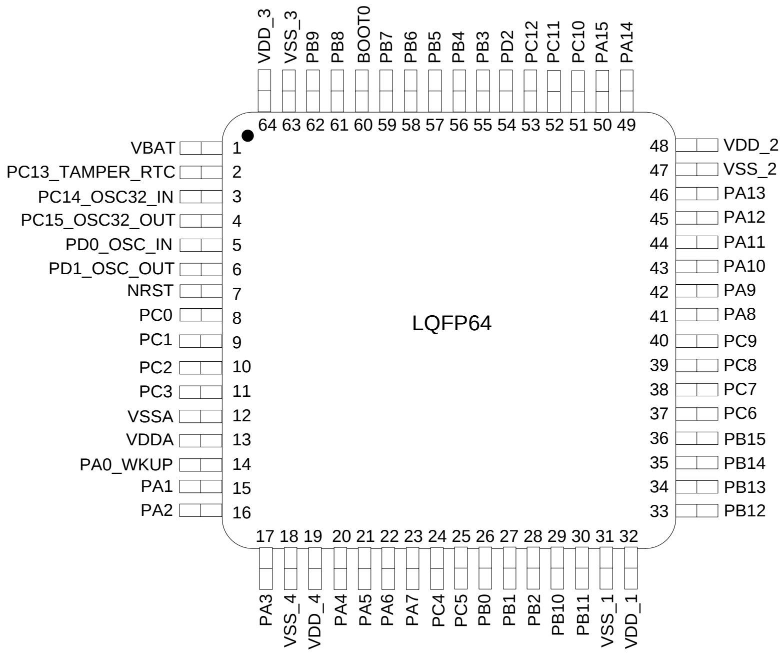
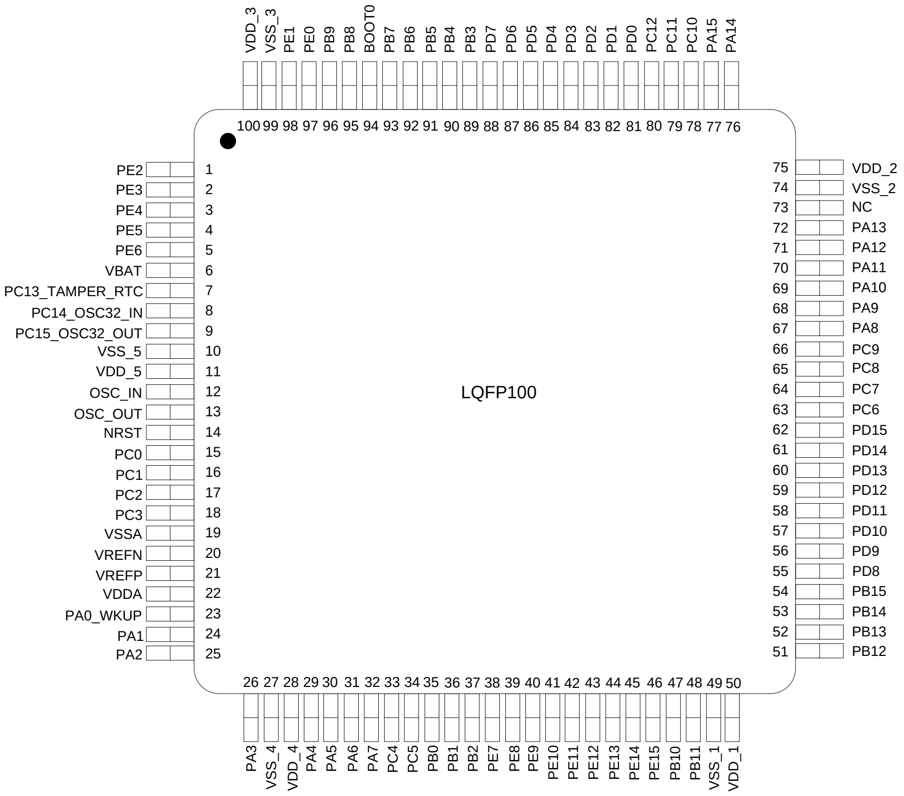


Figure 1-4 FT32F103Vx LQFP100 pinout



1.2 Pin descriptions

Table 1-1 FT32F103xC/D/E microcontroller pin definitions

Pins		Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP64	LQFP100					Default	Remap
-	1	PE2	I/O	FT	PE2	TRACECK FSMC_A23	-
-	2	PE3	I/O	FT	PE3	TRACED0 FSMC_A19	-
-	3	PE4	I/O	FT	PE4	TRACED1 FSMC_A20	-
-	4	PE5	I/O	FT	PE5	TRACED2 FSMC_A21	-
-	5	PE6	I/O	FT	PE6	TRACED3 FSMC_A22	-
1	6	V_{BAT}	S	-	V_{BAT}	-	-
2	7	PC13-TAMPER_RTC(5)	I/O	-	PC13(6)	TAMPER_RTC	-
3	8	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
4	9	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
-	10	V_{SS_5}	S	-	V_{SS_5}	-	-
-	11	V_{DD_5}	S	-	V_{DD_5}	-	-
5	12	OSC_IN	I	-	OSC_IN	-	-
6	13	OSC_OUT	O	-	OSC_OUT	-	-
7	14	NRST	I/O	-	NRST	-	-
8	15	PC0	I/O	-	PC0	ADC123_IN10	-
9	16	PC1	I/O	-	PC1	ADC123_IN11	-
10	17	PC2	I/O	-	PC2	ADC123_IN12	-
11	18	PC3	I/O	-	PC3	ADC123_IN13	-
12	19	V_{SSA}	S	-	V_{SSA}	-	-
-	20	V_{REF-}	S	-	V_{REF-}	-	-
-	21	V_{REF+}	S	-	V_{REF+}	-	-
13	22	V_{DDA}	S	-	V_{DDA}	-	-
14	23	PA0-WKUP	I/O	-	PA0	WKUP USART2_CTS(7) ADC123_IN0 TIM2_CH1_ETR(7) TIM5_CH1	-

Pins		Pin name	Type[1]	I/O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP64	LQFP100					Default	Remap
						TIM8_ETR	
15	24	PA1	I/O	-	PA1	USART2_RTS[7] ADC123_IN1 TIM5_CH2 TIM2_CH2[7]	-
16	25	PA2	I/O	-	PA2	USART2_TX[7] TIM5_CH3 ADC123_IN2 TIM2_CH3[7]	-
17	26	PA3	I/O	-	PA3	USART2_RX[7] TIM5_CH4 ADC123_IN3 TIM2_CH4[7]	-
18	27	V_{SS_4}	S	-	V_{SS_4}	-	-
19	28	V_{DD_4}	S	-	V_{DD_4}	-	-
20	29	PA4	I/O	-	PA4	SPI1_NSS[7] USART2_CK[7] DAC_OUT1 ADC12_IN4	-
21	30	PA5	I/O	-	PA5	SPI1_SCK[7] DAC_OUT2 ADC12_IN5	-
22	31	PA6	I/O	-	PA6	SPI1_MISO[7] TIM8_BKIN ADC12_IN6 TIM3_CH1[7]	TIM1_BKIN
23	32	PA7	I/O	-	PA7	SPI1_MOSI[7] TIM8_CH1N ADC12_IN7 TIM3_CH2[7]	TIM1_CH1N
24	33	PC4	I/O	-	PC4	ADC12_IN14	-
25	34	PC5	I/O	-	PC5	ADC12_IN15	-
26	35	PB0	I/O	-	PB0	ADC12_IN8 TIM3_CH3[7] TIM8_CH2N	TIM1_CH2N
27	36	PB1	I/O	-	PB1	ADC12_IN9 TIM3_CH4[7] TIM8_CH3N	TIM1_CH3N

Pins		Pin name	Type[1]	I/O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP64	LQFP100					Default	Remap
28	37	PB2	I/O	FT	PB2/BOOT1	-	-
-	38	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
-	39	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
-	40	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
-	41	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
-	42	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
-	43	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
-	44	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
-	45	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
-	46	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
29	47	PB10	I/O	FT	PB10	I2C2_SCL USART3_TX(7)	TIM2_CH3
30	48	PB11	I/O	FT	PB11	I2C2_SDA USART3_RX(7)	TIM2_CH4
31	49	V_{SS_1}	S	-	V_{SS_1}	-	-
32	50	V_{DD_1}	S	-	V_{DD_1}	-	-
33	51	PB12	I/O	FT	PB12	SPI2_NSS I2S2_WS I2C2_SMBA USART3_CK(7) TIM1_BKIN(7)	-
34	52	PB13	I/O	FT	PB13	SPI2_SCK I2S2_CK USART3_CTS(7) TIM1_CH1N(7)	-
35	53	PB14	I/O	FT	PB14	SPI2_MISO TIM1_CH2N(7) USART3_RTS(7)	-
36	54	PB15	I/O	FT	PB15	SPI2_MOSI I2S2_SD TIM1_CH3N(7)	-
-	55	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
-	56	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
-	57	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
-	58	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
-	59	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 USART3_RTS
-	60	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2

Pins		Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP64	LQFP100					Default	Remap
-	61	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
-	62	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
37	63	PC6	I/O	FT	PC6	I2S2_MCK TIM8_CH1 SDIO_D6	TIM3_CH1
38	64	PC7	I/O	FT	PC7	I2S3_MCK TIM8_CH2 SDIO_D7	TIM3_CH2
39	65	PC8	I/O	FT	PC8	TIM8_CH3 SDIO_D0	TIM3_CH3
40	66	PC9	I/O	FT	PC9	TIM8_CH4 SDIO_D1	TIM3_CH4
41	67	PA8	I/O	FT	PA8	USART1_CK TIM1_CH1(7) MCO	-
42	68	PA9	I/O	FT	PA9	USART1_TX(7) TIM1_CH2(7)	-
43	69	PA10	I/O	FT	PA10	USART1_RX(7) TIM1_CH3(7)	-
44	70	PA11	I/O	FT	PA11	USART1_CTS USBDM CAN_RX(7) TIM1_CH4(7)	-
45	71	PA12	I/O	FT	PA12	USART1_RTS USBDP CAN_TX(7) TIM1_ETR(7)	-
46	72	PA13	I/O	FT	JTMS-SWDIO	-	PA13
-	73	Not connected					-
47	74	V_{SS_2}	S	-	V_{SS_2}	-	-
48	75	V_{DD_2}	S	-	V_{DD_2}	-	-
49	76	PA14	I/O	FT	JTCK-SWCLK	-	PA14
50	77	PA15	I/O	FT	JTDI	SPI3_NSS I2S3_WS	TIM2_CH1_ETR PA15 SPI1_NSS
51	78	PC10	I/O	FT	PC10	UART4_TX SDIO_D2	USART3_TX
52	79	PC11	I/O	FT	PC11	UART4_RX	USART3_RX

Pins		Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP64	LQFP100					Default	Remap
						SDIO_D3	
53	80	PC12	I/O	FT	PC12	UART5_TX SDIO_CK	USART3_CK
5	81	PD0	I/O	FT	OSC_IN(8)	FSMC_D2(9)	CAN_RX
6	82	PD1	I/O	FT	OSC_OUT(8)	FSMC_D3(9)	CAN_TX
54	83	PD2	I/O	FT	PD2	TIM3_ETR UART5_RX SDIO_CMD	-
-	84	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
-	85	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
-	86	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
-	87	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
-	88	PD7	I/O	FT	PD7	FSMC_NE1 FSMC_NCE2	USART2_CK
55	89	PB3	I/O	FT	JTDO	SPI3_SCK I2S3_CK	PB3 TRACESWO TIM2_CH2 SPI1_SCK
56	90	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 TIM3_CH1 SPI1_MISO
57	91	PB5	I/O	FT	PB5	I2C1_SMBA SPI3_MOSI I2S3_SD	TIM3_CH2 SPI1_MOSI
58	92	PB6	I/O	FT	PB6	I2C1_SCL(7) TIM4_CH1(7)	USART1_TX
59	93	PB7	I/O	FT	PB7	I2C1_SDA(7) FSMC_NADV(9) TIM4_CH2(7)	USART1_RX
60	94	BOOT0	I	-	BOOT0	-	-
61	95	PB8	I/O	FT	PB8	TIM4_CH3(7) SDIO_D4	I2C1_SCL CAN_RX
62	96	PB9	I/O	FT	PB9	TIM4_CH4(7) SDIO_D5	I2C1_SDA CAN_TX
-	97	PE0	I/O	FT	PE0	TIM4_ETR FSMC_NBL0	-
-	98	PE1	I/O	FT	PE1	FSMC_NBL1	-
63	99	V_{SS_3}	S	-	V_{SS_3}	-	-

Pins		Pin name	Type[1]	I/O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP64	LQFP100					Default	Remap
64	100	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED)
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the FT32F1x3xx reference manual, available from the FMD website: www.fremontmicro.com.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the FT32F1x3xx reference manual, available from the FMD website: www.fremontmicro.com.
8. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the FT32F1x3xx reference manual.
9. For devices delivered in LQFP64 packages, the FSMC function is not available.

Table 1-2 FSMC pin definition

Pins	FSMC	
	NOR/PSRAM Mux	NAND 16 bit
PE2	A23	-
PE3	A19	-
PE4	A20	-
PE5	A21	-
PE6	A22	-
PE7	DA4	D4
PE8	DA5	D5
PE9	DA6	D6
PE10	DA7	D7
PE11	DA8	D8

Pins	FSMC	
	NOR/PSRAM Mux	NAND 16 bit
PE12	DA9	D9
PE13	DA10	D10
PE14	DA11	D11
PE15	DA12	D12
PD8	DA13	D13
PD9	DA14	D14
PD10	DA15	D15
PD11	A16	CLE
PD12	A17	ALE
PD13	A18	-
PD14	DA0	D0
PD15	DA1	D1
PD0	DA2	D2
PD1	DA3	D3
PD3	CLK	-
PD4	NOE	NOE
PD5	NWE	NWE
PD6	NWAIT	NWAIT
PD7	NE1	NCE2
PB7	NADV	-
PE0	NBL0	-
PE1	NBL1	-

2. Description

The FT32F103xC/D/E microcontroller incorporates the high-performance Arm® Cortex®-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 512 Kbytes and SRAM up to 64 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer three 12-bit ADCs, four general-purpose 16-bit timers plus two PWM timers, as well as standard and advanced communication interfaces: up to two I2Cs, three SPIs, two I2Ss, one SDIO, five USARTs, an USB and a CAN.

The FT32F103xC/D/E microcontroller operates in the -40 to +105 °C temperature range, from a 1.8 to 5.0V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the FT32F103xC/D/E microcontroller suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems video intercom, and HVAC.

2.1 Overview

2.1.1 Arm® Cortex®-M3 core with embedded Flash and SRAM

The Arm Cortex®-M3 processor is the one generation of Arm processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The Arm Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

With its embedded Arm core, FT32F103xC/D/E performance microcontroller is compatible with all Arm tools and software.

Figure 1-1 shows the general block diagram of the device family.

2.1.2 Embedded Flash memory

Up to 512 Kbytes of embedded Flash is available for storing programs and data.

2.1.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.1.4 Embedded SRAM

Up to 64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.1.5 FSMC (flexible static memory controller)

The FSMC is embedded in the FT32F103xC/D/E performance microcontroller. It supports the following modes: muxed-PSRAM, muxed-NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for NAND Flash
- The targeted frequency, f_{CLK}, is HCLK/2, so external access is at 36 MHz when HCLK is at 72 MHz and external access is at 24 MHz when HCLK is at 48 MHz

2.1.6 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost- effective graphic applications using LCD modules with embedded controllers or high- performance solutions using external controllers with dedicated acceleration.

2.1.7 Nested vectored interrupt controller (NVIC)

The FT32F103xC/D/E microcontroller embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.1.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.1.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See **Figure 1-2** for details on the clock tree.

2.1.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

2.1.11 Power supply schemes

- V_{DD} = 1.8 to 5.0V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.8 to 5.0V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 5.0V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to **Figure 4-3**.

2.1.12 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 1.8 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to **Table 4-6** for the values of $V_{POR/PDR}$ and V_{PVD}.

2.1.13 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.1.14 Low-power modes

The FT32F103xC/D/E microcontroller supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.6 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

- Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.6 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.1.15 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I2C, USART, general-purpose, basic and advanced-control timers TIMx, DAC, I2S, SDIO and ADC.

2.1.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.1.17 Timers and watchdogs

The FT32F103xC/D/E microcontroller devices include up to two advanced-control timers, up to four general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 2-1 compares the features of the advanced-control, general-purpose and basic timers.

Table 2-1 Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timers (TIM1 and TIM8)

The two advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the FT32F103xC/D/E microcontroller. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.

The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.1.18 I2C bus

Up to two I2C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.1.19 Universal synchronous/asynchronous receiver transmitters (USARTs)

The FT32F103xC/D/E microcontroller embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.1.20 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.1.21 Inter-integrated sound (I2S)

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 48 kHz are supported. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

2.1.22 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

2.1.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.1.24 Universal serial bus (USB)

The FT32F103xC/D/E microcontroller embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

2.1.25 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.1.26 ADC (analog to digital converter)

Three 12-bit analog-to-digital converters are embedded into FT32F103xC/D/E microcontroller and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timers (TIM1 and TIM8) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.1.27 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the FT32F103xC/D/E performance microcontroller. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.1.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2.0V < V_{DDA} < 5.0V$. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.1.29 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

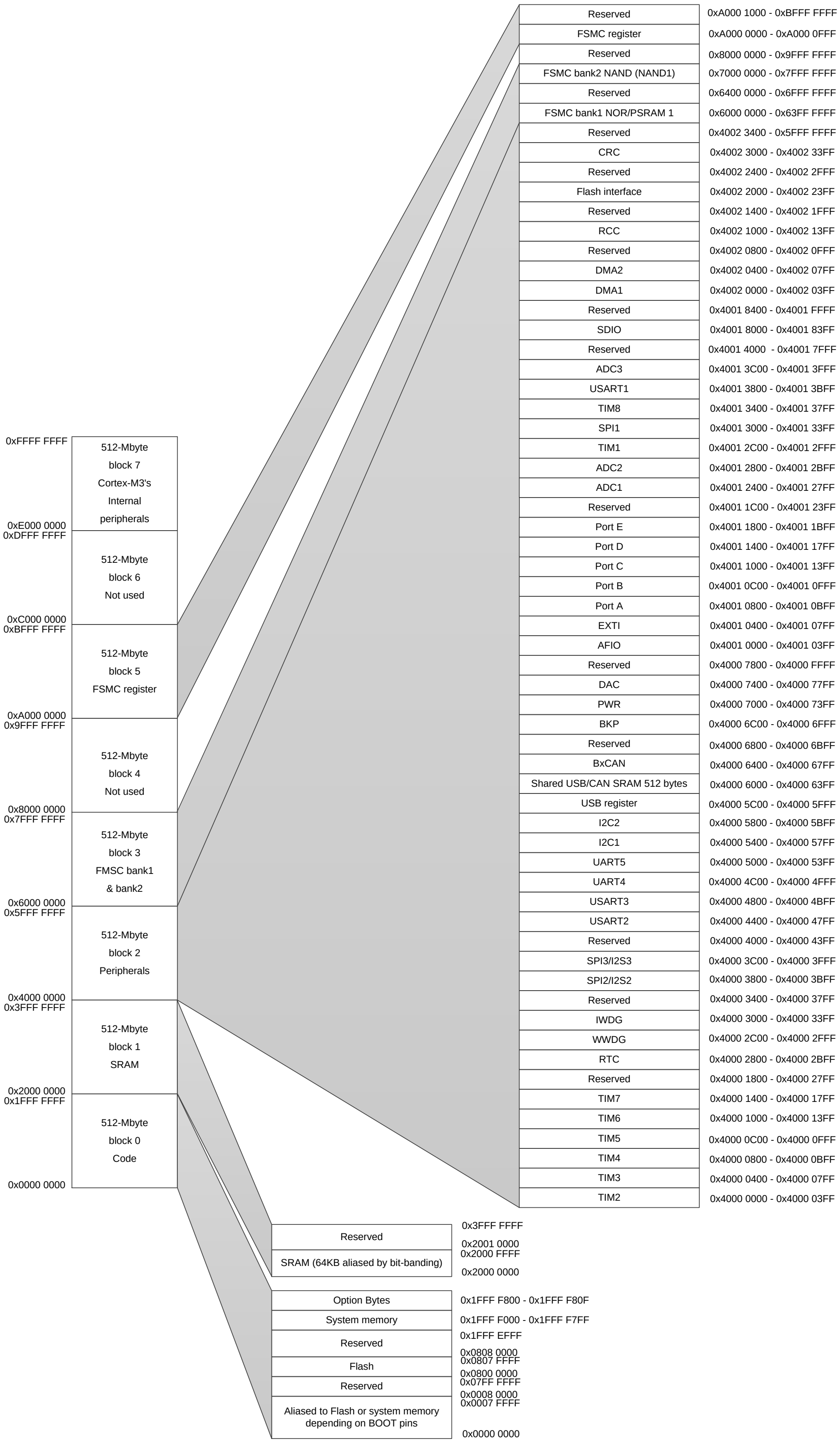
2.1.30 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the FT32F103xC/D/E through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

3. Memory mapping

The memory map is shown in **Figure 3-1.**

Figure 3-1 Memory map



Reserved	0xA000 1000 - 0xBFFF FFFF
FSMC register	0xA000 0000 - 0xA000 0FFF
Reserved	0x8000 0000 - 0x9FFF FFFF
FSMC bank2 NAND (NAND1)	0x7000 0000 - 0x7FFF FFFF
Reserved	0x6400 0000 - 0x6FFF FFFF
FSMC bank1 NOR/PSRAM 1	0x6000 0000 - 0x63FF FFFF
Reserved	0x4002 3400 - 0x5FFF FFFF
CRC	0x4002 3000 - 0x4002 33FF
Reserved	0x4002 2400 - 0x4002 2FFF
Flash interface	0x4002 2000 - 0x4002 23FF
Reserved	0x4002 1400 - 0x4002 1FFF
RCC	0x4002 1000 - 0x4002 13FF
Reserved	0x4002 0800 - 0x4002 0FFF
DMA2	0x4002 0400 - 0x4002 07FF
DMA1	0x4002 0000 - 0x4002 03FF
Reserved	0x4001 8400 - 0x4001 FFFF
SDIO	0x4001 8000 - 0x4001 83FF
Reserved	0x4001 4000 - 0x4001 7FFF
ADC3	0x4001 3C00 - 0x4001 3FFF
USART1	0x4001 3800 - 0x4001 3BFF
TIM8	0x4001 3400 - 0x4001 37FF
SPI1	0x4001 3000 - 0x4001 33FF
TIM1	0x4001 2C00 - 0x4001 2FFF
ADC2	0x4001 2800 - 0x4001 2BFF
ADC1	0x4001 2400 - 0x4001 27FF
Reserved	0x4001 1C00 - 0x4001 23FF
Port E	0x4001 1800 - 0x4001 1BFF
Port D	0x4001 1400 - 0x4001 17FF
Port C	0x4001 1000 - 0x4001 13FF
Port B	0x4001 0C00 - 0x4001 0FFF
Port A	0x4001 0800 - 0x4001 0BFF
EXTI	0x4001 0400 - 0x4001 07FF
AFIO	0x4001 0000 - 0x4001 03FF
Reserved	0x4000 7800 - 0x4000 FFFF
DAC	0x4000 7400 - 0x4000 77FF
PWR	0x4000 7000 - 0x4000 73FF
BKP	0x4000 6C00 - 0x4000 6FFF
Reserved	0x4000 6800 - 0x4000 6BFF
BxCAN	0x4000 6400 - 0x4000 67FF
Shared USB/CAN SRAM 512 bytes	0x4000 6000 - 0x4000 63FF
USB register	0x4000 5C00 - 0x4000 5FFF
I2C2	0x4000 5800 - 0x4000 5BFF
I2C1	0x4000 5400 - 0x4000 57FF
UART5	0x4000 5000 - 0x4000 53FF
UART4	0x4000 4C00 - 0x4000 4FFF
USART3	0x4000 4800 - 0x4000 4BFF
USART2	0x4000 4400 - 0x4000 47FF
Reserved	0x4000 4000 - 0x4000 43FF
SPI3/I2S3	0x4000 3C00 - 0x4000 3FFF
SPI2/I2S2	0x4000 3800 - 0x4000 3BFF
Reserved	0x4000 3400 - 0x4000 37FF
IWDG	0x4000 3000 - 0x4000 33FF
WWDG	0x4000 2C00 - 0x4000 2FFF
RTC	0x4000 2800 - 0x4000 2BFF
Reserved	0x4000 1800 - 0x4000 27FF
TIM7	0x4000 1400 - 0x4000 17FF
TIM6	0x4000 1000 - 0x4000 13FF
TIM5	0x4000 0C00 - 0x4000 0FFF
TIM4	0x4000 0800 - 0x4000 0BFF
TIM3	0x4000 0400 - 0x4000 07FF
TIM2	0x4000 0000 - 0x4000 03FF

Reserved	0x3FFF FFFF 0x2001 0000
SRAM (64KB aliased by bit-banding)	0x2000 FFFF 0x2000 0000

Option Bytes	0x1FFF F800 - 0x1FFF F80F
System memory	0x1FFF F000 - 0x1FFF F7FF
Reserved	0x1FFF EFFF 0x0808 0000
Flash	0x0807 FFFF 0x0800 0000
Reserved	0x07FF FFFF 0x0008 0000
Aliased to Flash or system memory depending on BOOT pins	0x0007 FFFF 0x0000 0000

4. Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.8 V ≤ V_{DD} ≤ 5.0 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

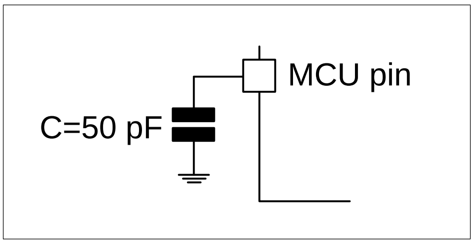
4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in **Figure 4-1**.

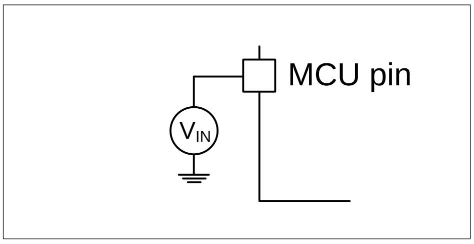
Figure 4-1 Pin loading conditions



4.1.5 Pin input voltage

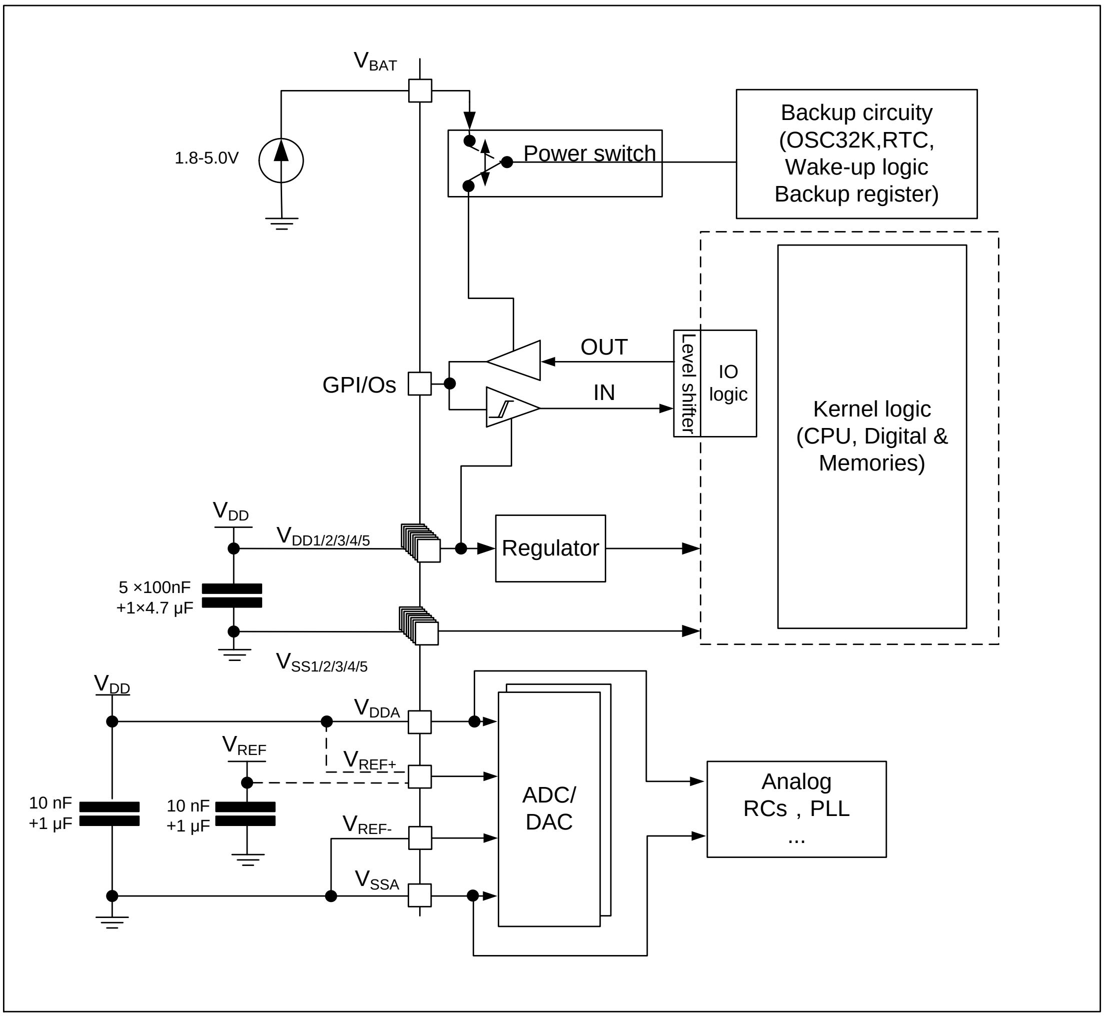
The input voltage measurement on a pin of the device is described in **Figure 4-2**.

Figure 4-2 Pin input voltage



4.1.6 Power supply scheme

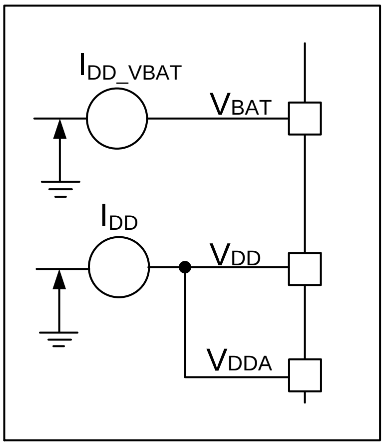
Figure 4-3 Power supply scheme



Caution: In **Figure 4-3**, the 4.7 µF capacitor must be connected to V_{DD3}.

4.1.7 Current consumption measurement

Figure 4-4 Current consumption measurement scheme



4.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in **Table 4-1** Voltage characteristics, **Table 4-2** Current characteristics and **Table 4-3** Thermal characteristics may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	-0.3	5.5	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS}-0.3	7.0	
	Input voltage on any other pin	V_{SS}-0.3	5.5	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX}-V_{SS}\|$	Variations between all the different ground pins(3)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see 4.3.12 Absolute maximum ratings (electrical sensitivity)		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to **Table 4-2** Current characteristics for the maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 4-2 Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	+5/+0	
	Injected current on any other pin(4)	±5	
$\sum I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note 3 below **Table 4-49**.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to **Table 4-1** Voltage characteristics for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to **Table 4-1** Voltage characteristics for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 4-3 Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	125	°C

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	1.8	5	V
$V_{DDA}^{(1)}$	Analog operating voltage (ADC not used)	Must be the same potential as $V_{DD}^{(2)}$	1.8	5	V
	Analog operating voltage (ADC used)		2.4	5	
V_{BAT}	Backup operating voltage	-	1.8	5	V
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low-power dissipation	-40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low-power dissipation	-40	125	
T_J	Junction temperature range	6 suffix version	-40	105	°C
		7 suffix version	-40	125	

1. When the ADC is used, refer to **Table 4-47** ADC characteristics.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

4.3.2 Operating conditions at power-up / power-down

The parameters given in **Table 4-5** are derived from tests performed under the ambient temperature condition summarized in **Table 4-4**.

Table 4-5 Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	

4.3.3 Embedded reset and power control block characteristics

The parameters given in **Table 4-6** are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**.

Table 4-6 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (PVDOPT = 0)	PLS[2:0]=000 (rising edge)	2.10	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2.00	2.08	2.16	
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.90	
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.80	
		PLS[2:0]=111 (rising edge)	2.76	2.88	3.00	
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.90	
V_{PVD}	Programmable voltage detector level selection (PVDOPT = 1)	PLS[2:0]=000 (rising edge)	1.65	1.72	1.79	V
		PLS[2:0]=000 (falling edge)	1.61	1.68	1.75	
		PLS[2:0]=001 (rising edge)	1.81	1.88	1.95	
		PLS[2:0]=001 (falling edge)	1.71	1.78	1.85	
		PLS[2:0]=010 (rising edge)	1.90	1.98	2.06	
		PLS[2:0]=010 (falling edge)	1.80	1.88	1.96	
		PLS[2:0]=011 (rising edge)	2.00	2.08	2.16	
		PLS[2:0]=011 (falling edge)	1.90	1.98	2.06	
		PLS[2:0]=100 (rising edge)	2.96	3.08	3.20	
		PLS[2:0]=100 (falling edge)	2.86	2.98	3.10	
		PLS[2:0]=101 (rising edge)	3.15	3.28	3.41	
		PLS[2:0]=101 (falling edge)	3.05	3.18	3.31	
		PLS[2:0]=110 (rising edge)	3.49	3.64	3.78	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		PLS[2:0]=110 (falling edge)	3.49	3.64	3.78	
		PLS[2:0]=111 (rising edge)	3.80	3.97	4.13	
		PLS[2:0]=111 (falling edge)	3.80	3.97	4.13	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.61(1)	1.68	1.75	V
		Rising edge	1.65	1.72	1.79	
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization	-	-	2.5	-	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.

4.3.4 Embedded reference voltage

The parameters given in **Table 4-7** are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**.

Table 4-7 Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 °C < T_A < +105 °C	1.16	1.20	1.26	V
		-40 °C < T_A < +85 °C	1.16	1.20	1.24	
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	100	ppm/°C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

4.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in **Figure 4-4** Current consumption measurement scheme.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in **Table 4-8**, **Table 4-9** and **Table 4-10** are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**.

Table 4-8 Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max[1]		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock[2], all peripherals enabled	72 MHz	20	20	mA
			48 MHz	13.5	13.5	
			36 MHz	9.5	9.5	
			24 MHz	7	7	
			16 MHz	5	5	
			8 MHz	3	3	
		External clock[2], all peripherals disabled	72 MHz	12	12	
			48 MHz	8.5	8.5	
			36 MHz	6	6	
			24 MHz	5	5	
			16 MHz	3.5	3.5	
			8 MHz	2	2	

1. Guaranteed by characterization results.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 4-9 Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max[1]		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock[2], all peripherals enabled	72 MHz	21	21	mA
			48 MHz	14.5	14.5	
			36 MHz	10	10	
			24 MHz	8	8	
			16 MHz	5.5	5.5	
			8 MHz	3	3	
		External clock[2], all peripherals disabled	72 MHz	13	13	
			48 MHz	9	9	
			36 MHz	6.5	6.5	
			24 MHz	5	5	
			16 MHz	4	4	
			8 MHz	2.5	2.5	

1. Guaranteed by characterization results at V_{DD} max, f_{HCLK} max.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 4-5 Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

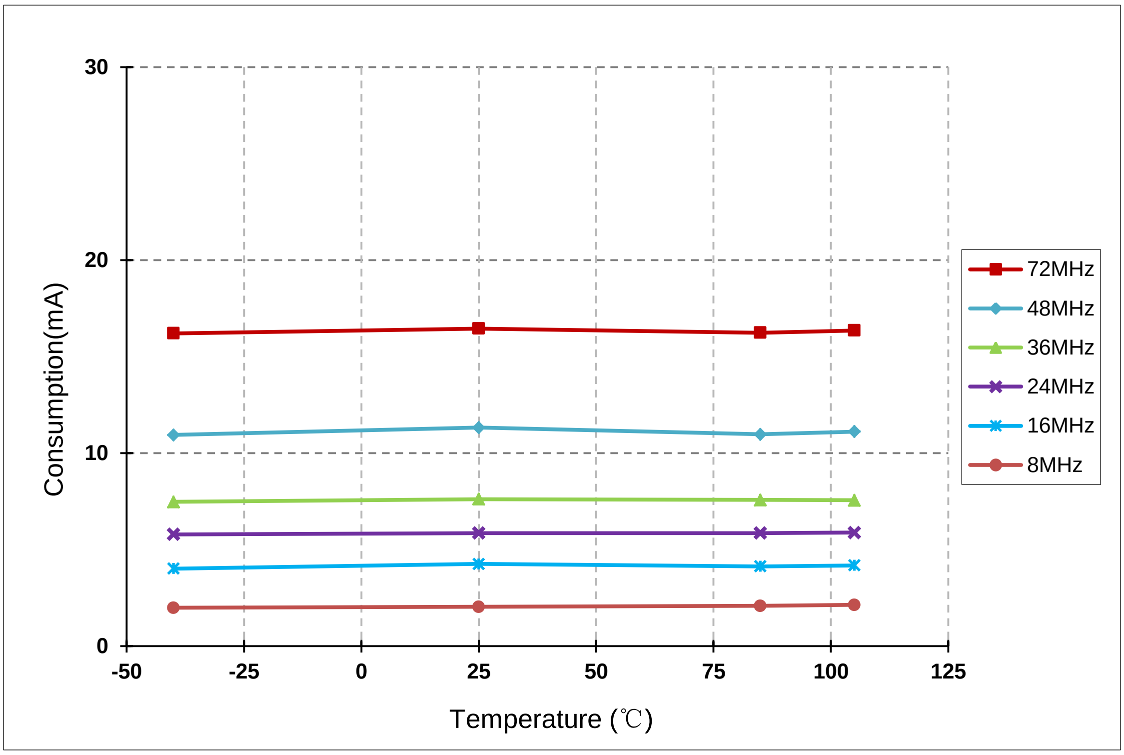


Figure 4-6 Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

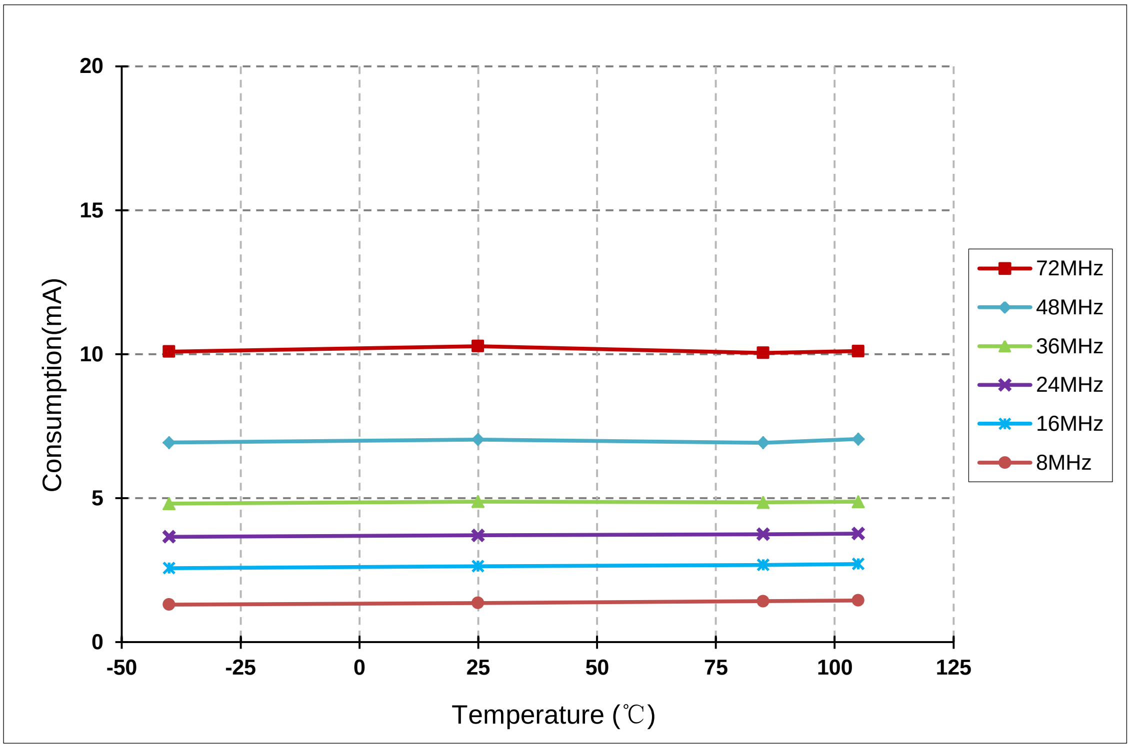


Table 4-10 Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max[1]		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock[2], all peripherals enabled	72 MHz	14	14	mA
			48 MHz	9.5	9.5	
			36 MHz	6.5	6.5	
			24 MHz	5	5	
			16 MHz	4	4	
			8 MHz	2.5	2.5	
		External clock[2], all peripherals disabled	72 MHz	5	5	
			48 MHz	3.5	3.5	
			36 MHz	3	3	
			24 MHz	2.5	2.5	
			16 MHz	2	2	
			8 MHz	1.5	1.5	

1. Guaranteed by characterization results at V_{DD} max, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 4-11 Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ[1]					Max		Unit
			V_{DD}/V_{BAT} = 1.8 V	V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	V_{DD}/V_{BAT} = 5.0 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	12.5	13.9	13.9	14.1	15.1	110	160	µA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high- speed oscillator OFF (no independent watchdog)	4.4	4.4	4.5	4.7	5.3	100	150	

Symbol	Parameter	Conditions	Typ[1]					Max		Unit
			V_{DD}/V_{BAT} = 1.8 V	V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	V_{DD}/V_{BAT} = 5.0 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	2.2	2.4	2.5	3.0	3.8	-	-	µA
		Low-speed internal RC oscillator ON, independent watchdog OFF	2.1	2.3	2.4	2.7	3.5	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.3	1.4	1.5	1.6	2.1	6.5[2]	14[2]	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	0.87	0.94	1.1	1.4	2.2	2.3[2]	2.5[2]	

1. Typical values are measured at T_A = 25 °C.
2. Guaranteed by characterization results.

Figure 4-7 Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

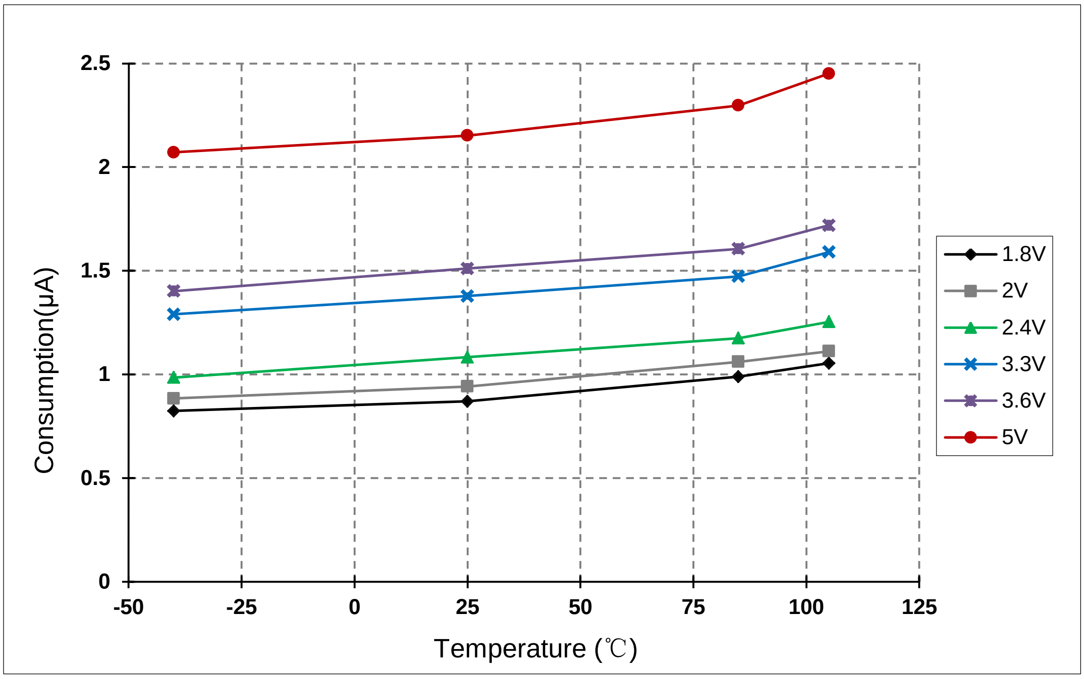


Figure 4-8 Typical current consumption in Stop mode with regulator in run mode versus temperature at different V_{DD} values

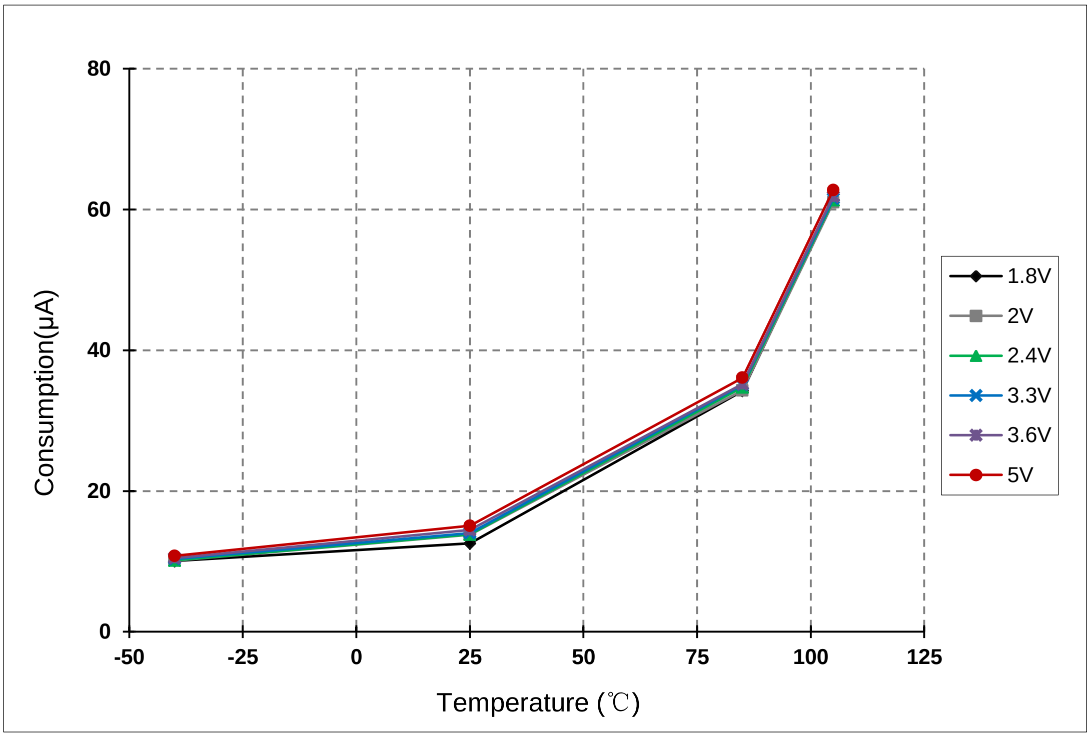


Figure 4-9 Typical current consumption in Stop mode with regulator in low-power mode versus temperature at different V_{DD} values

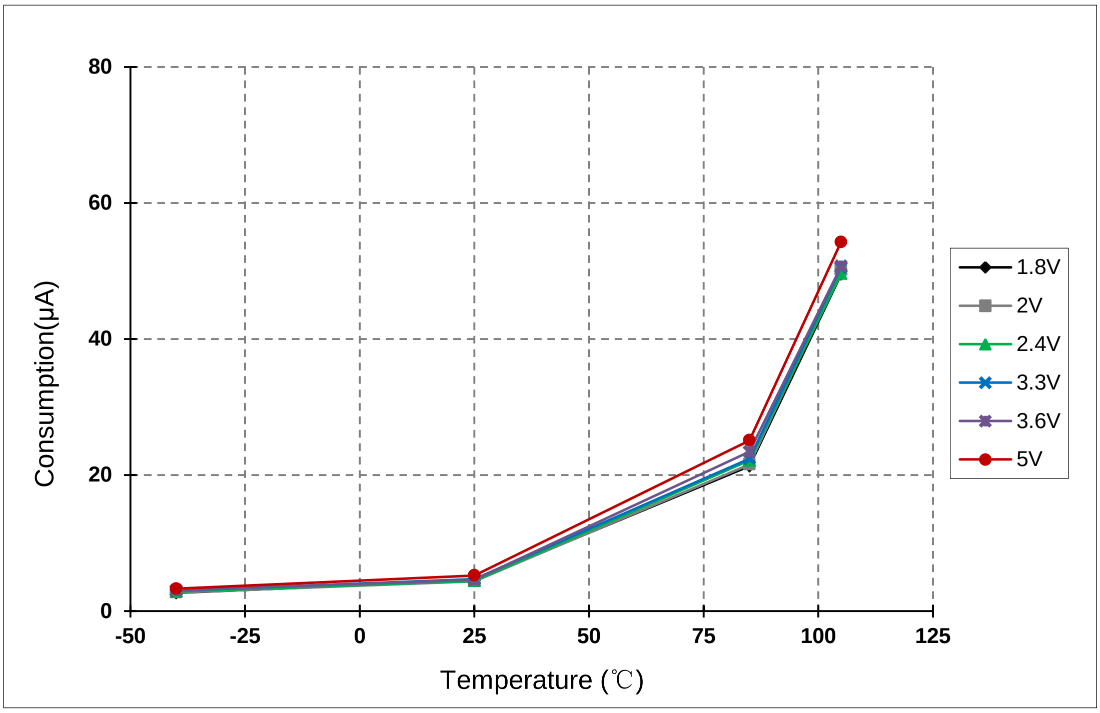
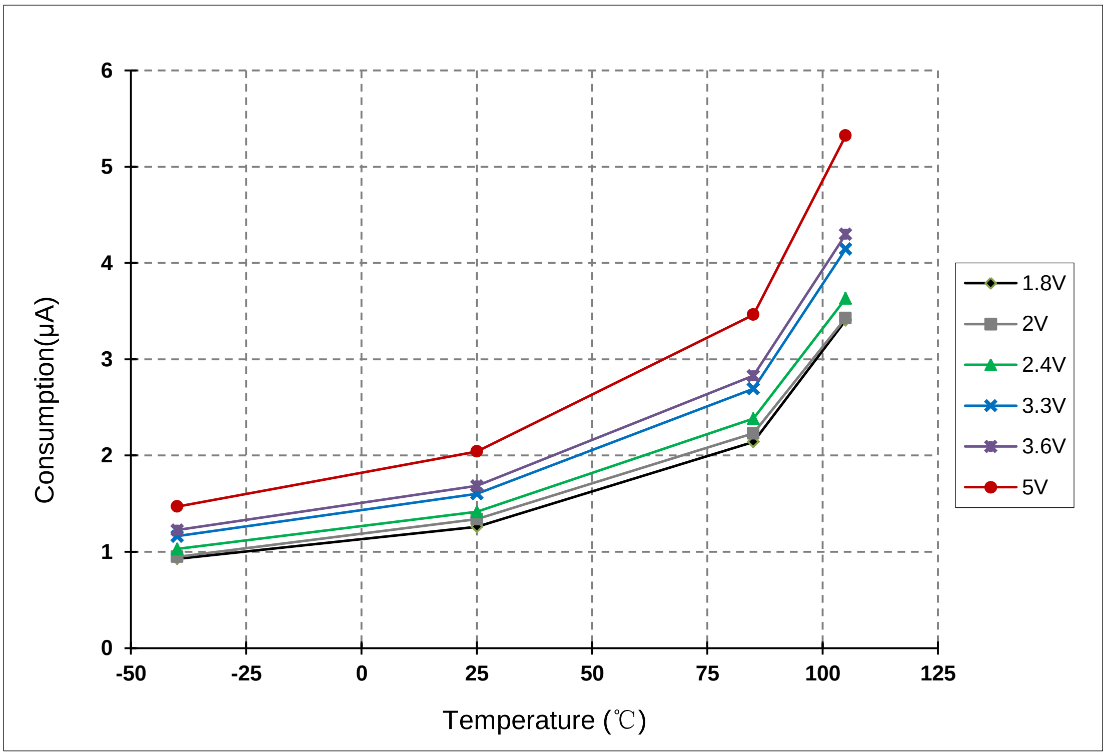


Figure 4-10 Typical current consumption in Standby mode versus temperature at different V_{DD} values



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**.
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling) When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

Table 4-12 Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	72 MHz	14.6	8.6	mA
			48 MHz	10.1	6.1	
			36 MHz	7.0	4.3	
			24 MHz	5.3	3.3	
			16 MHz	3.7	2.4	
			8 MHz	2.0	1.3	
			4 MHz	1.5	1.2	
			2 MHz	1.2	1.0	
			1 MHz	1.0	0.9	
			500 kHz	0.9	0.9	
			125 kHz	0.9	0.9	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	13.2	7.9	
			48 MHz	10.2	6.2	
			36 MHz	7.8	4.9	
			24 MHz	5.3	3.3	
			16 MHz	3.6	2.3	
			8 MHz	1.8	1.1	
			4 MHz	1.2	0.8	
			2 MHz	0.8	0.7	
			1 MHz	0.7	0.6	
			500 kHz	0.6	0.6	
			125 kHz	0.5	0.5	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 1.3 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 4-13 Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ[1]		Unit
				All peripherals enabled[2]	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock[3]	72 MHz	10.1	3.3	mA
			48 MHz	7.0	2.4	
			36 MHz	4.9	1.8	
			24 MHz	3.8	1.5	
			16 MHz	2.7	1.2	
			8 MHz	1.4	0.7	
			4 MHz	1.2	0.8	
			2 MHz	1.0	0.8	
			1 MHz	0.9	0.8	
			500 kHz	0.9	0.8	
			125 kHz	0.8	0.8	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	8.9	5.1	
			48 MHz	6.8	4.0	
			36 MHz	5.2	3.0	
			24 MHz	3.6	2.0	
			16 MHz	2.5	1.4	
			8 MHz	1.2	0.7	
			4 MHz	0.9	0.6	
			2 MHz	0.6	0.6	
			1 MHz	0.6	0.5	
			500 kHz	0.5	0.5	
			125 kHz	0.5	0.5	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 1.3 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in **Table 4-14**. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**.

Table 4-14 Peripheral current consumption

Peripheral		Current consumption	Unit
AHB (up to 72 MHz)	DMA1	5.07	μA/MHz
	DMA2	4.55	
	FSMC	12.90	
	CRC	0.42	
	SDIO	7.92	
	BusMatrix(1)	2.20	
APB1 (up to 36 MHz)	APB1-Bridge	2.80	μA/MHz
	TIM2	6.63	
	TIM3	6.50	
	TIM4	5.81	
	TIM5	5.53	
	TIM6	1.88	
	TIM7	1.82	
	SPI2/I2S2(2)	2.69	
	SPI3/I2S3(2)	2.69	
	USART2	4.54	
	USART3	4.12	
	UART4	3.90	
	UART5	3.70	
	I2C1	3.65	
	I2C2	4.17	
	USB	6.73	
	CAN1	5.68	
	DAC(3)	3.14	
	WWDG	1.33	
	PWR	1.53	
	BKP	1.75	
	IWDG	0.28	
APB2 (up to 72 MHz)	APB2-Bridge	2.80	μA/MHz
	GPIOA	2.72	
	GPIOB	2.20	
	GPIOC	2.74	
	GPIOD	2.43	
	GPIOE	2.30	
	GPIOF	1.84	
	GPIOG	1.92	
	SPI1	1.58	
	USART1	3.76	

Peripheral		Current consumption	Unit
APB2 (up to 72 MHz)	TIM1	7.41	μA/MHz
	TIM8	7.23	
	ADC1[4]	6.30	
	ADC2[4]	5.72	
	ADC3[4]	5.98	

1. The BusMatrix is automatically active when at least one master is ON. (CPU, DMA1 or DMA2).
2. When the I2S is enabled, a current consumption equal to 0.02 mA must be added.
3. When DAC_OU1 or DAC_OUT2 is enabled, a current consumption equal to 0.36 mA must be added.
4. Specific conditions for measuring ADC current consumption: f_{HCLK} = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$. When ADON bit in the ADCx_CR2 register is set to 1, a current consumption of analog part equal to 1.3 mA must be added for each ADC.

4.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in **Table 4-15** result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in **Table 4-4**.

Table 4-15 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency[1]	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time[1]		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time[1]		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance[1]	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	μA

1. Guaranteed by design.

Low-speed external user clock generated from an external source

The characteristics given in **Table 4-16** result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in **Table 4-4**.

Table 4-16 Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency[1]	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time[1]		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time[1]		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance[1]	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 4-11 High-speed external clock source AC timing diagram

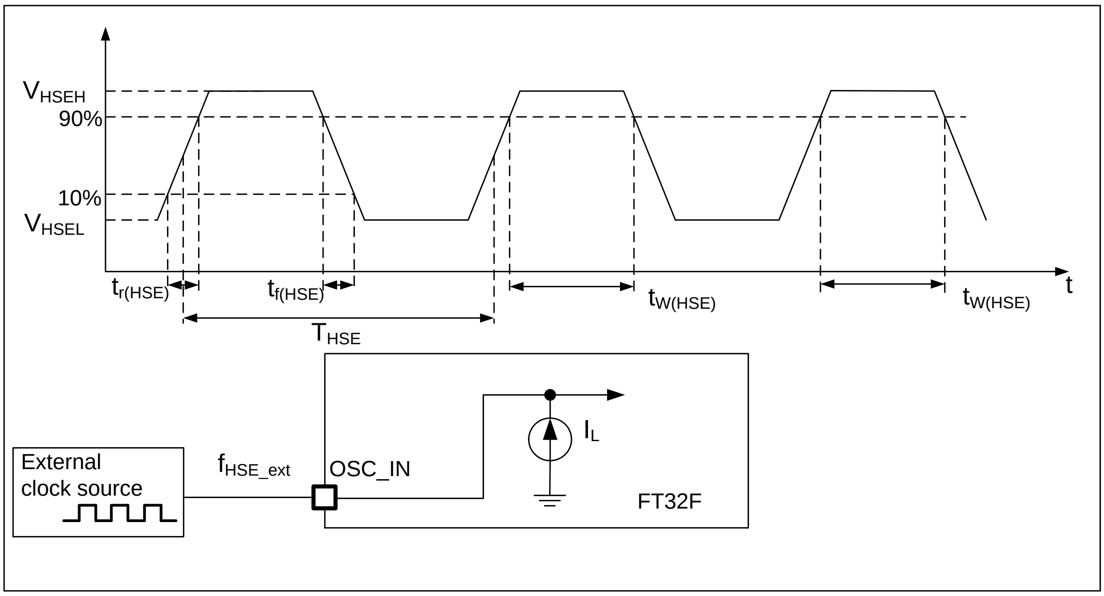
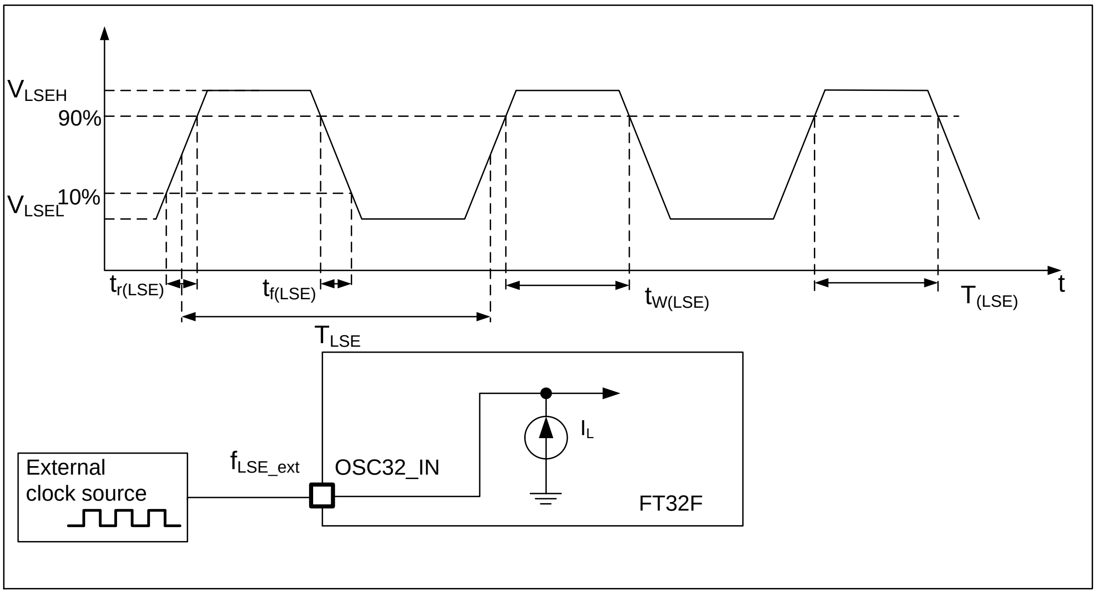


Figure 4-12 Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results obtained with typical external components specified in **Table 4-17**. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 4-17 HSE 4-16 MHz oscillator characteristics (1) (2)

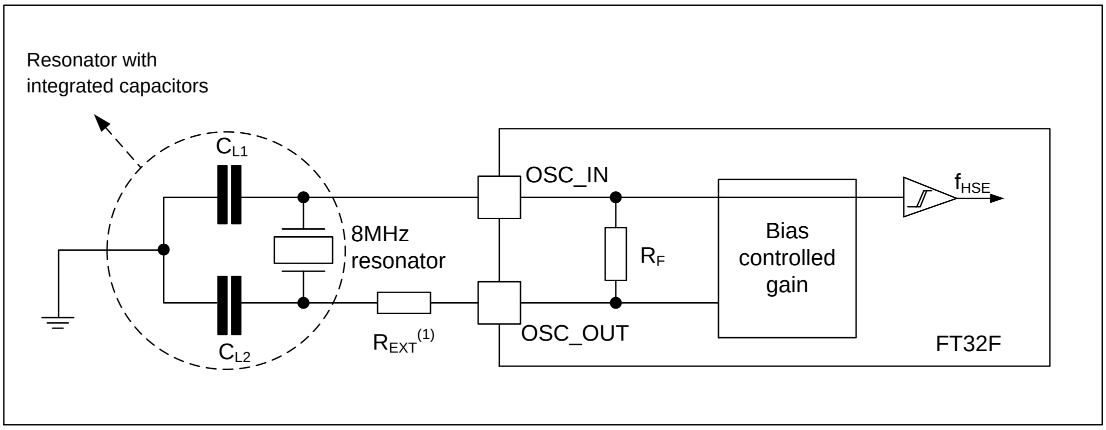
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	3.6	-	MΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	$R_S = 30\Omega$	-	30	-	pF
i_2	HSE driving current	$V_{DD} = 3.3$ V, $V_{IN} = V_{SS}$ with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.

3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see **Figure 4-13**). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Figure 4-13 Typical application with an 8MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in **Table 4-18**. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 4-18 LSE oscillator characteristics (f_{LSE} = 32.768 kHz)$^{(1)(2)}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	15	-	MΩ
$C^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)	R_S = 30 kΩ	-	-	15	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_2	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}		-	-	1.4	µA
g_m	Oscillator transconductance	-		5	-	-	µA/V
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs below the table.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer, PCB layout and humidity.

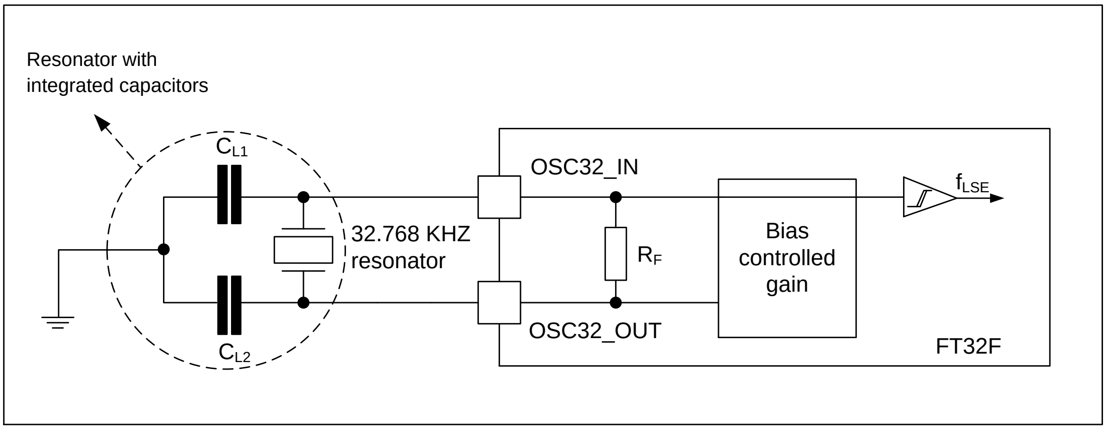
NOTE: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see **Figure 4-14**). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF), it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Figure 4-14 Typical application with a 32.768 kHz crystal



4.3.7 Internal clock source characteristics

The parameters given in **Table 4-19** are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**.

High-speed internal (HSI) RC oscillator

Table 4-19 HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register		-	-	1(2)	%
		Factory-calibrated(3)	T_A = -40 to 105 °C	-2	-	2.5	%
			T_A = -10 to 85 °C	-1.5	-	2.2	%
			T_A = 0 to 70 °C	-1.3	-	2	%
			T_A = 25 °C	-1.1	-	1.8	%
$t_{su(HSI)}$(3)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-		-	80	100	µA

1. V_{DD} = 3.3 V, T_A = -40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.

Low-speed internal (LSI) RC oscillator

Table 4-20 LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.5	µA

1. V_{DD} = 3 V, T_A = -40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Wakeup time from low-power mode

The wakeup times given in **Table 4-21** is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator

- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**.

Table 4-21 Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	22	µs
	Wakeup from Stop mode (regulator in low-power mode)	22	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

4.3.8 PLL characteristics

The parameters given in **Table 4-22** PLL characteristicsare derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**.

Table 4-22 PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

4.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

Table 4-23 Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max[(1)]	Unit
t_{prog}	16-bit programming time	T_A = -40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (2 KB) erase time	T_A = -40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = -40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 72 MHz with 2 wait states, V_{DD} = 3.3 V	-	-	28	mA
		Write mode f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	7	mA
		Erase mode f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	1.8	-	5.0	V

1. Guaranteed by design.

Table 4-24 Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min[(1)]	
N_{END}	Endurance	T_A = -40 to +85 °C (6 suffix versions) T_A = -40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle[(2)] at T_A = 85 °C	30	Years
		1 kcycle[(2)] at T_A = 105 °C	10	
		10 kcycles[(2)] at T_A = 55 °C	20	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

4.3.10 FSMC characteristics

Asynchronous waveforms and timings

Figure 4-15 and **Figure 4-16** represent asynchronous waveforms, **Table 4-25** and **Table 4-26** provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Figure 4-15 Asynchronous multiplexed PSRAM/NOR read waveforms

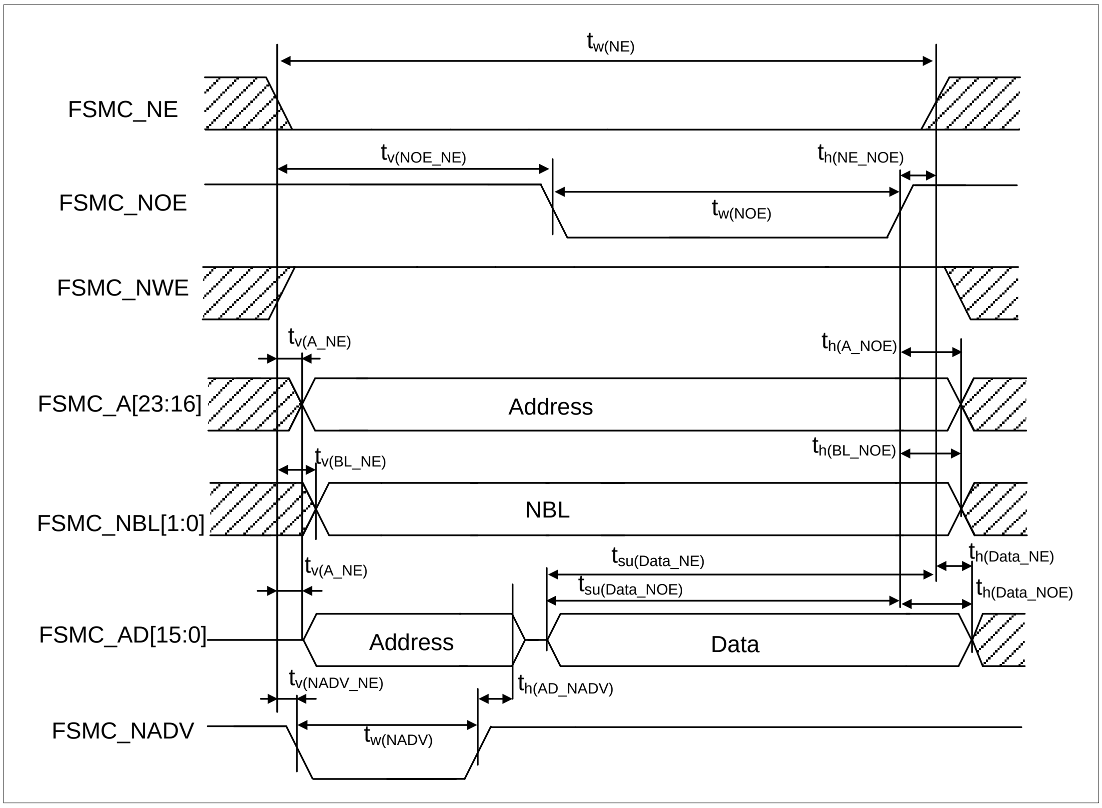


Table 4-25 Asynchronous multiplexed PSRAM/NOR read timings$^{(1)(2)}$

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7t_{HCLK}$ - 2	$7t_{HCLK}$ + 2	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK}$ - 0.5	$3t_{HCLK}$ + 1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4t_{HCLK}$ - 1	$4t_{HCLK}$ + 2	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	-1	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	t_{HCLK} - 1.5	t_{HCLK} + 1.5	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after	t_{HCLK}	-	ns

Symbol	Parameter	Min	Max	Unit
	FSMC_NADV high			
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	t_{HCLK} - 2	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	2t_{HCLK} + 24	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	2t_{HCLK} + 25	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Figure 4-16 Asynchronous multiplexed PSRAM/NOR write waveforms

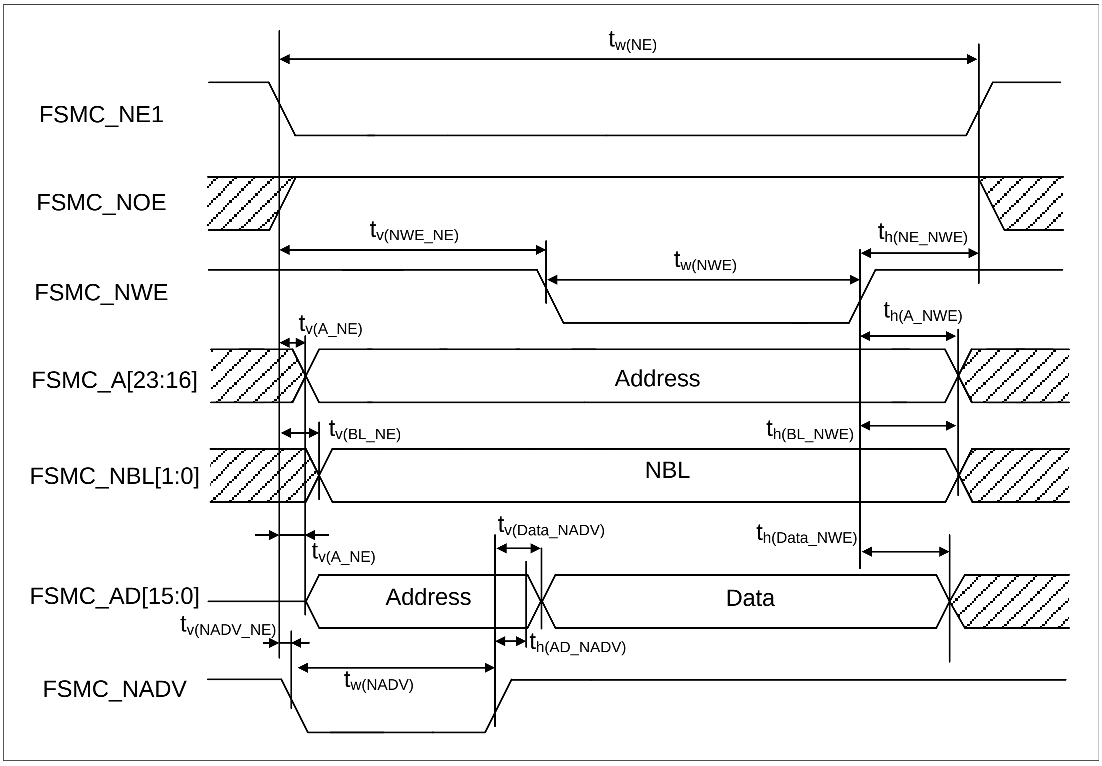


Table 4-26 Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	5t_{HCLK} - 1	5t_{HCLK} + 2	ns
$t_{v(NWE\_NE)}$	FSMC_NE1 low to FSMC_NWE low	2t_{HCLK}	2t_{HCLK} + 1	ns
$t_{w(NWE)}$	FSMC_NWE low time	2t_{HCLK} - 1	2t_{HCLK} + 2	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	t_{HCLK} - 1	-	ns
$t_{v(A\_NE)}$	FSMC_NE1 low to FSMC_A valid	-	7	ns
$t_{v(NADV\_NE)}$	FSMC_NE1 low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	t_{HCLK} - 1	t_{HCLK} + 1	ns

Symbol	Parameter	Min	Max	Unit
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK} - 3	-	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$4t_{HCLK}$	-	ns
$t_{v(BL\_NE)}$	FSMC_NE1 low to FSMC_BL valid	-	1.6	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	t_{HCLK} - 1.5	-	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	t_{HCLK} + 1.5	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	t_{HCLK} – 5	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 4-17 represents synchronous waveforms and **Table 4-27** provides the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the FT32F1x3xx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 4-17 Synchronous multiplexed NOR/PSRAM read timings

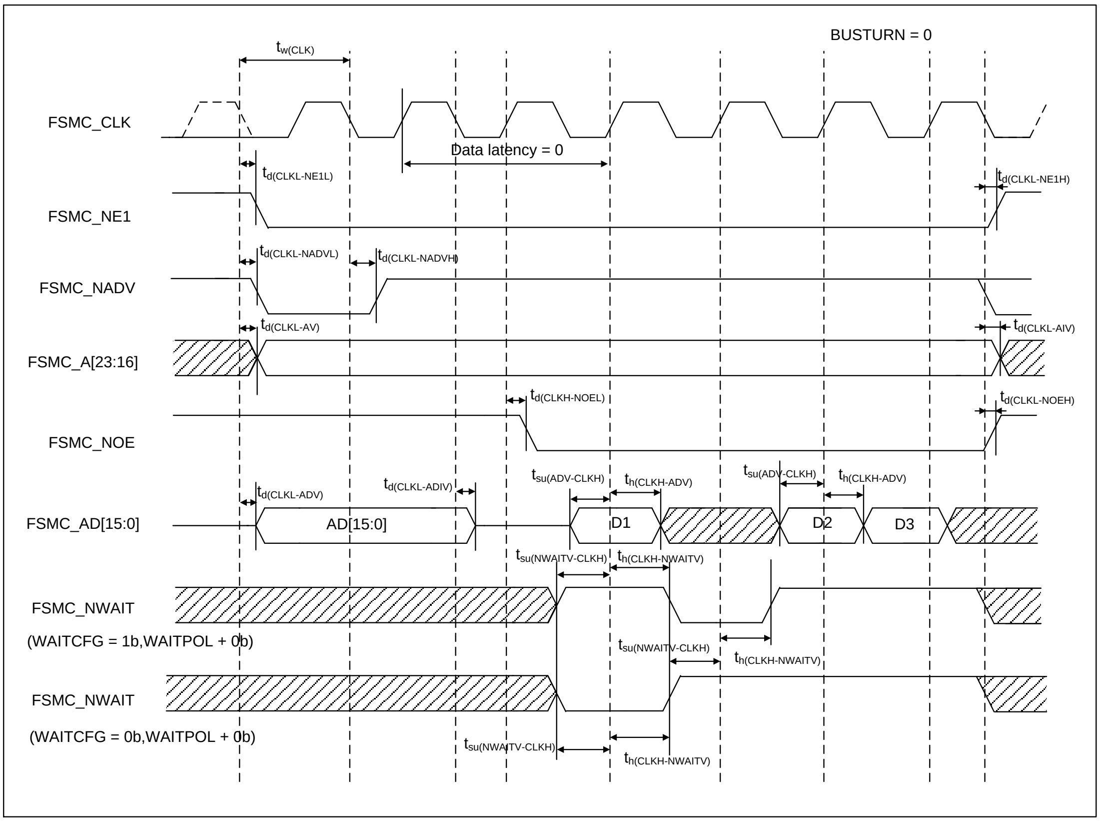


Table 4-27 Synchronous multiplexed NOR/PSRAM read timings[(1)(2)]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NE1L)}$	FSMC_CLK low to FSMC_NE1 low	-	1.5	ns
$t_{d(CLKL-NE1H)}$	FSMC_CLK low to FSMC_NE1 high	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...23)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...23)	2	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 4-18 through **Figure 4-21** represent synchronous waveforms. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime =0x03;
- COM.FSMC_HoldSetupTime =0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 4-18 NAND controller waveforms for read access

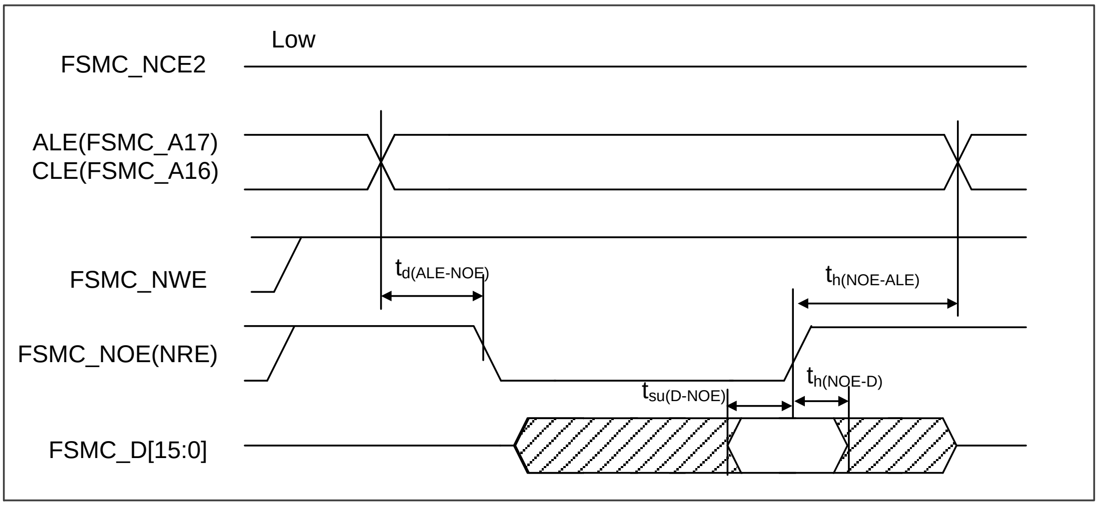


Figure 4-19 NAND controller waveforms for write access

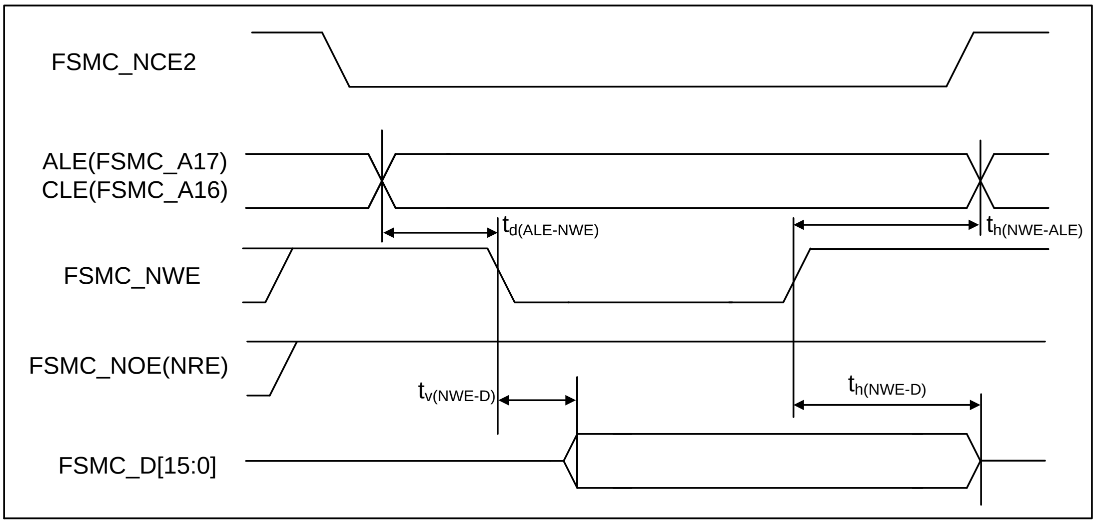


Figure 4-20 NAND controller waveforms for common memory read access

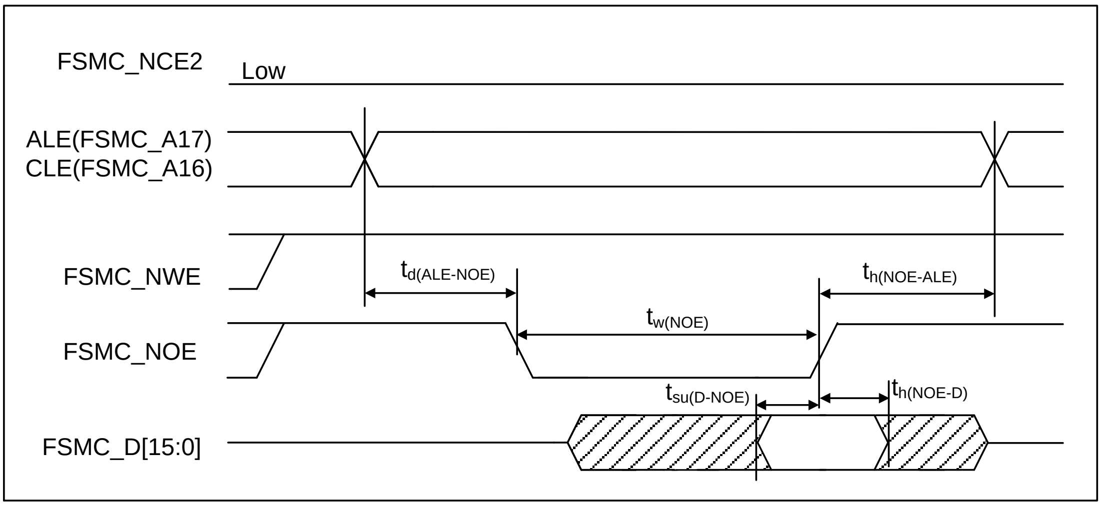


Figure 4-21 NAND controller waveforms for common memory write access

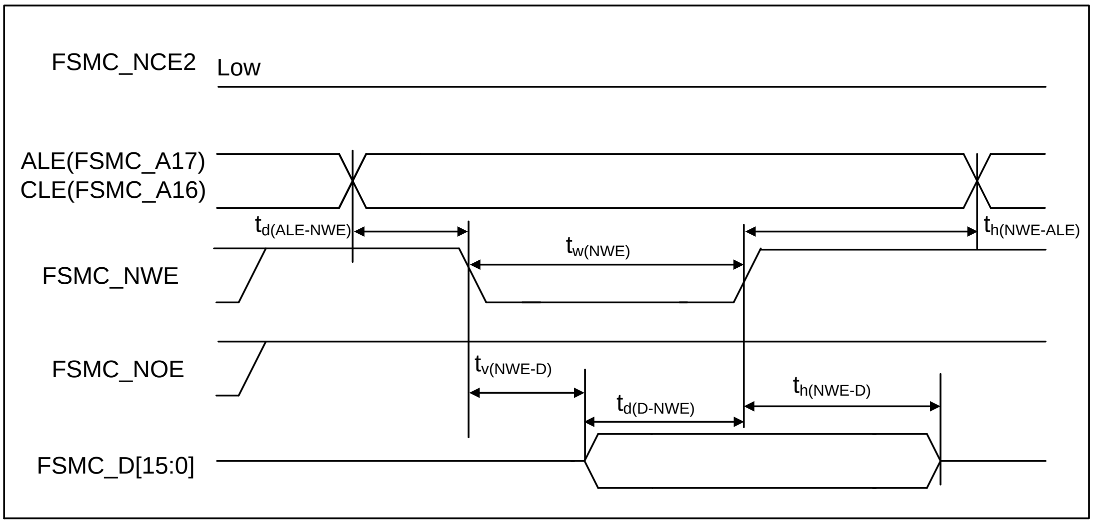


Table 4-28 Switching characteristics for NAND Flash read and write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$(2)	FSMC_D[15:0] valid before FSMC_NWE high	$5t_{HCLK} + 12$	-	ns
$t_{w(NOE)}$(2)	FSMC_NWE low width	$4t_{HCLK} - 1.5$	$4t_{HCLK} + 1.5$	ns
$t_{su(D-NOE)}$(2)	FSMC_D[15:0] valid data before FSMC_NOE high	25	-	ns
$t_{h(NOE-D)}$(2)	FSMC_D[15:0] valid data after FSMC_NOE high	7	-	-
$t_{w(NWE)}$(2)	FSMC_NWE low width	$4t_{HCLK} - 1$	$4t_{HCLK} + 1$	ns
$t_{v(NWE-D)}$(2)	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$(2)	FSMC_NWE high to FSMC_D[15:0] invalid	$2t_{HCLK} + 4$	-	ns
$t_{d(ALE-NWE)}$(3)	FSMC_ALE valid before FSMC_NWE low	-	$3t_{HCLK} + 1.5$	ns
$t_{h(NWE-ALE)}$(3)	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK} + 4.5$	-	ns
$t_{d(ALE-NOE)}$(3)	FSMC_ALE valid before FSMC_NOE low	-	$3t_{HCLK} + 2$	ns
$t_{h(NOE-ALE)}$(3)	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK} + 4.5$	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.
3. Guaranteed by design.

4.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). The device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

Table 4-29 EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE-J1752/3 standard which specifies the test board and the pin loading.

Table 4-30 EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, compliant with SAE-J1752/3	0.1 to 30 MHz	8	12	dB/µV
			30 to 130 MHz	31	21	
			130 MHz to 1GHz	28	33	
			SAE EMI Level	4	4	-

4.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the MIL-STD-883 / JS-002 standard.

Table 4-31 ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Min (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to MIL-STD-883	3A	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JS-002	C3	1000	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78 IC latch-up standard.

Table 4-32 Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	V_{DD} = 3.6 V, T_A = +105 °C conforming to JESD78	II level A

4.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

Table 4-33 I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

4.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in **Table 4-34** are derived from tests performed under the conditions summarized in **Table 4-4**. All I/Os are CMOS and TTL compliant.

Table 4-34 I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage	-	-0.3	-	0.28*(V_{DD} - 2) + 0.8	V
	IO FT[1] input low level voltage		-0.3	-	0.32*(V_{DD} - 2) +0.75	V
V_{IH}	Standard IO input high level voltage	-	0.41*(V_{DD} - 2) + 1.3	-	V_{DD} + 0.3	V
	IO FT[1] input high level voltage	V_{DD} > 2 V	0.42*(V_{DD} - 2) + 1	-	5.5	V
		V_{DD} ≤ 2 V			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis[2]	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis[2]		5% V_{DD}[3]	-	-	mV
I_{lkg}	Input leakage current[4]	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	3	-	
R_{PU}	Weak pull-up equivalent resistor[5]	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor[5]	$V_{IN} = V_{DD}$	30	40	50	KΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD} + 0.3V the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. If negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in **Figure 4-22** and **Figure 4-23** for standard I/Os, and in **Figure 4-24** and **Figure 4-25** for 5 V tolerant I/Os.

Figure 4-22 Standard I/O input characteristics - CMOS port

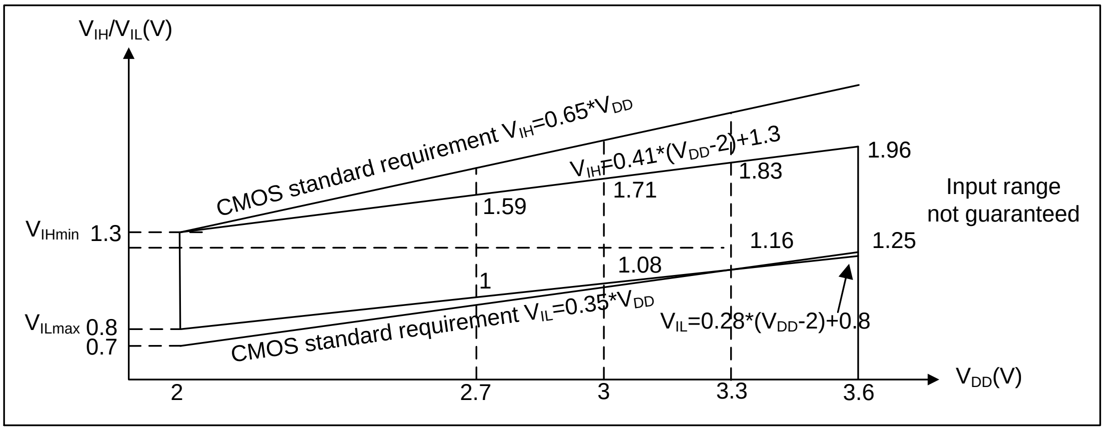


Figure 4-23 Standard I/O input characteristics - TTL port

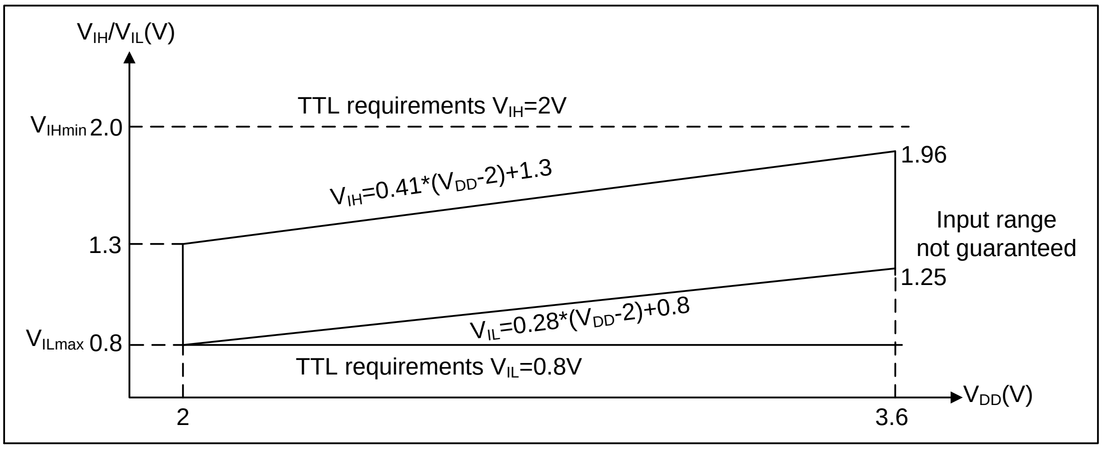


Figure 4-24 5 V tolerant I/O input characteristics - CMOS port

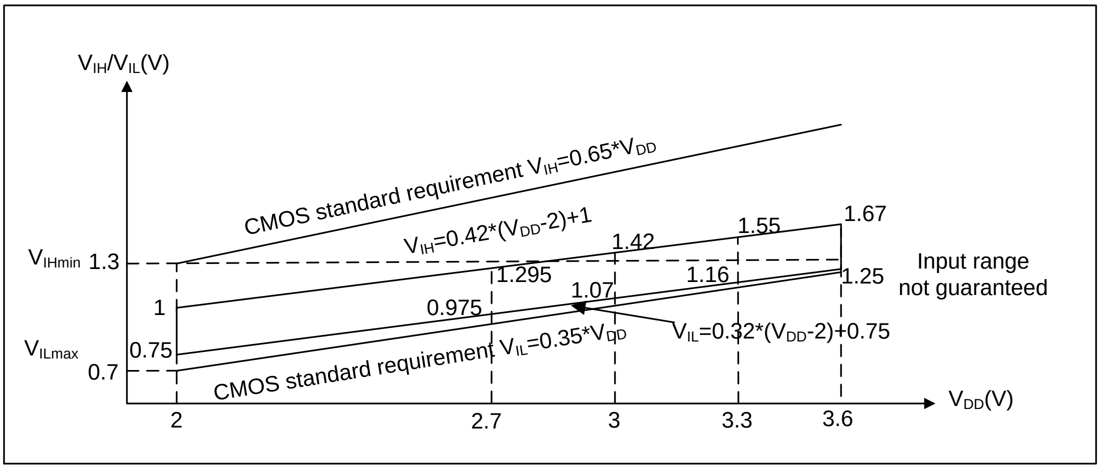
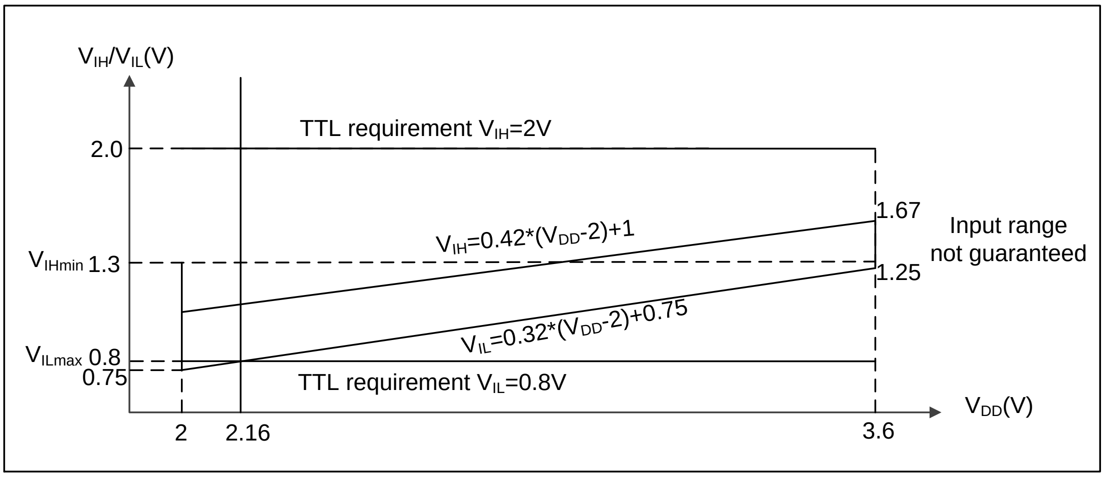


Figure 4-25 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3 mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in 4.2 Absolute maximum ratings:

- The sum of the currents sourced by all the I/Os on V_{DD} plus the maximum Run consumption of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating I_{VDD} (see **Table 4-2**).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see **Table 4-2**).

Output voltage levels

Unless otherwise specified, the parameters given in **Table 4-35** are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**. All I/Os are CMOS and TTL compliant.

Table 4-35 Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(3), I_{IO} = +8 mA 2.7 V < VDD < 5.0 V	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD} - 0.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(3), I_{IO} = +8mA 2.7 V < VDD < 5.0 V	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	I_{IO} = +20 mA	-	1.3	V

Symbol	Parameter	Conditions	Min	Max	Unit
	when 8 pins are sunk at same time	2.7 V < V_{DD} < 5.0 V			
$V_{OH}^{(2)(4)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD} - 1.3	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
$V_{OH}^{(2)(4)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD} - 0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in **Table 4-2** and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in **Table 4-2** and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. Guaranteed by characterization results.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in **Figure 4-26** and **Table 4-36**, respectively.

Unless otherwise specified, the parameters given in **Table 4-36** are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**.

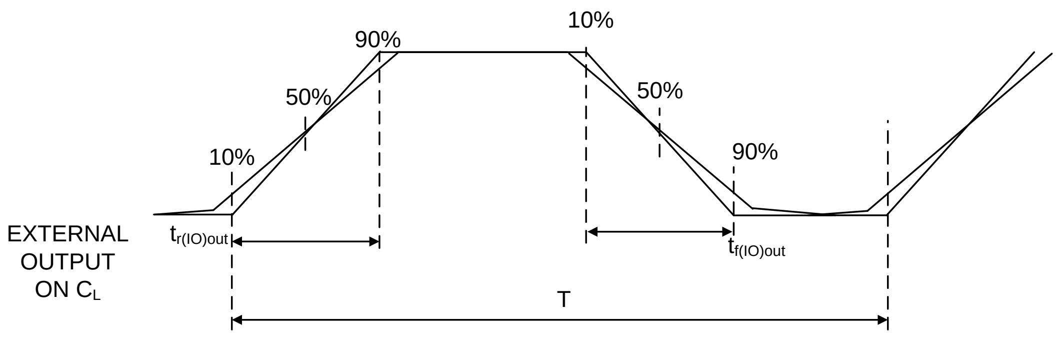
Table 4-36 I/O AC characteristics (1)

MODEx[1:0] bit value	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 5.0 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 5.0 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 5.0 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 5.0 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 5.0 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 5.0 V	-	30	MHz
			C_L = 50 pF,	-	20	MHz

MODEx[1:0] bit value	Symbol	Parameter	Conditions	Min	Max	Unit
			V_{DD} = 2 V to 2.7 V			
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 5.0 V	-	5[3]	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 5.0 V	-	8[3]	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12[3]	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 5.0 V	-	5[3]	
			C_L = 50 pF, V_{DD} = 2.7 V to 5.0 V	-	8[3]	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12[3]	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the FT32F1x3xx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in **Figure 4-26**.
3. Guaranteed by design.

Figure 4-26 I/O AC characteristics definition



Maximum frequency is achieved if $(t_r+t_f) \leq (2/3)T$ and if the duty cycle is (45-55%)
when loaded by C_L specified in the table "I/O AC characteristics"

4.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see **Table 4-34**).

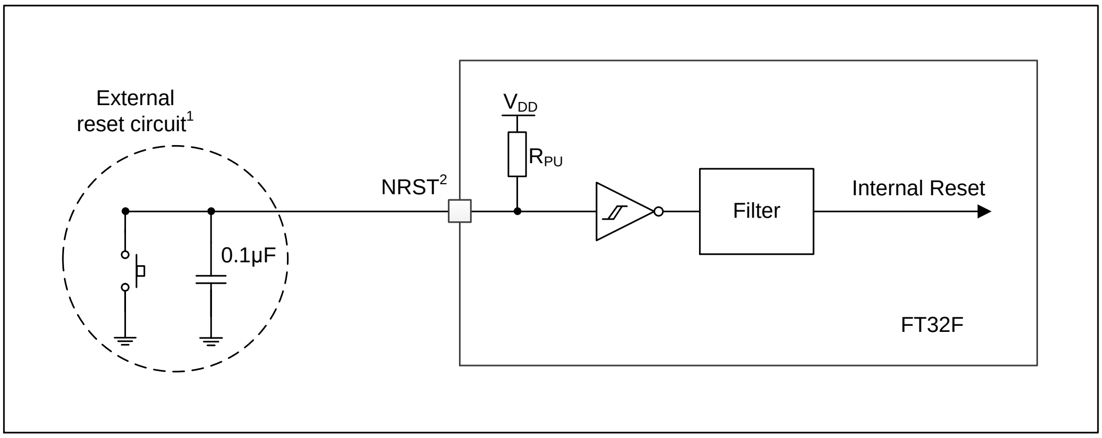
Unless otherwise specified, the parameters given in **Table 4-37** are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in **Table 4-4**.

Table 4-37 NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage	V_{DD} = 2.0~3.6 V	-0.5	-	0.8	V
		V_{DD} = 1.8~5.0 V	-0.5	-	$0.42*V_{DD}-0.2$	
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage	V_{DD} = 2.0~3.6 V	2	-	$V_{DD}+0.5$	
		V_{DD} = 1.8~5.0 V	$0.46*V_{DD}+0.4$	-	$V_{DD}+0.5$	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor$^{(2)}$	$V_{IN} = V_{SS}$	7.5	10	12.5	kΩ
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 4-27 Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in **Table 4-37** NRST pin characteristics.Otherwise the reset will not be taken into account by the device.

4.3.16 TIM timer characteristics

The parameters given in **Table 4-38** are guaranteed by design.

Refer to 4.3.14 I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 4-38 TIMx(1) characteristcs

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$ / 2	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 x 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers

4.3.17 Communications interfaces

I2C interface characteristics

The FT32F103xC/D/E microcontroller performance line I2C interface meets the requirements of the standard I2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to be not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I2C characteristics are described in **Table 4-39**.

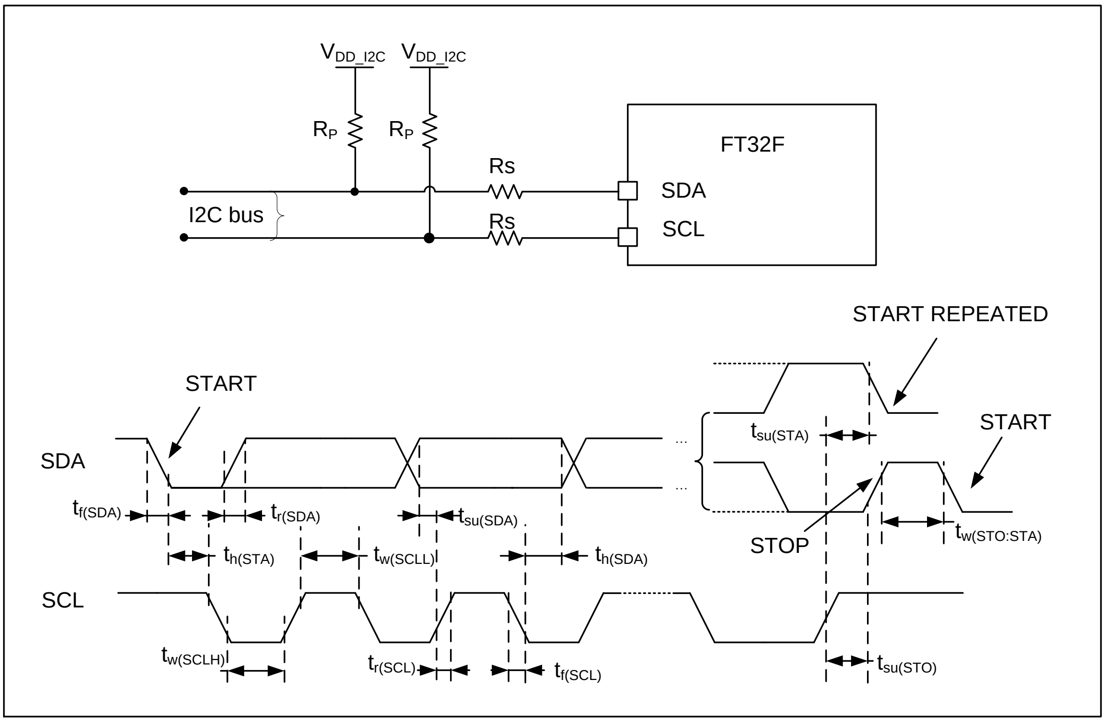
Refer also to 4.3.14 I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 4-39 I2C characteristics

Symbol	Parameter	Standard mode I2C(1)(2)		Fast mode I2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	µs
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	µs
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	0	50(4)	0	50(4)	ns

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I2C frequencies. It must be at least 4 MHz to achieve the fast mode I2C frequencies and it must be a multiple of 10 MHz in order to reach the I2C fast mode maximum clock speed of 400 kHz.
3. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region on the falling edge of SCL.
4. The minimum width of the spikes filtered by the analog filter is above t_{SP}(max).

Figure 4-28 I2C bus AC wavaforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs: Series protection resistors.
3. Rp: Pull-up resistors.
4. VDD_I2C : I2C bus supply

Table 4-40 SCL frequency (f_{PCLK1}= 36 MHz ,V_{DD_I2C} = 3.3 V)$^{(1)(2)}$

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 KΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I2C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

I2S - SPI characteristics

Unless otherwise specified, the parameters given in **Table 4-41** for SPI or in **Table 4-42** for I2S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in **Table 4-4**.

Refer to 4.3.14 I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I2S).

Table 4-41 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}^{(1)}$	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}^{(1)}$	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}^{(1)}$	Data input setup time	Master mode	5	-	
$t_{su(SI)}^{(1)}$		Slave mode	5	-	
$t_{h(MI)}^{(1)}$	Data input hold time	Master mode	5	-	
$t_{h(SI)}^{(1)}$		Slave mode	4	-	
$t_{a(SO)}^{(1)(2)}$	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}^{(1)(3)}$	Data output disable time	Slave mode	2	10	
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}^{(1)}$		Master mode (after enable edge)	2	-	

1. Guaranteed by characterization results.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 4-29 SPI timing diagram - slave mode and CPHA = 0

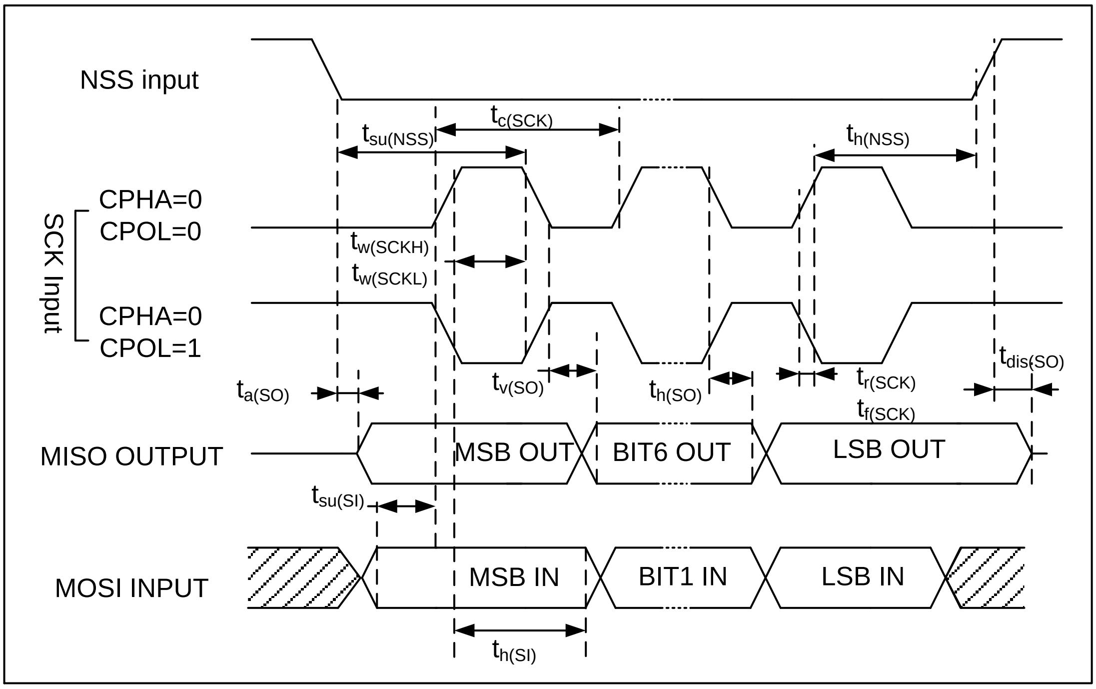
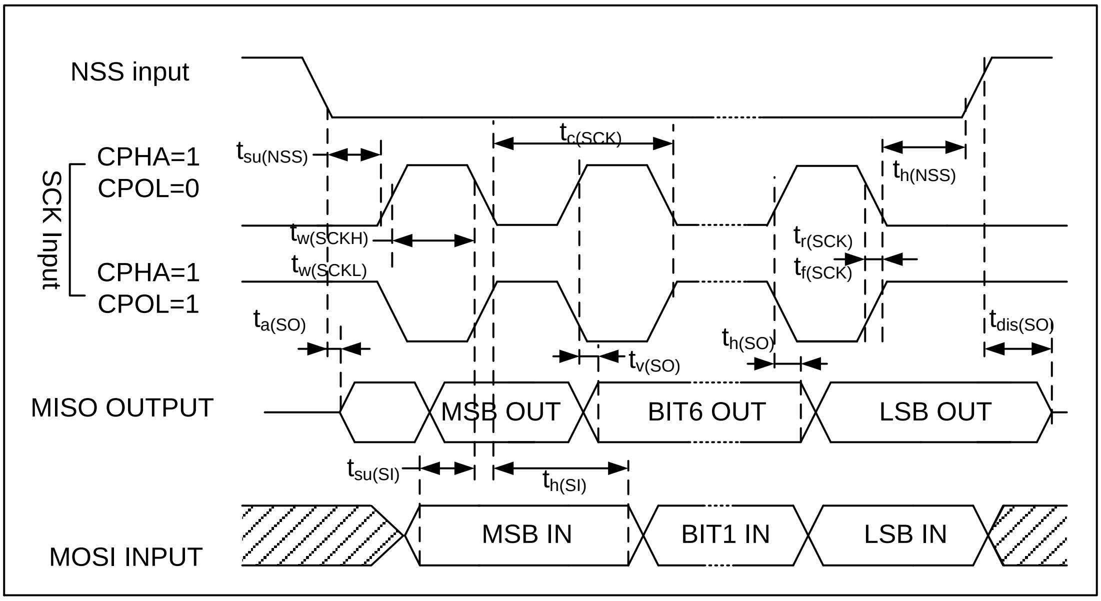
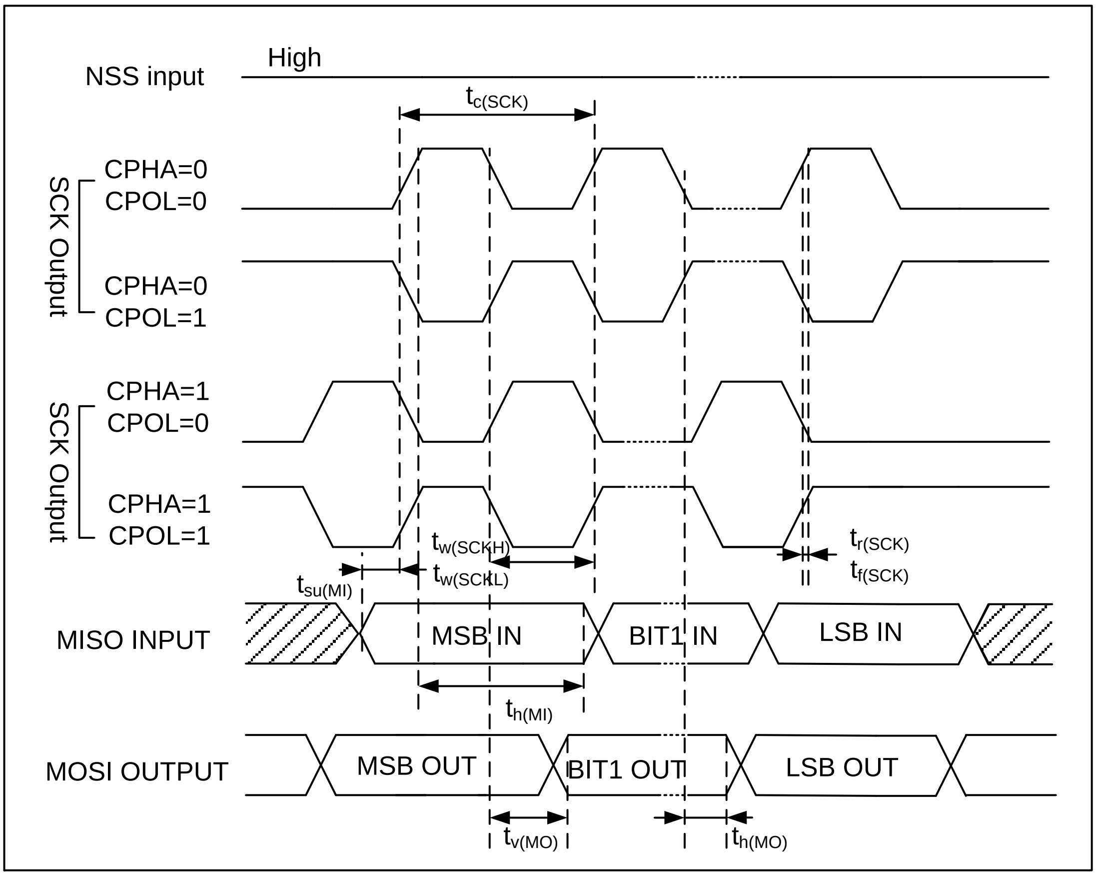


Figure 4-30 SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 4-31 SPI timing diagram - master mode[1]



1. Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

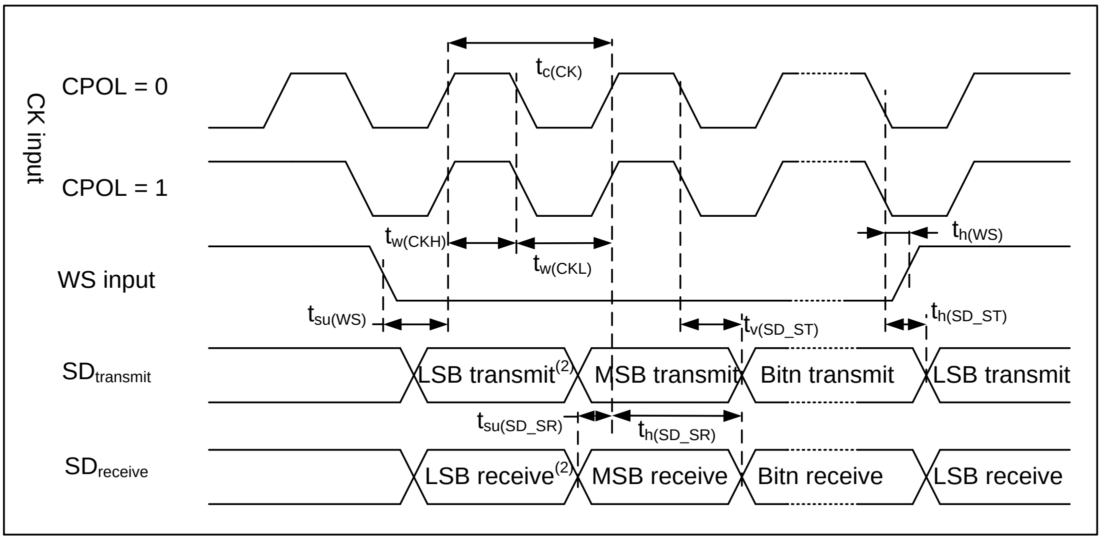
Table 4-42 I2S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode		30	70	%
f_{CK} $1/t_{c(CK)}$	I2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)		1.522	1.525	MHz
		Slave mode		0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I2S clock rise and fall time	Capacitive load C_L = 50 pF		-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode		3	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	I2S2	2	-	
			I2S3	0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode		4	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode		0	-	
$t_{w(CKH)}$ (1)	CK high and low time	Master f_{PCLK}= 16 MHz, audio frequency = 48kHz		312.5	-	
$t_{w(CKL)}$ (1)				345	-	
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	I2S2	2	-	

Symbol	Parameter	Conditions		Min	Max	Unit
			I2S3	6.5	-	
$t_{su(SD\_SR)}$ (1)	Data input setup time	Slave receiver		1.5	-	
$t_{h(SD\_MR)}$ (1)(2)	Data input hold time	Master receiver		0	-	
$t_{h(SD\_SR)}$ (1)(2)		Slave receiver		0.5	-	
$t_{v(SD\_ST)}$ (1)(2)	Data output valid time	Slave transmitter (after enable edge)		-	18	
$t_{v(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)		11	-	
$t_{v(SD\_MT)}$ (1)(2)	Data output valid time	Master transmitter (after enable edge)		-	3	
$t_{vh(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)		0	-	

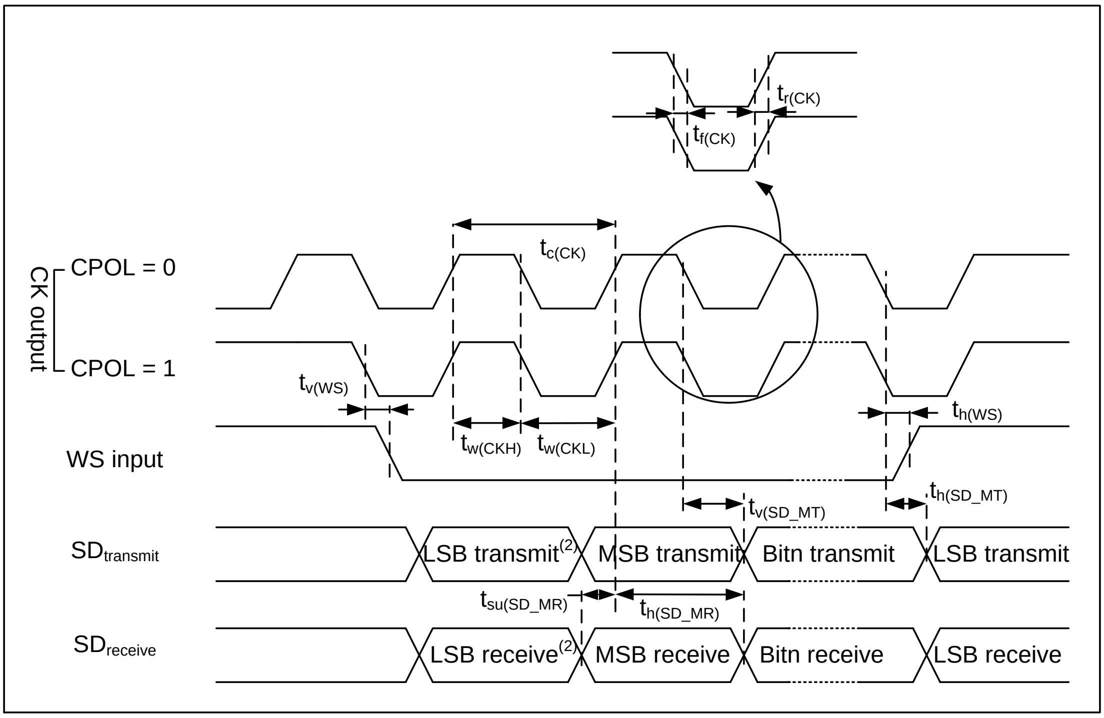
1. Guaranteed by design and/or characterization results.
2. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PLCLK} =125 ns.

Figure 4-32 I2S slave timing diagram(Philips protocol)(1)



1. Measurement points are done at CMOS levels: 0.3*V_{DD} and 0.7*V_{DD}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 4-33 I2S master timing diagram (Philips protocol)(0)



1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in **Table 4-43** are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in **Table 4-4**.

Refer to 4.3.14 I/O port characteristics for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 4-34 SDIO high-speed mode

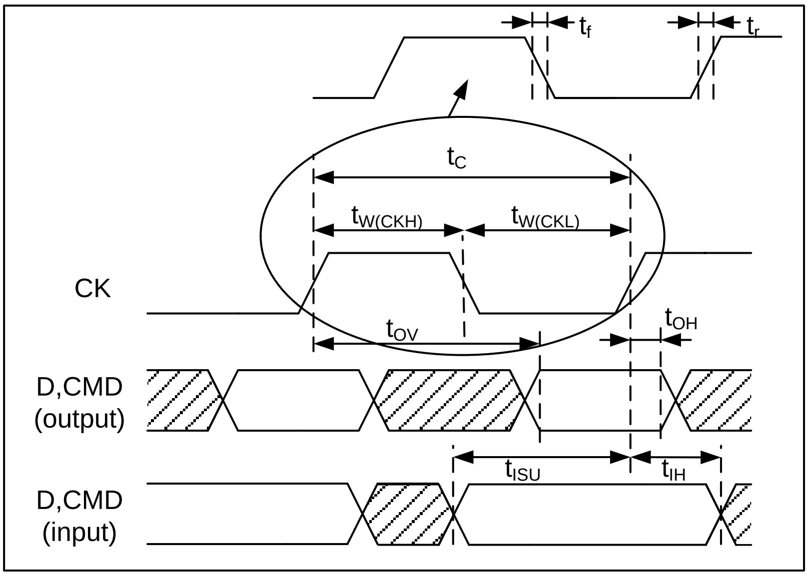


Figure 4-35 SD default mode

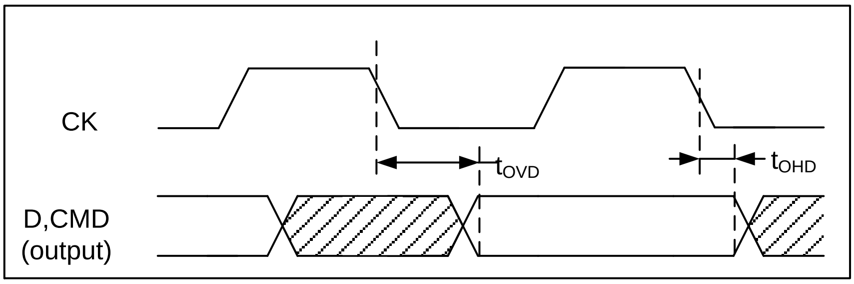


Table 4-43 SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leq 30$ pF	0	48	MHz
$t_{W(CKL)}$	Clock low time, $f_{PP} = 16$ MHz	$C_L \leq 30$ pF	32	-	ns
$t_{W(CKH)}$	Clock high time, $f_{PP} = 16$ MHz	$C_L \leq 30$ pF	30	-	
t_r	Clock rise time	$C_L \leq 30$ pF	-	4	
t_f	Clock fall time	$C_L \leq 30$ pF	-	5	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leq 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leq 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \leq 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \leq 30$ pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 4-44 USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 4-45 USB DC electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0 to 3.6 V voltage range.
3. The FT32F103xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0V V_{DD} voltage range.
4. Guaranteed by characterization results.
5. R_L is the load connected on the USB drivers

Figure 4-36 USB timings: definition of data signal rise and fall time

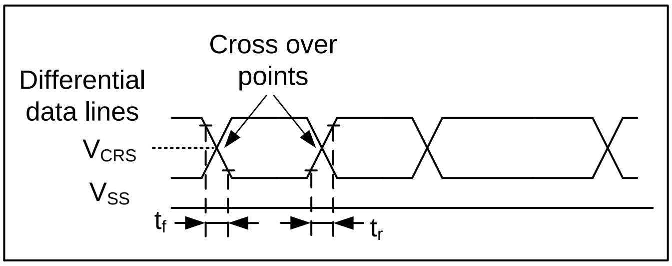


Table 4-46 USB: full-speed electrical characteristics

Driver characteristics(1)					
Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall Time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise / fall time matching	t_r / t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification.

4.3.18 CAN (controller area network) interface

Refer to 4.3.14 I/O port characteristics for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

4.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in **Table 4-47** are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in **Table 4-4**.

Note: It is recommended to perform a calibration after each power-up.

Table 4-47 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	5.0	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0			V
I_{VREF}	Current on the V_{REF} input pin	-	-	160 (1)	220	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{ADC}(2)	Sampling switch resistance	-	-	1	-	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	10	-	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5(5)	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by characterization results.
2. Guaranteed by design.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to 1.1 Pinouts and 1.2 Pin descriptions for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in **Table 4-47**.
5. In order to obtain the best accuracy, it is recommended to use 7.5 * $1/f_{ADC}$ when V_{DD} < 2.8 V.

Table 4-48 ADC accuracy - limited test conditions(1)(2)

Symbol	Parameter	Test conditions	Typ	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, V_{DDA} = 3 V to 5 V, T_A = 25 °C, Measurements made after ADC calibration, V_{REF+} = V_{DDA}	±1.5	LSB
EO	Offset error		±1.0	
EG	Gain error		±1.0	
ED	Differential linearity error		±1.0	
EL	Integral linearity error		±1.0	

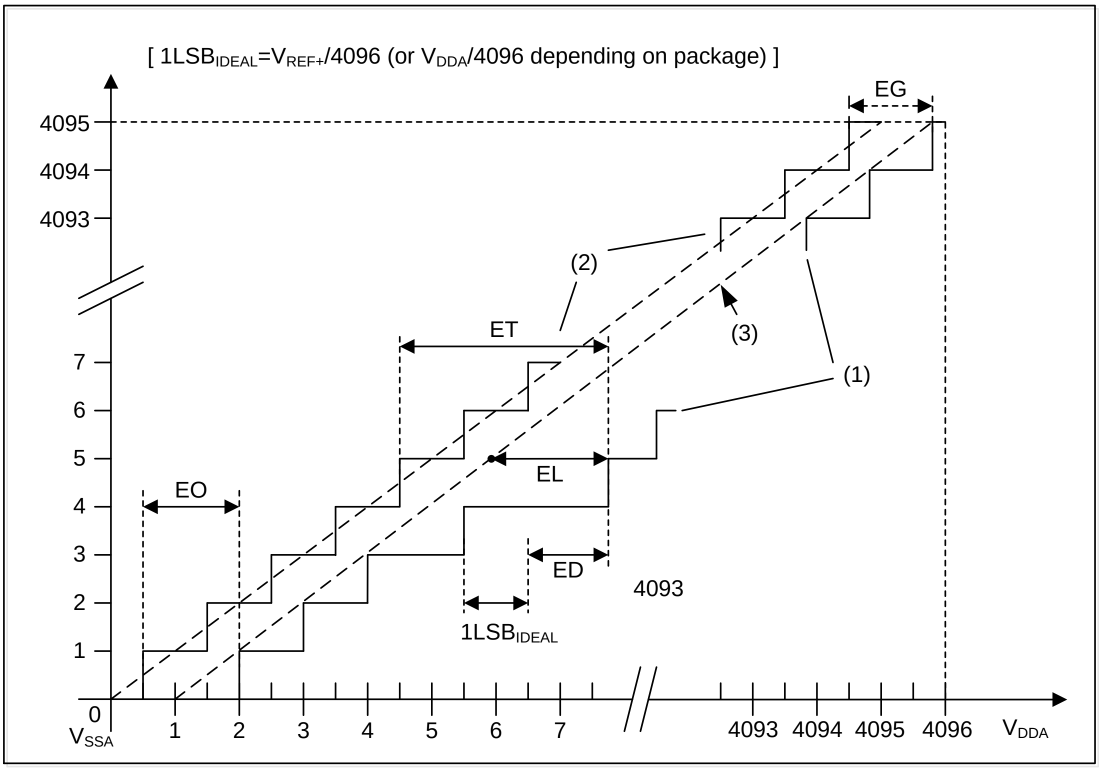
1. ADC DC accuracy values are measured after internal calibration, sampling time is 7.5 * 1/f_{ADC}。
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\sum I_{INJ(PIN)}$ in 4.3.13 I/O current injection characteristics does not affect the ADC accuracy.

Table 4-49 ADC accuracy(1)(2)(3)

Symbol	Parameter	Test conditions	Typ	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, V_{DDA} = 2.4 V to 5 V, Measurements made after ADC calibration	±2.0	LSB
EO	Offset error		±1.5	
EG	Gain error		±1.5	
ED	Differential linearity error		±1.0	
EL	Integral linearity error		±1.5	

1. ADC DC accuracy values are measured after internal calibration, sampling time is 7.5 * 1/f_{ADC}。
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\sum I_{INJ(PIN)}$ in 4.3.13 I/O current injection characteristics does not affect the ADC accuracy.

Figure 4-37 ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. ET = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.

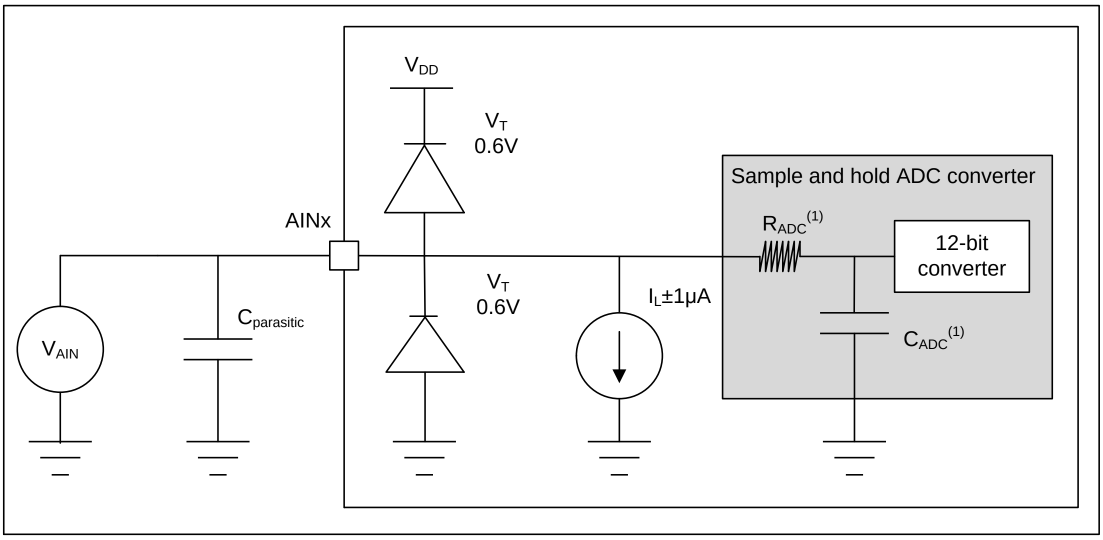
   EO = Offset Error: deviation between the first actual transition and the first ideal one.

   EG = Gain Error: deviation between the last ideal transition and the last actual one.

   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.

   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 4-38 Typical connection diagram using the ADC

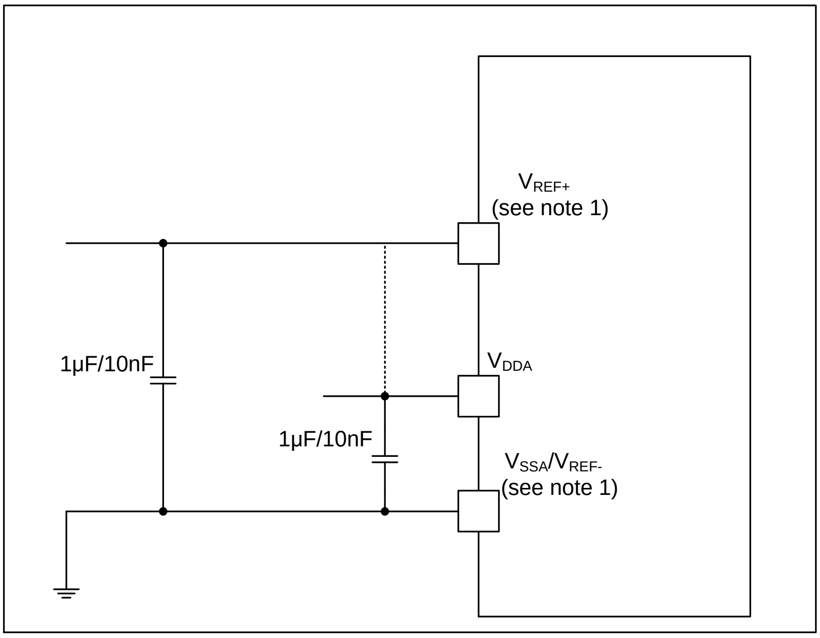


1. Refer to **Table 4-47** for the values of R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance. A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

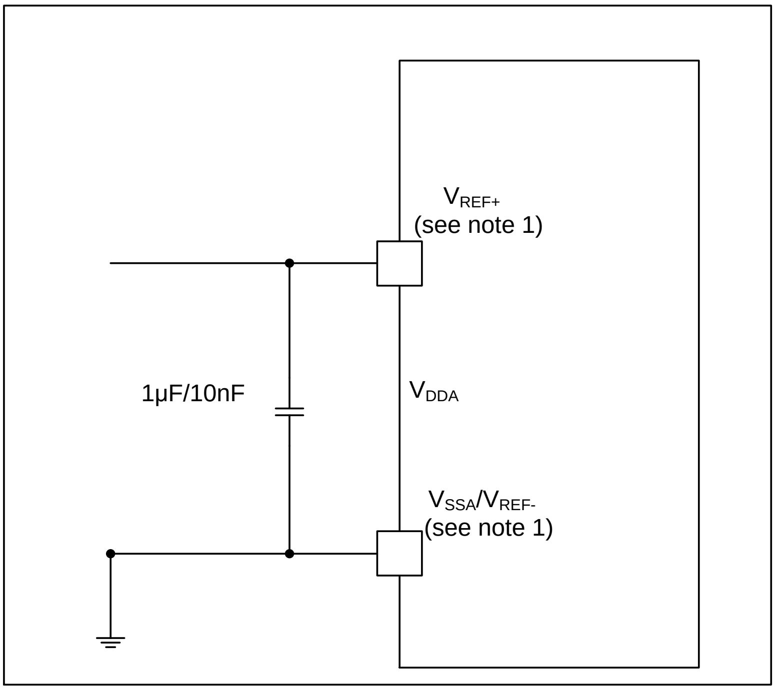
Power supply decoupling should be performed as shown in **Figure 4-39** or **Figure 4-40**, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 4-39 Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages

Figure 4-40 Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

4.3.20 DAC electrical specifications

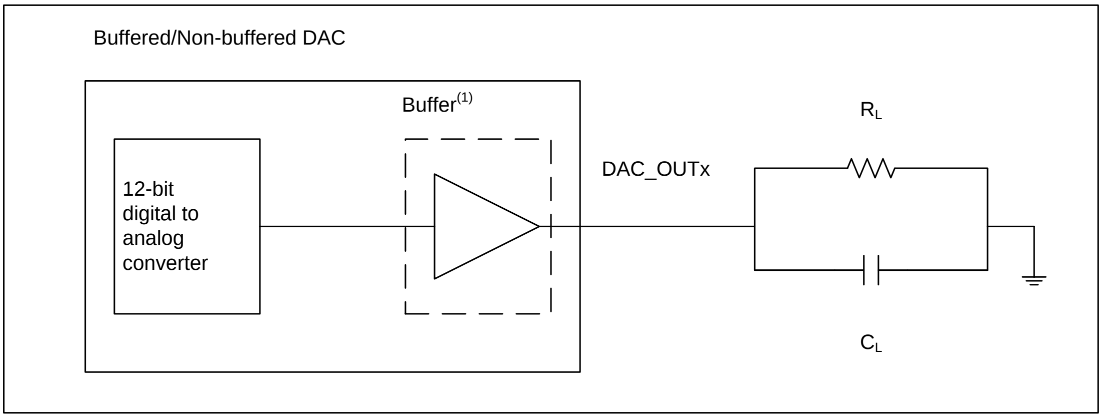
Table 4-50 DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	5.0	V	-
V_{REF+}	Reference supply voltage	2.4	-	5.0	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(2)	Impedance output with buffer OFF	-	15	-	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output Excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) and (0xEAB) at V_{REF+} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} - 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} - 1LSB	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}	DAC DC current consumption in quiescent mode(3)	-	-	380	µA	With no load, middle code (0x800) on the inputs
		-	-	480	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(4)	Differential non linearity Difference between two consecutive code - 1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
		-	-	±2	LSB	Given for the DAC in 12-bit configuration
INL(3)	Integral non linearity	-	-	±1	LSB	Given for the DAC in 10-bit

Symbol	Parameter	Min	Typ	Max	Unit	Comments
	(difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)					configuration
		-	-	±4	LSB	Given for the DAC in 12-bit configuration
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+} / 2)	-	-	±10	mV	-
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(3)	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}$(3)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF,$R_{LOAD} \geq 5$kΩ
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1 LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
P_{SRR+}(1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	-67	-40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design.
2. Guaranteed by characterization.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results.

Figure 4-41 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

4.3.21 Temperature sensor characteristics

Table 4-51 TS characteristics

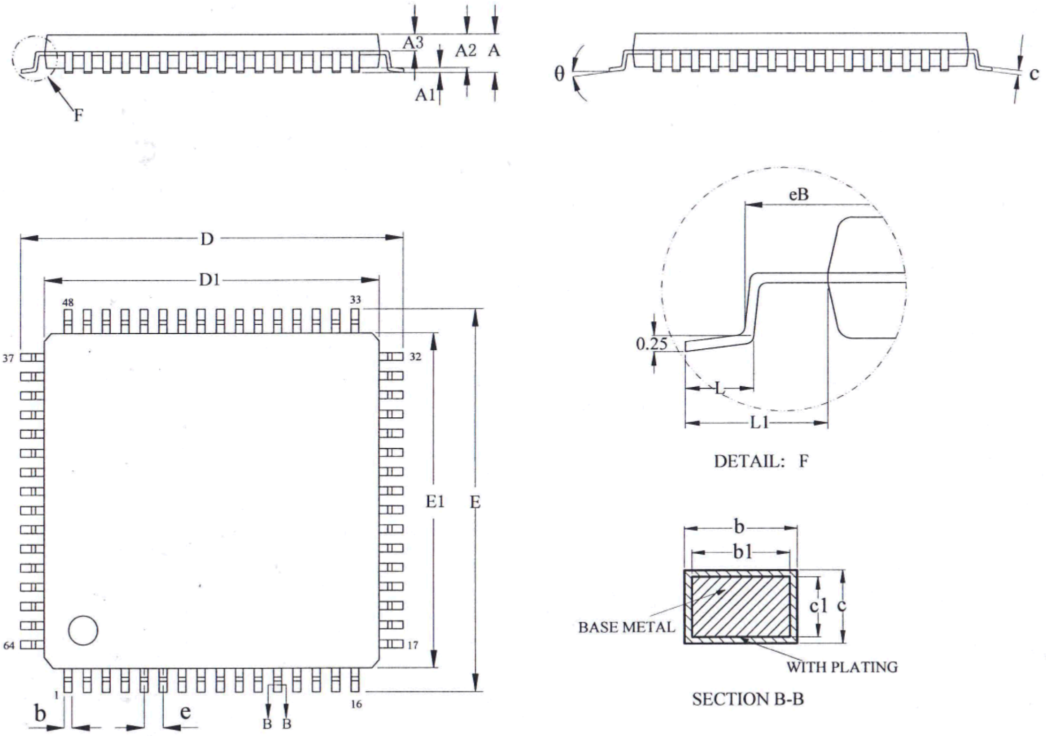
Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope	Average slope	3.5	4.05	4.5	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.438	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(2)(1)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

5. Package information

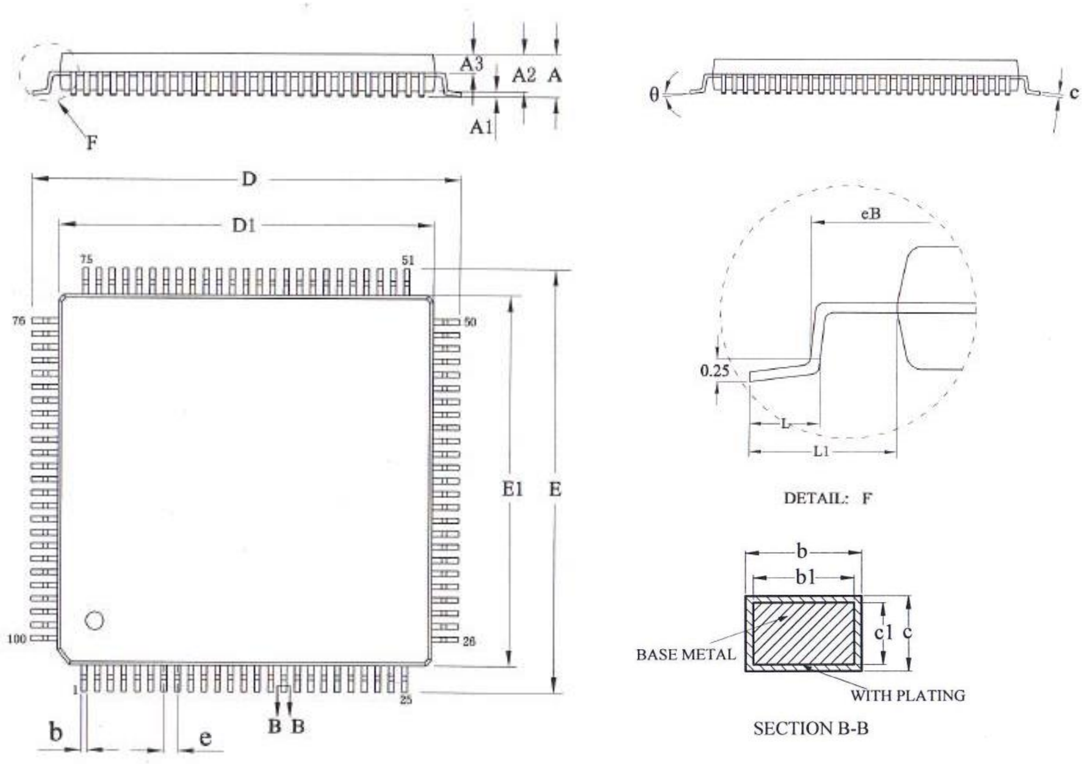
The device chip is available in LQFP64 and LQFP100 packages.

LQFP64



Symbol	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.063
A1	0.050	-	0.150	0.002	-	0.006
A2	1.350	1.400	1.450	0.053	0.055	0.057
A3	0.590	0.640	0.690	0.023	0.025	0.027
b	0.180	-	0.260	0.007	-	0.010
b1	0.170	0.200	0.230	0.007	0.008	0.009
c	0.130	-	0.170	0.005	-	0.007
c1	0.120	0.130	0.140	0.005	0.005	0.006
D	11.800	12.000	12.200	0.465	0.472	0.480
D1	9.900	10.000	10.100	0.390	0.394	0.398
E	11.800	12.000	12.200	0.465	0.472	0.480
E1	9.900	10.000	10.100	0.390	0.394	0.398
eB	11.050	-	11.250	0.435	-	0.443
e	0.500BSC			0.020BSC		
L	0.450	-	0.750	0.018	-	0.030
L1	1.000REF			0.039REF		
θ	0°	-	7°	0°	-	7°

LQFP100



Symbol	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.063
A1	0.050	-	0.150	0.002	-	0.006
A2	1.350	1.400	1.450	0.053	0.055	0.057
A3	0.590	0.640	0.690	0.023	0.025	0.027
b	0.180	-	0.260	0.007	-	0.010
b1	0.170	0.200	0.230	0.007	0.008	0.009
c	0.130	-	0.170	0.005	-	0.007
c1	0.120	0.130	0.140	0.005	0.005	0.006
D	15.800	16.000	16.200	0.622	0.630	0.638
D1	13.900	14.000	14.100	0.547	0.551	0.555
E	15.800	16.000	16.200	0.622	0.630	0.638
E1	13.900	14.000	14.100	0.547	0.551	0.555
eB	15.050	-	15.350	0.593	-	0.604
e		0.500BSC			0.020BSC	
L	0.450	-	0.750	0.018	-	0.030
L1		1.000REF			0.039REF	
θ	0°	-	7°	0°	-	7°

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