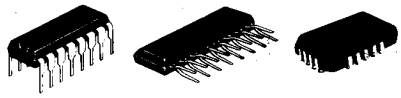


M5M4257AP,J,L-85,-10,-12,-15

NIBBLE MODE 262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the 18-pin plastic leaded chip carrier configuration and an increase in system densitites. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

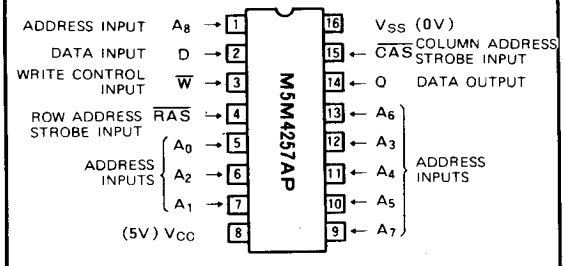
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4257AP, J, L-85	85	160	300
M5M4257AP, J, L-10	100	190	260
M5M4257AP, J, L-12	120	220	230
M5M4257AP, J, L-15	150	260	200

- Standard 16 pin DIP, 18 pin PLCC, 16 pin ZIP
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4257AP, J, L-85 . . . . . 385mW (max)
  - M5M4257AP, J, L-10 . . . . . 360mW (max)
  - M5M4257AP, J, L-12 . . . . . 330mW (max)
  - M5M4257AP, J, L-15 . . . . . 305mW (max)
- Unlatched output enables two-dimensional chip selection
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Nibble-mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms
- $\overline{CAS}$ controlled output allows hidden refresh

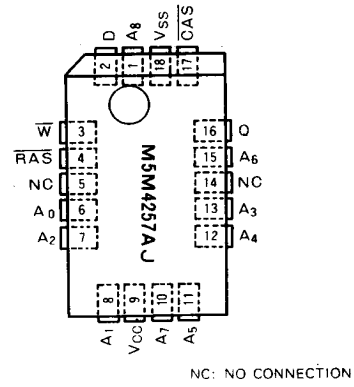
APPLICATION

Main memory unit for computers, Microcomputer memory

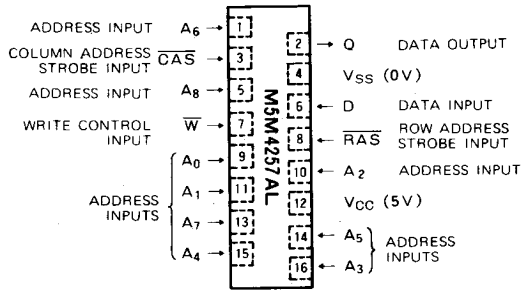
PIN CONFIGURATION (TOP VIEW)



Outline 16P4H(DIP)



Outline 18P0A (PLCC)



Outline 16P5A (ZIP)

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FUNCTION

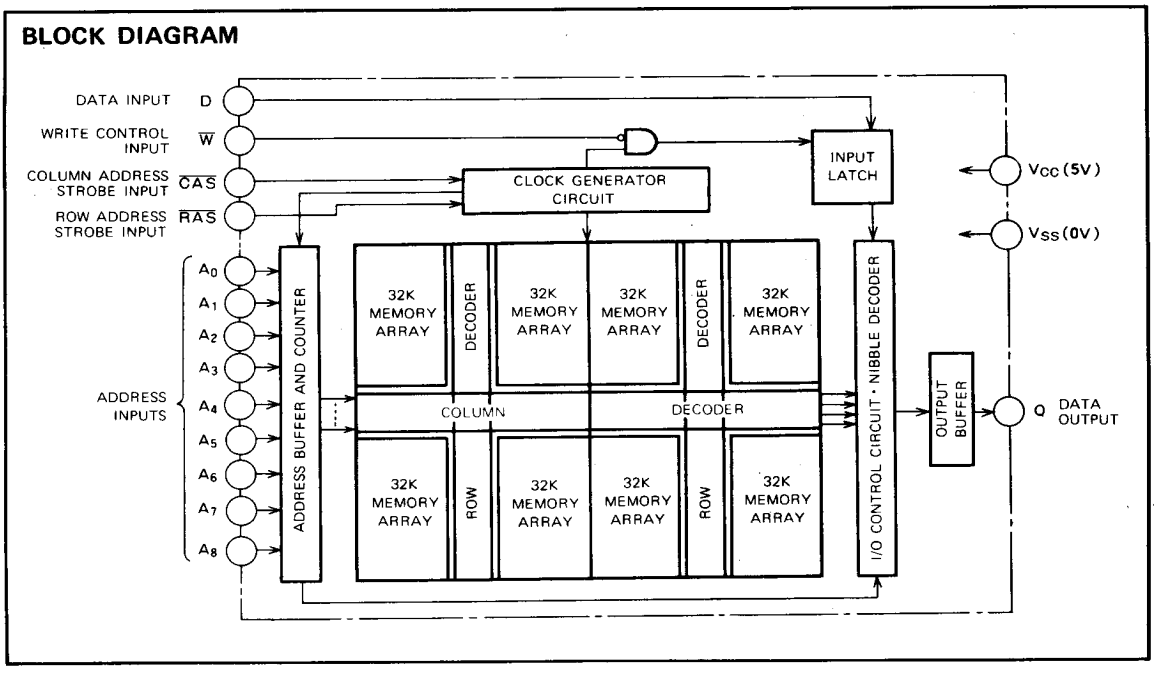
The M5M4257AP, J, L provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode. $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q	
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.

BLOCK DIAGRAM



NIBBLE MODE 262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta＝25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}＝−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}＝4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦V_{CC}, Other input pins＝0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M4257AP, J, L-85	$\overline{RAS}$, $\overline{CAS}$ cycling t_{CR}＝t_{CW}＝min, output open			70	mA
		M5M4257AP, J, L-10				65	
		M5M4257AP, J, L-12				60	
		M5M4257AP, J, L-15				55	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$＝$\overline{CAS}$＝V_{IH}			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M4257AP, J, L-85	$\overline{RAS}$ cycling $\overline{CAS}$＝V_{IH} $t_{C(RAS)}$＝min, output open			60	mA
		M5M4257AP, J, L-10				55	
		M5M4257AP, J, L-12				50	
		M5M4257AP, J, L-15				45	
$I_{CC5(AV)}$	Average supply current from V_{CC}, nibble mode (Note 3, 4)	M5M4257AP, J, L-85	$\overline{RAS}$＝V_{IL}, $\overline{CAS}$ cycling t_{CN}＝min, output open			35	mA
		M5M4257AP, J, L-10				30	
		M5M4257AP, J, L-12				25	
		M5M4257AP, J, L-15				20	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4257AP, J, L-85	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(RAS)}$＝min, Output open			65	mA
		M5M4257AP, J, L-10				60	
		M5M4257AP, J, L-12				55	
		M5M4257AP, J, L-15				50	
$C_{I(A)}$	Input capacitance, address inputs		V_I＝V_{SS} f＝1MHz V_I＝25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
C_O	Output capacitance		V_O＝V_{SS}, f＝1MHz, V_I＝25mVrms			7	pF

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC5(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

NIBBLE MODE 262144-BIT (262144-WORD BY 1-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits								Unit
			M5M4257A-85		M5M4257A-10		M5M4257A-12		M5M4257A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		4		4		4		4	ms
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width	t_{RP}	65		80		90		100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	85	10000	100	10000	120	10000	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	45	10000	50	10000	60	10000	75	10000	ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width (Note 8)	t_{CPN}	20		20		25		25		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$	t_{CSH}	85		100		120		150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$	t_{RSH}	45		50		60		75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$ (Note 9)	t_{CRP}	10		10		10		10		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 10)	t_{RCD}	15	40	15	50	20	60	25	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$	t_{ASR}	0		0		0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$	t_{ASC}	−5		−5		−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$	t_{RAH}	10		10		15		20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$	t_{CAH}	15		15		20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$	t_{AR}	55		65		80		100		ns
t_{THL}	Transition time	t_T	3	50	3	50	3	50	3	50	ns
t_{TLH}			3	50	3	50	3	50	3	50	ns

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min}$ and $V_{IL\ max}$. Reference levels for transition time are also between V_{IH} and V_{IL}.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)\ min} = t_{h(RAS-RA)\ min} + 2t_{THL(tTLH)} + t_{su(CA-CAS)\ min}$.

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits								Unit
			M5M4257A-85		M5M4257A-10		M5M4257A-12		M5M4257A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	160		190		220		260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$	t_{RCS}	0		0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$ (Note 11)	t_{RCH}	0		0		0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$ (Note 11)	t_{RRH}	10		10		10		10		ns
$t_{dis(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	20	0	25	0	25	0	35	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time (Note 13)	t_{CAC}		45		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time (Note 14)	t_{RAC}		85		100		120		150	ns

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12: $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.
13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max. Test conditions; Load = 2TTL, C_L = 100pF.
14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$ max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2TTL, C_L = 100pF.

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits								Unit
			M5M4257A-85		M5M4257A-10		M5M4257A-12		M5M4257A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	160		190		220		260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$ (Note 17)	t_{WCS}	−10		−10		−10		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$	t_{WCH}	15		20		25		30		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$	t_{WCR}	55		70		85		105		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write	t_{RWL}	30		35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write	t_{CWL}	30		35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	15		20		25		30		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$	t_{DS}	0		0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$	t_{DH}	15		20		25		30		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$	t_{DHR}	55		70		85		105		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Alternative Symbol	Limits								Unit
				M5M4257A-85		M5M4257A-10		M5M4257A-12		M5M4257A-15		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{CRW}	Read-write cycle time	(Note 15)	t_{RWC}	185		220		255		295		ns
t_{CRMW}	Read-modify-write cycle time	(Note 16)	t_{RMWC}	195		235		265		310		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write		t_{RWL}	30		35		40		45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write		t_{CWL}	30		35		40		45		ns
$t_{w(W)}$	Write pulse width		t_{WP}	15		20		25		30		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$		t_{RCS}	0		0		0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write	(Note 17)	t_{RWD}	70		90		110		135		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write	(Note 17)	t_{CWD}	30		40		50		60		ns
$t_{su(D-W)}$	Data-in setup time before write		t_{DS}	0		0		0		0		ns
$t_{h(W-D)}$	Data-in hold time after write		t_{DH}	15		20		25		30		ns
$t_{dis(CAS)}$	Output disable time		t_{OFF}	0	20	0	25	0	30	0	35	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time	(Note 13)	t_{CAC}		45		50		60		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time	(Note 14)	t_{RAC}		85		100		120		150	ns

Note 15: t_{CRW} min is defined as t_{CRW} min = $t_{d(RAS-W)}$ max + $t_{d(CAS-W)}$ min + $t_{h(W-RAS)}$ + $t_{w(RASH)}$ + $3t_{TLH}(t_{THL})$.

16: t_{CRMW} min is defined as t_{CRMW} min = $t_{a(RAS)}$ max + $t_{h(W-RAS)}$ + $t_{w(RASH)}$ + $3t_{TLH}(t_{THL})$.

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$ min and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above (delayed write), the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

Nibble Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits								Unit
			M5M4257A-85		M5M4257A-10		M5M4257A-12		M5M4257A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CN}	Nibble mode cycle time	t_{NC}	45		50		55		70		ns
$t_{aN(CAS)}$	Nibble mode access time	t_{NAC}		20		25		30		40	ns
$t_{wN(CASL)}$	Nibble mode $\overline{CAS}$ low pulse width	t_{NCAS}	20		25		30		40		ns
$t_{wN(CASH)}$	Nibble mode precharge time	t_{NP}	15		15		15		20		ns
$t_{hN(CAS-RAS)}$	Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	20		25		30		40		ns
$t_{dN(CAS-W)}$	Nibble mode $\overline{CAS}$ to WRITE delay	t_{NCWD}	20		25		30		40		ns
$t_{wNRMW(CASL)}$	Nibble mode RMW $\overline{CAS}$ pulse width	t_{NCRW}	45		55		65		85		ns
$t_{hNRMW(W-CAS)}$	Nibble mode $\overline{WRITE}$ to $\overline{CAS}$ lead time	t_{NCWL}	20		25		30		40		ns
$t_{hNRMW(CAS-RAS)}$	Nibble mode RMW $\overline{RAS}$ hold time	t_{NWSH}	45		55		65		85		ns
$t_{suN(W-CAS)}$	Nibble mode $\overline{WRITE}$ setup time before $\overline{CAS}$	t_{NWCS}	0		0		0		0		ns

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

Symbol	Parameter	Alternative Symbol	Limits								Unit
			M5M4257A-85		M5M4257A-10		M5M4257A-12		M5M4257A-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{suR(CAS-RAS)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	10		10		10		10		ns
$t_{hR(RAS-CAS)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	15		20		25		30		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		0		ns

Note 18: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

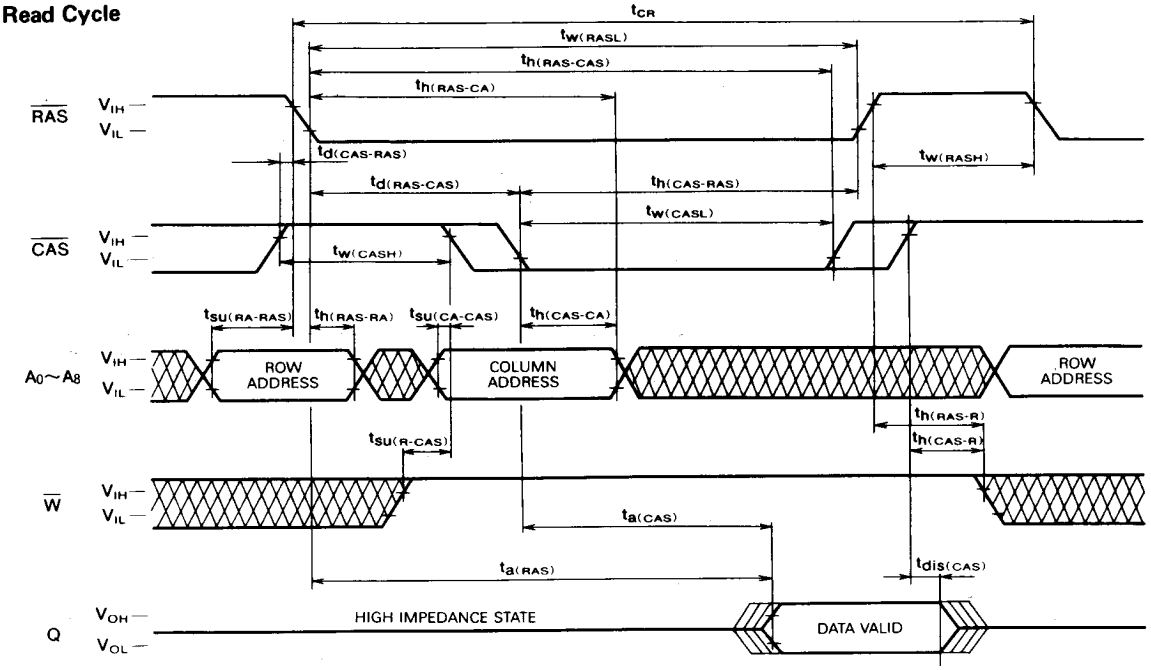
Nibble Mode Addressing Sequence Example

Sequence	Nibble bit	Column address									Row address									
		A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	
$\overline{RAS}/\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	External address
toggle $\overline{CAS}$	2	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	1	Internally generated address
toggle $\overline{CAS}$	3	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	
toggle $\overline{CAS}$	4	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	1	
toggle $\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	

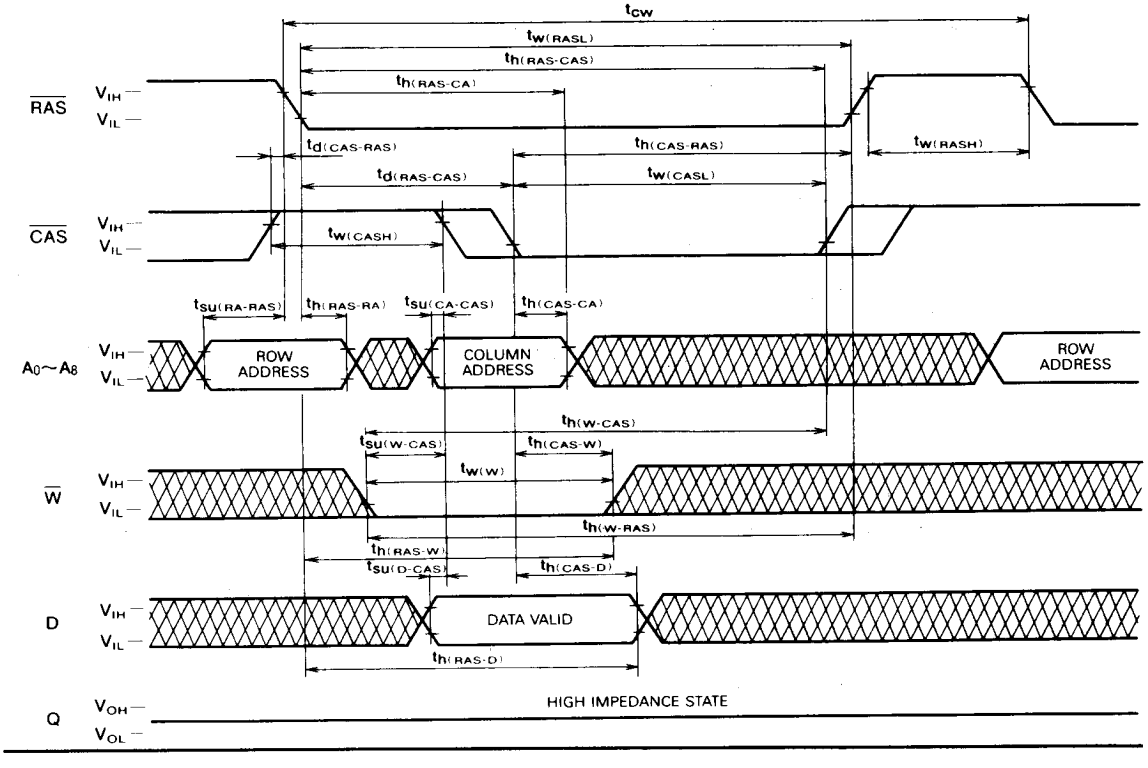
MITSUBISHI ELECTRIC

TIMING DIAGRAMS (Note 19)

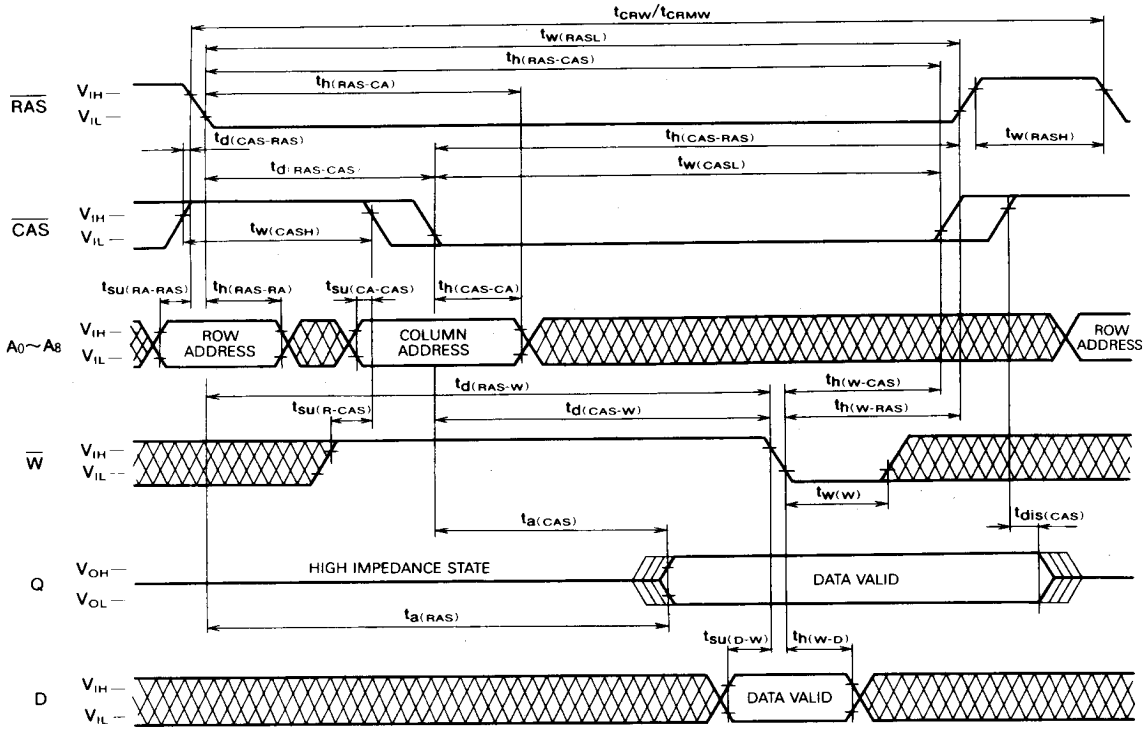
Read Cycle



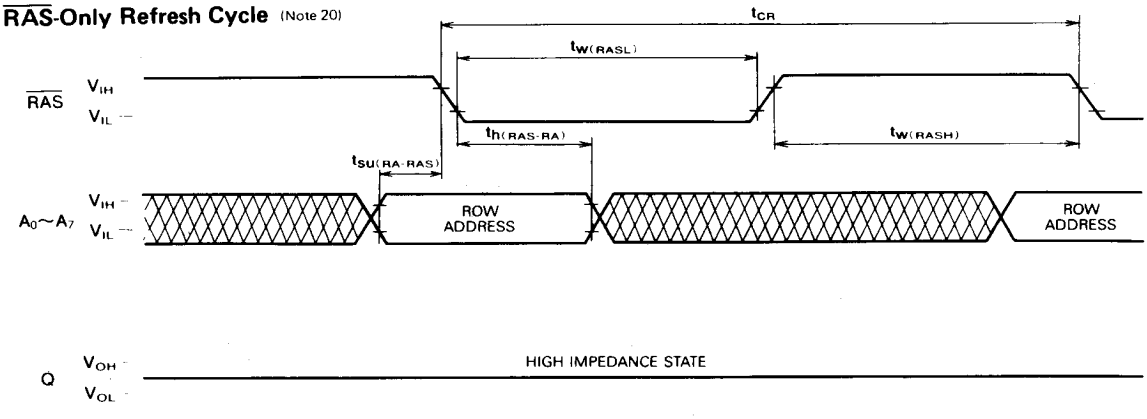
Write Cycle (Early Write)



Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 20)



Note 19. Indicates the don't care input.

The center-line indicates the high-impedance state.

Note 20. $\overline{CAS} = V_{IH}$, $\overline{W}$, D = don't care.
A8 may be V_{IH} or V_{IL}.

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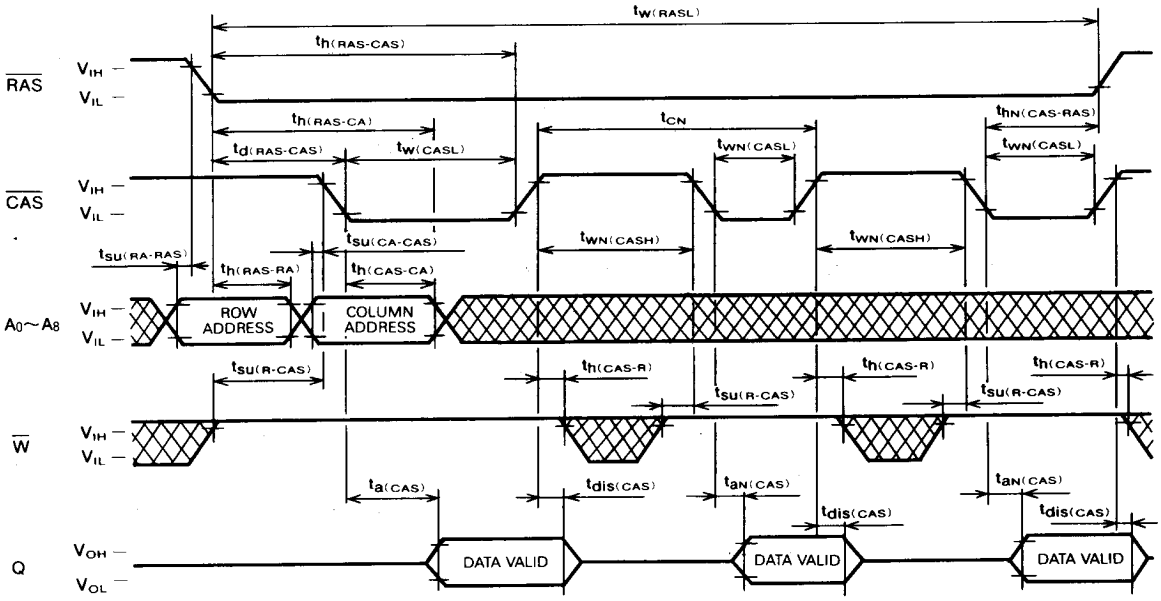
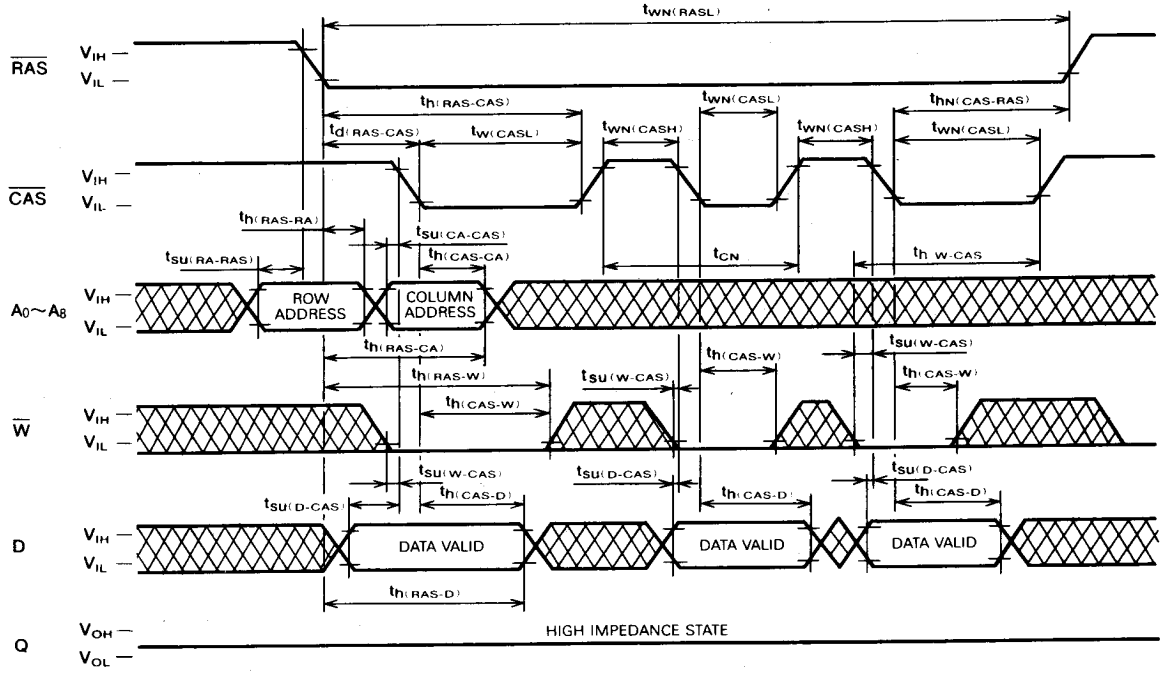
Nibble Mode Read Cycle (Note 21)

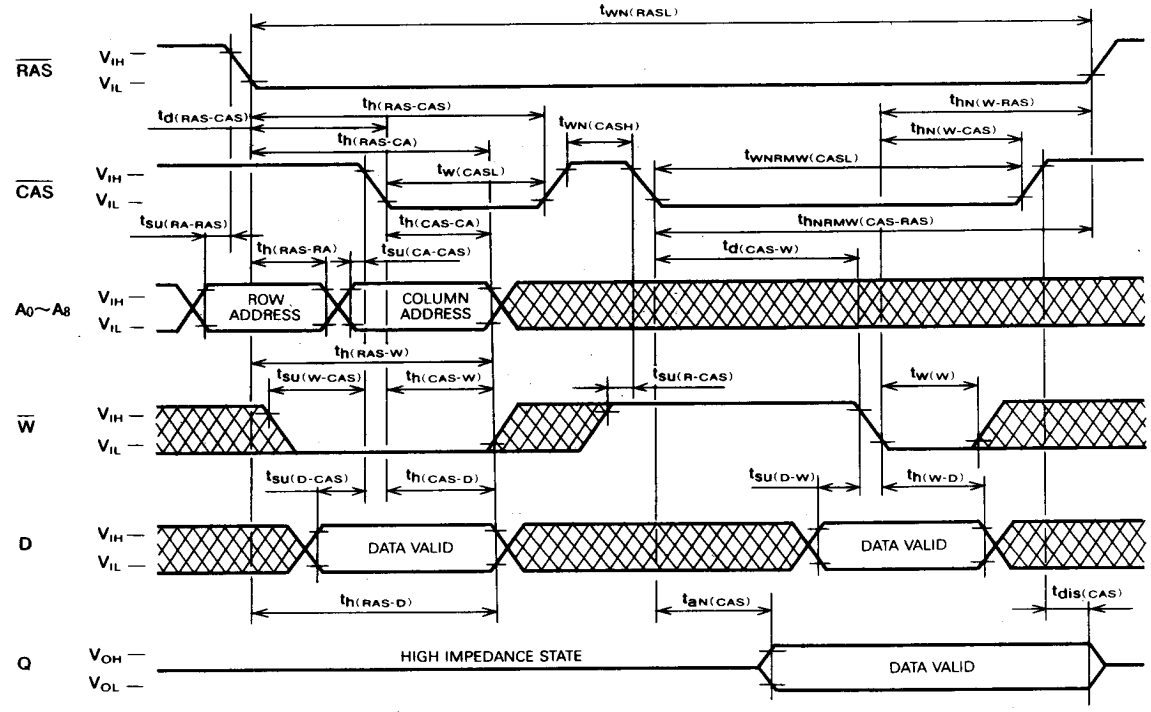


Note 21: Pin 1 at Row Time and Column Time Determines the Starting Address of the Nibble Cycle.

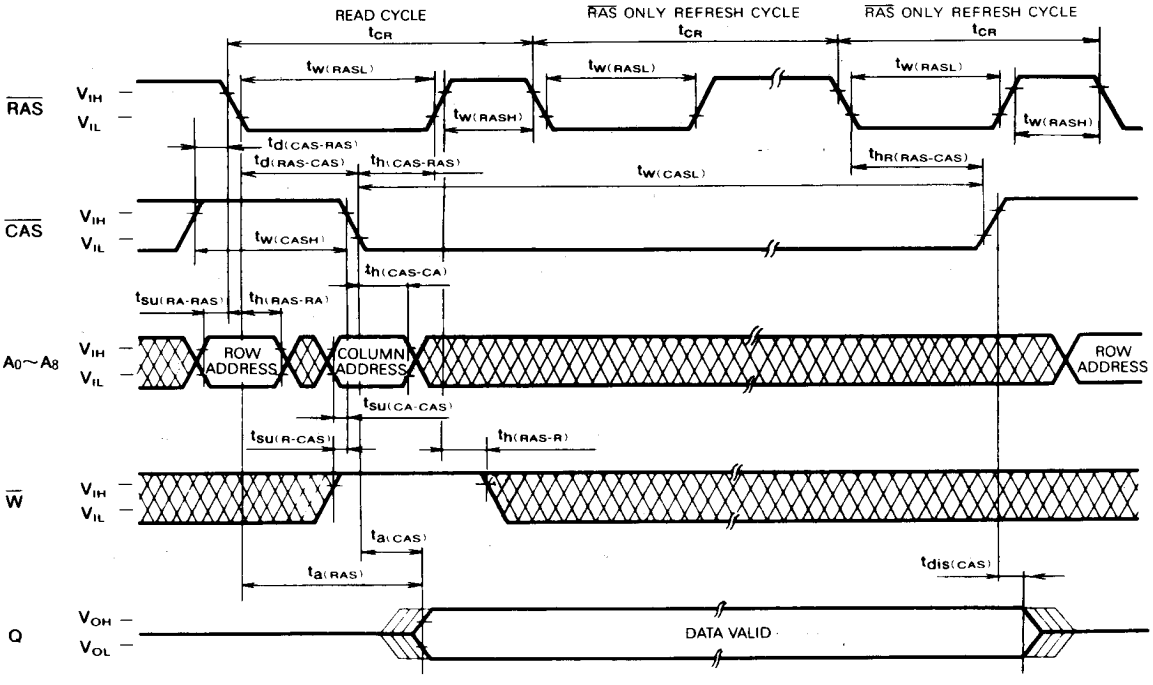
Nibble Mode Write Cycle (Early Write)



Nibble Mode Read-Modify-Write Cycle



Hidden Refresh Cycle



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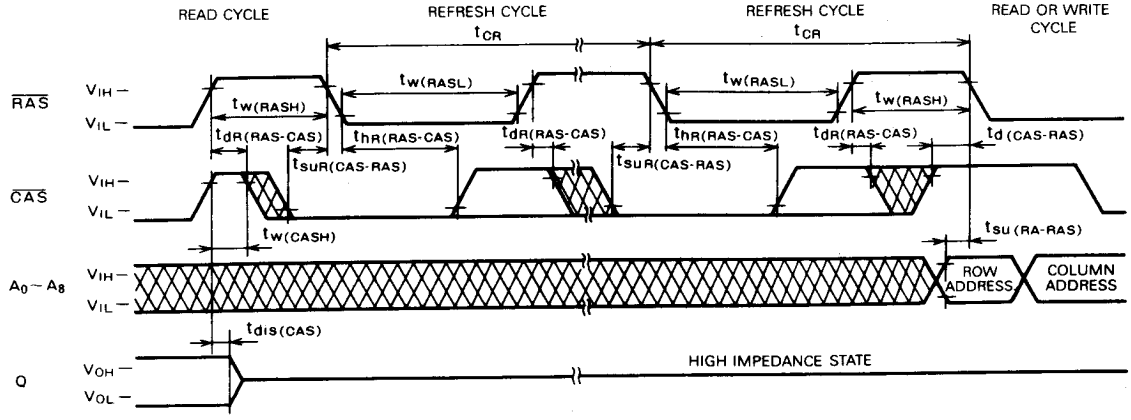
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 22)



Note 22. $\overline{W}$, D = don't care.