IC Memory

Dynamic RAM

■ Low Voltage Operation 64M Dynamic RAM

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
16M ∞ 4	μPD4264400	50 60 70	8K/64*	100 90 80	0.5	3.3±0.3	• 32-pin SOJ (400 mil) • 32-pin TSOP II (400 mil)	Fast page
	μPD4265400	50 60 70	4K/64	130 110 100				
8M ∞ 8	μPD4264800	50 60 70	8K/64*	105 95 85				–
	μPD4265800	50 60 70	4K/64	135 115 105				
4M ∞ 16	μPD4264160	50 60 70	8K/64*	110 100 90			• 50-pin TSOP II (400 mil)	Fast page + Byte read/write
	μPD4265160	50 60 70	4K/64	140 120 110				

* CBR/Hidden Refresh: 4K/64

■ Low Voltage Operation 64M Dynamic RAM with Self Refresh

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current				Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Self refresh (μA)	Long refresh (μA)			
16M ∞ 4	μPD42S64400★	50 60 70	8K/128*	100 90 80	0.2	300	300	3.3±0.3	• 32-pin SOJ (400 mil) • 32-pin TSOP II (400 mil)	Fast page
	μPD42S65400★	50 60 70	4K/128	130 110 100						
8M ∞ 8	μPD42S64800★	50 60 70	8K/128*	105 95 85						
	μPD42S65800★	50 60 70	4K/128	135 115 105						
4M ∞ 16	μPD42S64160★	50 60 70	8K/128*	110 100 90					• 50-pin TSOP II (400 mil)	
	μPD42S65160★	50 60 70	4K/128	140 120 110						

* CBR/Hidden Refresh: 4K/128

★: Under development

Dynamic RAM

■ 16M Dynamic RAM

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
4M ∞ 4	**μPD4216400**	50 60 70 80	4K/64	100 90 80 70	1	5±10 %	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)	Fast page
	μPD4217400	50 60 70 80	2K/32	10 110 100 90				
2M ∞ 8	**μPD4216800**	50 60 70 80	4K/64	100 90 80 70			• 28-pin SOJ (400 mil) • 28-pin TSOP II (400 mil)	
	μPD4217800	50 60 70 80	2K/32	120 110 100 90				
1M ∞ 16	**μPD4216160**	60 70 80	4K/64	100 90 80			• 42-pin SOJ (400 mil) • 50-pin TSOP II (400 mil)	Fast page + Byte read/write
	μPD4218160	60 70 80	1K/16	160 150 140				

■ 16M Dynamic RAM with Self Refresh

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current				Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Self refresh (μA)	Long refresh (μA)			
4M ∞ 4	**μPD42S16400**	50 60 70 80	4K/128	100 90 80 70	0.25	250	450	5±10 %	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)	Fast page
	μPD42S17400	50 60 70 80	2K/128	120 110 100 90			400			
2M ∞ 8	**μPD42S16800**	50 60 70 80	4K/128	100 90 80 70			450		• 28-pin SOJ (400 mil) • 28-pin TSOP II (400 mil)	
	μPD42S17800	50 60 70 80	2K/128	120 110 100 90			400			
1M ∞ 16	**μPD42S16160**	60 70 80	4K/128	100 90 80			450		• 42-pin SOJ (400 mil) • 50-pin TSOP II (400 mil)	Fast page + Byte read/write
	μPD42S18160	60 70 80	1K/128	160 150 140			350			

Dynamic RAM

■ Low Voltage Operation 16M Dynamic RAM

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
4M ∞ 4	**μPD4216400L**	60 70 80	4K/64	80 70 60	0.5	3.3±0.3	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)	Fast page
	μPD4217400L	60 70 80	2K/32	100 90 80				
2M ∞ 8	**μPD4216800L**	60 70 80	4K/64	80 70 60			• 28-pin SOJ (400 mil) • 28-pin TSOP II (400 mil)	–
	μPD4217800L	60 70 80	2K/32	100 90 80				
1M ∞ 16	**μPD4216160L**	60 70 80	4K/64	90 80 70			• 42-pin SOJ (400 mil) • 50-pin TSOP II (400 mil)	Fast page + Byte read/write
	μPD4218160L	60 70 80	1K/16	150 140 130				

■ Low Voltage Operation 16M Dynamic RAM with Self Refresh

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current				Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Self refresh (μA)	Long refresh (μA)			
4M ∞ 4	**μPD42S16400L**	60 70 80	4K/128	80 70 60	0.15	150	220	3.3±0.3	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)	Fast page
	μPD42S17400L	60 70 80	2K/128	100 90 80			200			
2M ∞ 8	**μPD42S16800L**	60 70 80	4K/128	80 70 60			220		• 28-pin SOJ (400 mil) • 28-pin TSOP II (400 mil)	
	μPD42S17800L	60 70 80	2K/128	100 90 80			200			
1M ∞ 16	**μPD42S16160L**	60 70 80	4K/128	90 80 70			220		• 42-pin SOJ (400 mil) • 50-pin TSOP II (400 mil)	Fast page + Byte read/write
	μPD42S18160L	60 70 80	1K/128	150 140 130			180			

Dynamic RAM

■ 16M Dynamic RAM (Hyper Page Mode*)

Organization (words × bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
4M × 4	**μPD4216405**	50 60 70 80	4K/64	100 90 80 70	1	5±10 %	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)	Hyper page
	μPD4217401	50 60 70 80	2K/32	10 110 100 90				
2M × 8	**μPD4217801**	50 60 70 80	2K/32	120 110 100 90			• 28-pin SOJ (400 mil) • 28-pin TSOP II (400 mil)	
1M × 16	**μPD4216161**	60 70 80	4K/64	100 90 80			• 42-pin SOJ (400 mil) • 50-pin TSOP II (400 mil)	Hyper page + Byte read/write
	μPD4218161	60 70 80	1K/16	160 150 140				

*: Hyper Page Mode is equivalent to EDO

■ 16M Dynamic RAM with Self Refresh (Hyper Page Mode*)

Organization (words × bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current				Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Self refresh (μA)	Long refresh (μA)			
4M × 4	**μPD42S16405**	50 60 70 80	4K/128	100 90 80 70	0.25	250	450	5±10 %	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)	Hyper page
	μPD42S17401	50 60 70 80	2K/128	120 110 100 90			400			
2M × 8	**μPD42S17801**	50 60 70 80	2K/128	120 110 100 90			400		• 28-pin SOJ (400 mil) • 28-pin TSOP II (400 mil)	
1M × 16	**μPD42S16161**	60 70 80	4K/128	100 90 80			450		• 42-pin SOJ (400 mil) • 50-pin TSOP II (400 mil)	Hyper page + Byte read/write
	μPD42S18161	60 70 80	1K/128	160 150 140			350			

*: Hyper Page Mode is equivalent to EDO

Dynamic RAM

■ Low Voltage Operation 16M Dynamic RAM (Hyper Page Mode*)

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
4M ∞ 4	**μPD42164005L**	60 70 80	4K/64	80 70 60	0.5	3.3±0.3	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)	Hyper page
	μPD4217401L	60 70 80	2K/32	100 90 80				
2M ∞ 8	**μPD4217801L**	60 70 80	2K/32	100 90 80			• 28-pin SOJ (400 mil) • 28-pin TSOP II (400 mil)	–
1M ∞ 16	**μPD4216161L**	60 70 80	4K/64	90 80 70			• 42-pin SOJ (400 mil) • 50-pin TSOP II (400 mil)	Hyper page + Byte read/write
	μPD4218161L	60 70 80	1K/16	150 140 130				

*: Hyper Page Mode is equivalent to EDO

■ Low Voltage Operation 16M Dynamic RAM with Self Refresh (Hyper Page Mode*)

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current				Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Self refresh (μA)	Long refresh (μA)			
4M ∞ 4	**μPD42S16401L**	60 70 80	4K/128	80 70 60	0.15	150	220	3.3±0.3	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)	Hyper page
	μPD42S17401L	60 70 80	2K/128	100 90 80			200			
2M ∞ 8	**μPD42S17801L**	60 70 80	2K/128	100 90 80			200		• 28-pin SOJ (400 mil) • 28-pin TSOP II (400 mil)	
1M ∞ 16	**μPD42S16161L**	60 70 80	4K/128	90 80 70			220		• 42-pin SOJ (400 mil) • 50-pin TSOP II (400 mil)	Hyper page + Byte read/write
	μPD42S18161L	60 70 80	1K/128	150 140 130			180			

*: Hyper Page Mode is equivalent to EDO

Dynamic RAM

■ 4M Dynamic RAM

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (ms)	Standby (mA)	Long refresh (μA)			
1M ∞ 4	**μPD424400**	60 70	1K/16	120 100	1	–	5±10 %	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)	Fast page
	μPD424400-L	60 70	1K/128	120 100	0.2	300			
512K ∞ 8	**μPD424800**	60 70 80	1K/16	105 105 95	1	–		• 28-pin SOJ (400 mil) • 28-pin TSOP II (400 mil)	
256K ∞ 16	**μPD424260**	60 70 80	512/8	160 160 145				• 40-pin SOJ (400 mil) • 44-pin TSOP II (400 mil)	Fast page Byte read/write

■ 4M Dynamic RAM with Self Refresh

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current				Supply voltage (V)	Package	Remarks
				Active (ms)	Standby (mA)	Self refresh (μA)	Long refresh (μA)			
1M ∞ 4	**μPD42S4400**	60 70	1K/128	120 100	0.15	150	200	5±10 %	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)	Fast page
512K ∞ 8	**μPD42S4800**	60 70 80	1K/128	105 105 95					• 28-pin SOJ (400 mil) • 28-pin TSOP II (400 mil)	
256K ∞ 16	**μPD42S4260**	60 70 80	512/128	160 160 145					• 40-pin SOJ (400 mil) • 44-pin TSOP II (400 mil)	Fast page Byte read/write

■ Low Voltage Operation 4M Dynamic RAM

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (ms)	Standby (mA)			
256K ∞ 16	**μPD424260AL**	60 70 80	512/8	80 70 60	0.5	3.3±0.3	• 40-pin SOJ (400 mil) • 44-pin TSOP II (400 mil)	Fast page Byte read/write

■ Low Voltage Operation 4M Dynamic RAM with Self Refresh

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current				Supply voltage (V)	Package	Remarks
				Active (ms)	Standby (mA)	Self refresh (μA)	Long refresh (μA)			
256K ∞ 16	**μPD42S4260AL**	60 70 80	512/128	80 70 60	0.08	80	100	3.3±0.3	• 40-pin SOJ (400 mil) • 44-pin TSOP II (400 mil)	Fast page Byte read/write

Dynamic RAM

■ 4M Dynamic RAM (Hyper Page Mode*)

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (ms)	Standby (mA)	Long refresh (μA)			
256K ∞ 16	**μPD424210**	60-G 70	512/8	160 150	1	–	5±10 %	• 40-pin SOJ (400 mil) • 44-pin TSOP II (400 mil)	Hyper page Byte read/write

*: Hyper Page Mode is equivalent to EDO

■ 4M Dynamic RAM with Self Refresh (Hyper Page Mode*)

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current				Supply voltage (V)	Package	Remarks
				Active (ms)	Standby (mA)	Self refresh (μA)	Long refresh (μA)			
256K ∞ 16	**μPD42S4210**	60-G 70	512/128	160 150	0.15	150	200	5±10 %	• 40-pin SOJ (400 mil) • 44-pin TSOP II (400 mil)	Hyper page Byte read/write

*: Hyper Page Mode is equivalent to EDO

■ Low Voltage Operation 4M Dynamic RAM (Hyper Page Mode*)

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (ms)	Standby (mA)			
256K ∞ 16	**μPD424210AL**	60 70 80	512/8	80 70 60	0.5	3.3±0.3	• 40-pin SOJ (400 mil) • 44-pin TSOP II (400 mil)	Hyper page Byte read/write

*: Hyper Page Mode is equivalent to EDO

■ Low Voltage Operation 4M Dynamic RAM with Self Refresh (Hyper Page Mode*)

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current				Supply voltage (V)	Package	Remarks
				Active (ms)	Standby (mA)	Self refresh (μA)	Long refresh (μA)			
256K ∞ 16	**μPD42S4210AL**	60 70 80	512/128	80 70 60	0.08	80	100	3.3±0.3	• 40-pin SOJ (400 mil) • 44-pin TSOP II (400 mil)	Hyper page Byte read/write

*: Hyper Page Mode is equivalent to EDO

Dynamic RAM

■ Synchronous DRAM

Organization (words ∞ bits)	Part number	Cycle time MIN. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current			Inter-face	Supply voltage (V)	Package
				Active Normal/Burst (Grade-10, C.L.=3) (mA)	Standby (Power down Mode) (mA)	Self refresh (mA)			
4M ∞ 4	μPD4516421	10 (100 MHz) 12 (83 MHz) 13 (75 MHz) 15 (66 MHz)	2K/32	80 mA/150 mA (MAX.)	2	2	LVTTL	3.3±0.3	• 44-pin TSOP II (400 mil)
2M ∞ 8	μPD4516821			85 mA/165 mA (MAX.)					
1M ∞ 16	μPD4516161			90 mA/210 mA (MAX.)					• 50-pin TSOP II (400 mil)

C.L. = CAS Latency

■ Rambus™ DRAM (under development)

Organization (words ∞ bits)	Part number		Operating frequency (MHz)	Supply voltage (V)	Maximum supply current (mA)	Package
2M ∞ 9	μPD488170L	–A50	250	3.3 ±0.15	250	• 32-pin SVP • 72/36-pin SSOP
		–A40	200			
2M ∞ 8	μPD488130L	–A50	250			
		–A40	200			

Dynamic RAM Module

■ SIMM

Capacity (byte)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
32M	8M × 36	**MC-428000A36**	60 70 80	1420 1260 1140	24	5±10 %	• 72-pin SIMM socket type (solder-coated/gold-plated)	Fast page
	8M × 32	**MC-428000A32**	60 70 80	860 780	16			
		MC-428000F32	60 70	940 860	16			Hyper page (EDO)
16M	4M × 36	**MC-424000A36**	60 70 80	1360 1200 1080	12		• 72-pin SIMM socket type socket type (solder-coated/gold-plated)	Fast page
	4M × 32	**MC-424000A32**	60 70 80	880 800 720	8			
		MC-424000F32	60 70	880 800	8			Hyper page (EDO)
8M	2M × 36	**MC-422000A36**	60 70 80 100	1300 1180 1060 940	24			Fast page
	2M × 32	**MC-422000A32**	60 70 80	324 304 284	4			Fast page 16M DRAM Base
		MC-422000F32	60 70	324 304	4			Hyper page (EDO)
4M	1M × 36	**MC-421000A36**	60 70 80 100	1240 1120 1000 880	12		• 72-pin SIMM socket type socket type (solder-coated/gold-plated)	Fast page
	1M × 32	**MC-421000A32**	60 70 80	320 300 280	2			Fast page 16M DRAM Base
		MC-421000F32	60 70	320 300	2			Hyper page (EDO)

■ SOD (SOD: Small Outline DIMM, DIMM: Dual Inline Memory Module)

Organization (words × bits)	Bank	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current			Supply voltage (V)	Package	Mounted devices	Remarks
					Active (mA)	Standby (mA)	Self refresh (μA)				
1M × 32	1	**MC-42S1000LAD32S**	60 70 80	1K/128	300 280 260	1	360	3.3±0.3	• 72-pin SOD Socket type (Gold plated)	D42S18160LG5 × 2 pcs.	Fast page Self refresh
2M × 32	1	**MC-42S2000LAB32S**	60 70 80	2K/128	400 360 320	2	600			D42S17800LG5 × 4 pcs.	
	2	**MC-42S2000LAD32S**	60 70 80	1K/128	301 281 261		720			D42S18160LG5 × 4 pcs.	
4M × 32	1	**MC-42S4000LAC32S**	60 70 80	2K/128	800 720 640	4	1200			D42S17400LG3 × 8 pcs.	
	2	**MC-42S4000LAB32S**	60 70 80		405 365 325		1200			D42S17800LG5 × 8 pcs.	

Dynamic RAM Module

■ 8 Byte DIMM (DIMM: Dual Inline Memory Module)

Organization (words ∞ bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
1M ∞ 64	**MC-421000AA64**	60 70 80	1K/16	650 610 570	68	5.0±0.25	• 168-pin DIMM Socket type (Gold plated)	Fast page
	MC-421000FA64	60 70		650 610				Hyper page (EDO)
2M ∞ 64	**MC-422000AA64**	60 70 80		660 620 580	72			Fast page
	MC-422000FA64	60 70		660 620				Hyper page (EDO)
1M ∞ 72 (ECC)	**MC-421000AD72**	60 70 80		890 810 750	70			Fast page
2M ∞ 72 (ECC)	**MC-422000AB72**	60 70 80	2K/32	1000 910 820	73			
	MC-422000FB72	60 70		1000 910				Hyper page (EDO)
	MC-422000LAB72	60 70 80		910 820 730	14	3.3±0.3		Fast page
	MC-422000LFB72	60 70		910 820				Hyper page (EDO)
4M ∞ 72 (ECC)	**MC-424000AB72**	60 70 80		1990 1810 1630	82	5.0±0.25		Fast page
	MC-424000AC72	60 70 80	4K/64	1630 1480 1270				
	MC-424000FB72★	60 70	2K/32	1990 1810				Hyper page (EDO)
	MC-424000FC72	60 70	4K/64	1630 1450				
	MC-424000LAB72	60 70 80	2K/32	1810 1630 1450	19	3.3±0.3		Fast page
	MC-424000LAC72	70 80	4K/64	1270 1090				Hyper page (EDO)
	MC-424000LFB72★	60 70	2K/32	1810 1630				
	MC-424000LFC72	60 70	4K/64	1450 1270				

★: Under development

Dynamic RAM Module

■ Synchronous DRAM DIMM

Organization (words ∞ bits)	Part number	Mnimum cycle time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
2M ∞ 72	**MC-452AA72**	10 12 13	2K/32	765 720 675	18	3.3±0.3	• 200-pin DIMM Socket type (Gold plated)	Unbuffered
	MC-452BA72	10 12 13		TBD	TBD			Buffered
2M ∞ 80	**MC-452AA80**	10 12 13		850 800 750	20			Unbuffered
	MC-454BA80	10 12 13		TBD	TBD			Buffered
4M ∞ 72	**MC-454BA/BC72**	10 12 13						
4M ∞ 80	**MC-454BA/BC80**	10 12 13						

Static RAM

■ Low Power Static RAM

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Data retention (μA)			
256K	32K × 8	**μPD43256B**	70	45	0.1	50	5±10 %	• 28-pin DIP (600 mil)	L version
		with $\overline{CS}$, $\overline{OE}$	85	45	0.05	20		• 28-pin SOP (450 mil)	LL version
								• 32-pin TSOP I (600 mil)	
								• 28-pin TSOP I (8 × 13.4 mm)	
		μPD43257B	70	45	0.1	50		• 28-pin DIP (600 mil)	L version
		with $\overline{CE1}$, CE2	85	45	0.05	20		• 28-pin SOP (450 mil)	LL version
1M	128K × 8	**μPD431000A**	70	70	0.1	50		• 32-pin DIP (600 mil)	L version
		with $\overline{CE1}$, CE2,	85		0.05	20		• 32-pin SOP (525 mil)	LL version
		$\overline{OE}$	100					• 32-pin TSOP I (8 × 20 mm)	

■ Low Power Static RAM Low Voltage (2.7 to 5.5 V) Operation

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package
				Active (mA)	Standby (μA)	Data retention (μA)		
256K	32K × 8	**μPD43256B-B12**	120	20	25	20	3±10 %	• 28-pin SOP (450 mil)
				45	50		3.3 < V_{CC} < 4.5	• 32-pin TSOP I (600 mil)
		with $\overline{CS}$, $\overline{OE}$	85				5±10 %	• 28-pin TSOP I (8 × 13.4 mm)
1M	128K × 8	**μPD431000A-B15**	150	20	25	20	3±10 %	• 32-pin SOP (525 mil)
				70	50		3.3 < V_{CC} < 4.5	• 32-pin TSOP I (8 × 20 mm)
		with $\overline{CE1}$, CE2,	100				5±10 %	
		$\overline{OE}$						

■ Low Power Static RAM Low Voltage (3.0 to 5.5 V) Operation

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package
				Active (mA)	Standby (mA)	Data retention (μA)		
256K	32K × 8	**μPD43256B-A10**	100	45	50	20	3.3 ± 0.3 V	• 28-pin SOP (450 mil)
			85				5±10 %	• 32-pin TSOP I (600 mil)
		μPD43256B-A12	120				3.3 ± 0.3 V	• 28-pin TSOP I (8 × 13.4 mm)
			85				5±10 %	

Static RAM

■ Fast Static RAM

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Data retention (μA)			
1M	128K × 8	**μPD431008**	15 17 20	160 150 140	10	–	5±10 %	• 32-pin SOJ (400 mil)	–
	128K × 9	**μPD431009**	15 17 20	160 150 140				• 36-pin SOJ (400 mil)	
	64K × 16	**μPD431016**	15 17 20	240 230 220				• 44-pin SOJ (400 mil)	
	64K × 18	**μPD431018**	15 17 20	240 230 220					
4M	1M × 4	**μPD434004**	20 25	150 140				• 32-pin SOJ (400 mil)	
	512K × 8	**μPD434008**	20 25	190 170				• 36-pin SOJ (400 mil)	

■ Fast Static RAM Low Voltage (3.0 to 3.6 V) Operation

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package
				Active (mA)	Standby (mA)	Data retention (μA)		
1M	128K × 8	**μPD431008L**	17 20	120 100	5	–	3.3±0.3	• 32-pin SOJ (400 mil)
	128K × 9	**μPD431009L**						• 36-pin SOJ (400 mil)
	64K × 16	**μPD431016L**						• 44-pin SOJ (400 mil)
	64K × 18	**μPD431018L**						

■ Synchronous Static RAM

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Data retention (μA)			
1M	32K × 32	**μPD431232L**	8 9 12	250	2	–	3.3±0.2	• 100-pin TQFP	–

Static RAM

■ BiCMOS Fast Static RAM

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Data retention (μA)			
256K	32K × 8	**μPD46258**	6 7	–	–	–	5±10 %	• 32-pin SOJ (300 mil)	–
1M	128K × 8	**μPD461008**	8 9 10	185				• 32-pin SOJ (400 mil)	

■ BiCMOS Fast Static RAM (3.3 V ± 0.3 V)

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Data retention (μA)			
256K	32K × 8	**μPD46259L**	12	130	20	–	3.3±0.3	• 32-pin SOJ (300 mil)	–
1M	64K × 16	**μPD461016L**	10 12	260	70		$3.3^{+0.3}_{-0.15}$	• 44-pin SOJ (400 mil)	
							3.3±0.3		
	64K × 18	**μPD461018L**	10 12	260			$3.3^{+0.3}_{-0.15}$	• 44-pin TSOP II (400 mil)	
							3.3±0.3		

■ BiCMOS Synchronous Static RAM

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Data retention (μA)			
1M	32K × 18	**μPD461318**★	2 2.5 3 7 8.5 10	TBD	TBD	–	3.3±0.3	• 119-pin BGA	User-option ① Dual-CLK R/L ② Single-CLK R/R
	32K × 36	**μPD461336**★	2 2.5 3 7 8.5 10						

★: Under development

Mask ROM

■ Mask ROM

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
32M	2M × 16 or 1M × 32 (selectable)	μPD23C32140★	100/30	120	0.1	5 ±10 %	• 70-pin SSOP (500 mil) • 70-pin TSOP II (400 mil)	with page access read mode
	4M × 8 or 2M × 16 (selectable)	μPD23C32000	120	70			• 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm)★ • 44-pin TSOP II (400 mil)★	–
16M	2M × 8 or 1M × 16 (selectable)	μPD23C16000W μPD23C16040A	120 120/35	70 100			• 42-pin DIP (600 mil) • 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm) • 44-pin TSOP II (400 mil)	μPD16040A ··· with page access read mode
8M	1M × 8 or 512K × 16 (selectable)	μPD23C8000W	120	70				Pin-compatible with PROM μPD27C8000
	1M × 8	μPD23C8001EJ	120	50			• 32-pin DIP (600 mil) • 32-pin SOP (525 mil)	Pin-compatible with PROM μPD27C8001
4M	512K × 8 or 256K × 16 (selectable)	μPD23C4000S μPD23C4040	100 10/50	100 150			• 40-pin DIP (600 mil) • 40-pin SOP (525 mil)	Pin-compatible with PROM μPD27C4000 μPD23C4040 ··· with page access read mode
	512K × 8	μPD23C4001EJ	120	50			• 32-pin DIP (600 mil) • 32-pin SOP (525 mil) • 40-pin TSOP I (10 × 20 mm)	Pin-compatible with PROM μPD27C4001
2M	256K × 8	μPD23C2001E	200	40				Pin-compatible with PROM μPD27C2001
1M	128K × 8	μPD23C1001EA	150	40				Pin-compatible with PROM μPD27C1001A
		μPD23C1000EB					• 32-pin DIP (600 mil)	Pin-compatible with PROM μPD27C1000A
		μPD23C1000B μPD23C1010B					• 28-pin DIP (600 mil)	–

★: Under development

■ Mask ROM (Low Voltage Operation)

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
32M★	4M × 8 or 2M × 16 (selectable)	μPD23C32000	200	20	20	3.0±0.3	• 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm) • 44-pin TSOP II (400 mil)	–
16M	2M × 8 or 1M × 16 (selectable)	μPD23C16000LW	200	20	20		• 42-pin DIP (600 mil) • 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm) • 44-pin TSOP II (400 mil)	
8M	1M × 8 or 512K × 16 (selectable)	μPD23C8000LW	230	30	30			

★: Under development

PROM

■ UV EPROM

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
8M	1M × 8 or 512K × 16 (selectable)	**μPD27C8000**	120 150 170	50	0.1	V_{PP} = 12.5±0.3 V_{CC} = 5 ±10 %	• 42-pin DIP (600 mil)	Pin-compatible with Mask ROM μPD23C8000 series
	1M × 8	**μPD27C8001**	120 150 170	30			• 32-pin DIP (600 mil)	Pin-compatible with Mask ROM μPD23C8001E series
4M	512K × 8 or 256K × 16 (selectable)	**μPD27C4000**	150 170 200	50			• 40-pin DIP (600 mil)	Pin-compatible with Mask ROM μPD23C4000 series
	256K × 16	**μPD27C240**	100 120 150					–
	512K × 8	**μPD27C4001**	120★ 150 170 200	30			• 32-pin DIP (600 mil)	Pin-compatible with Mask ROM μPD23C4001E series
		μPD27C040	100 120 150	50				
2M	256K × 8	**μPD27C020**	120 150	30				Pin-compatible with Mask ROM μPD23C2001E series
1M	128K × 8	**μPD27C010A**	100 120 150					Pin-compatible with Mask ROM μPD23C1001E series
	64K × 16	**μPD27C210A**	120 150	50			• 40-pin DIP (600 mil)	Pin-compatible with Mask ROM μPD23C1024E series

★: Under development

■ ONE TIME PROM

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
8M	1M × 8 or 512K × 16 (selectable)	**μPD27C8000**	150 170	50	0.1	V_{PP} = 12.5±0.3 V_{CC} = 5 ±10 %	• 42-pin DIP (600 mil) • 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm)	Pin-compatible with Mask ROM μPD23C8000 series
	1M × 8	**μPD27C8001**	150 170	30			• 32-pin DIP (600 mil) • 32-pin SOP (525 mil)	Pin-compatible with Mask ROM μPD23C8001E series
4M	512K × 8 or 256K × 16 (selectable)	**μPD27C4000**	150 170 200	50			• 40-pin DIP (600 mil) • 40-pin SOP (525 mil)	Pin-compatible with Mask ROM μPD23C4000 series
	512K × 8	**μPD27C4001**	120★ 150 170 200	30			• 32-pin DIP (600 mil) • 32-pin SOP (525 mil) • 40-pin TSOP I (10 × 20 mm)	Pin-compatible with Mask ROM μPD23C4001E series

★: Under development

PROM

■ EEPROM

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
256K	32K × 8	**μPD28C256**	200 250	50	0.1	5 ±10 %	• 28-pin DIP (600 mil)	–
64K	8K × 8	**μPD28C64A**	150 200				• 28-pin DIP (600 mil) • 28-pin SOP (450 mil) • 32-pin TSOP I (600 mil)	

■ SERIAL EEPROM

Capacity (bits)	Organization (words × bits)	Part number	Serial interface	Active current (mA)	Standby current (mA)	Supply voltage (V)	Package
2K	256 × 8	**μPD6252**	CE, CS, SCL, SDA (2-wire BUS)	1.5	0.02	5 V ±10 %	• 8-pin DIP (300 mil) • 8-pin SOP (300 mil)
1K	128 × 8	**μPD6253**					
4K	512 × 8	**μPD6254**					
2K	256 × 8	**μPD6272**	CE, CS, I^2C BUS				
1K	128 × 8	**μPD6273**					
4K	512 × 8	**μPD6274**					
2K	256 × 8	**μPD6255**	CS, SCL, SDA (2-wire BUS)	1.0	0.005	1.8 to 3.5 V	
4K	512 × 8	**μPD6257**	CS, SCK, SI, SO (3-wire BUS)	1.5	0.003	5 V ±10 %	
8K	1024 × 8	**μPD6258**					

Flash MEMORY

■ Flash MEMORY

Capacity (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
1M	128K × 8	**μPD28F001**	80 100 120	50	0.1	V_{PP} = 12±0.6 V_{CC} = 5 ±10 %	• 32-pin SOP (525 mil) • 32-pin TSOP I (8 × 20 mm) • 32-pin QFJ	–

Other

■ Dual-Port Graphic Buffer

Capacity (bits)	Organization (words × bits)	Part number	Random access time MAX. (ns)	Serial read cycle time (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
					Active (mA)	Standby (mA)			
4M	256K × 16	**μPD482444**	60 70 80	20 22 25	130 110 90	10	5±10 %	• 64-pin SSOP (525 mil)	2WE Byte Control Fast Page Flash/Block Write Split Buffer Stopping Column
		μPD482445	60 70 80	20 22 25	130 110 90			• 64-pin SSOP (525 mil) • 70-pin TSOP II (400 mil)	2WE Byte Control Hyper Page Flash/Block Write Split Buffer Stopping Column
		μPD482445L	70 80	22 25	110 90	7	3.3±0.3		
2M	256K × 8	**μPD482234**	60 70 80	20 22 25	155 195 190	10	5±10 %	• 40-pin SOJ • 44-pin TSOP II	Fast page Flash write Block write Split buffer
		μPD482235	60 70 80	20 22 25	155 195 190				Hyper page Flash write Block write Split buffer

■ Synchronous Graphics RAM

Capacity (bits)	Organization	Part number	Cycle time MIN. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current (mA)			Interface	Supply voltage (V)	Package	Function
					Active Normal/Burst (Grade–10, C.L=3)	Standby power down mode	Self refresh				
8M	128K × 2 banks × 32 bits	**μPD481850**	10 (100 MHz) 12 (83 MHz) 15 (66 MHz)	1024/16	105/365 90/310 85/285	3	2	LVTTL	3.3±0.3	• 100-pin QFP (14 × 20 mm)	Sychronous Interface Write-per-bit (Old Mask) 8 column Block Write

■ Graphic Memory

Capacity (bits)	Organization (words × bits)	Part number	Random access time MAX. (ns)	Page mode access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
					Active (mA)	Standby (mA)			
4M	256K × 16	**μPD481440**	70 80	35 40	180 165	2	5±10 %	• 40-pin SOJ (400 mil)	2WE Byte Control Flash write Block write

Other

■ Silicon File

Capacity (bits)	Organization (words ∞ bits)	Part number	Random access time MAX. (ns)	Page mode access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package
					Active (mA)	Self refresh (μA)		
16M	16M ∞ 1	**μPD426171**	60 70 80	40 45 50	100 90 80	Ta=0 to 55 °C: 30 (–L) Ta=0 to 55 °C: 50	3.3±0.3	• 26-pin SOJ (300 mil) • 26-pin TSOP II (300 mil)
	4M ∞ 4	**μPD426174**	60 70 80	40 45 50	100 90 80			
4M	4M ∞ 1	**μPD42641**	80	20	90	Ta=0-70°C: 240 Ta=0-60°C: 120 Ta=0-50°C: 60	5±10 %	• 26-pin SOJ • 26-pin TSOP II
	1M ∞ 4	**μPD42644**						
	4M ∞ 1	**μPD42641-L**				Ta=0-70°C: 120 Ta=0-60°C: 60 Ta=0-50°C: 30		
	1M ∞ 4	**μPD42644-L**						

■ Field/Line Buffer

Capacity (bits)	Organization (words ∞ bits)	Part number	Read/Write cycle time MIN. (ns)	Data hold period (ms)	Maximum supply current active (mA)	Supply voltage (V)	Package	Remarks
2M	256 ∞ 8	**μPD42280**	30/30 40/40 60/60	–	90 75 60	5±10 %	• 28-pin SOP • 28-pin ZIP	Field buffer FIFO structure
80K	10096 ∞ 8 5048 ∞ 16	**μPD485506**	25/25 27/27 35/35		140		• 44-pin TSOP II	FAX, PPC Line buffer FIFO structure
40K	5048 ∞ 8	**μPD485505**	25/25 27/27 35/35		90		• 24-pin SOP	
7K	910 ∞ 8	**μPD42101**	34/34 34/69 69/69	1	70 60 35		• 24-pin DIP • 24-pin SOP	NTSC Line buffer FIFO structure
9K	1135 ∞ 8	**μPD42102**	25/25 28/28 28/56 56/56		80 80 70 40			PAL Line buffer FIFO structure