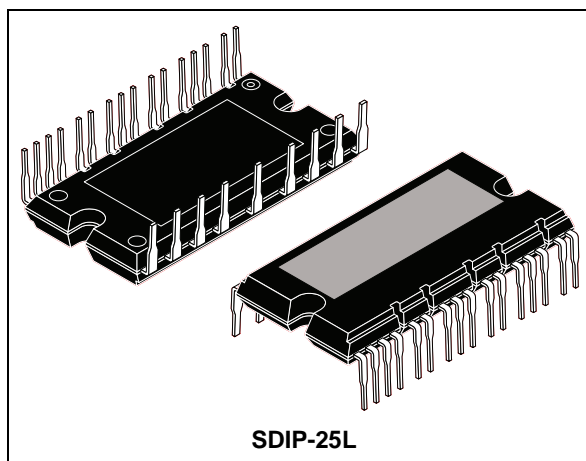


## SLLIMM™ small low-loss intelligent molded module IPM, 3-phase inverter, 14 A, 600 V short-circuit rugged IGBT

Datasheet - production data



### Features

- IPM 14 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- $V_{CE(sat)}$  negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull-down / pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Smart shutdown function
- Comparator for fault protection against overtemperature and overcurrent
- DBC substrate leading to low thermal resistance
- Isolation rating of 2500 V<sub>rms</sub>/min
- UL Recognized: UL1557 file E81734

### Applications

- 3-phase inverters for motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners and sewing machines

### Description

This intelligent power module provides a compact, high performance AC motor drive in a simple, rugged design. Combining ST proprietary control ICs with the most advanced short-circuit-rugged IGBT system technology, this device is ideal for 3-phase inverters in applications such as home appliances and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

**Table 1. Device summary**

Order code	Marking	Package	Packing
STGIPS14K60	GIPS14K60	SDIP-25L	Tube

# Contents

<b>1</b>	<b>Internal block diagram and pin configuration</b>	<b>3</b>
<b>2</b>	<b>Electrical ratings</b>	<b>5</b>
2.1	Absolute maximum ratings	5
2.2	Thermal data	6
<b>3</b>	<b>Electrical characteristics</b>	<b>7</b>
3.1	Control part	9
3.2	Waveform definitions	12
<b>4</b>	<b>Smart shutdown function</b>	<b>13</b>
<b>5</b>	<b>Applications information</b>	<b>15</b>
5.1	Recommendations	16
<b>6</b>	<b>Package information</b>	<b>17</b>
6.1	SDIP-25L package information	17
6.2	Packing information	19
<b>7</b>	<b>Revision history</b>	<b>20</b>

# 1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

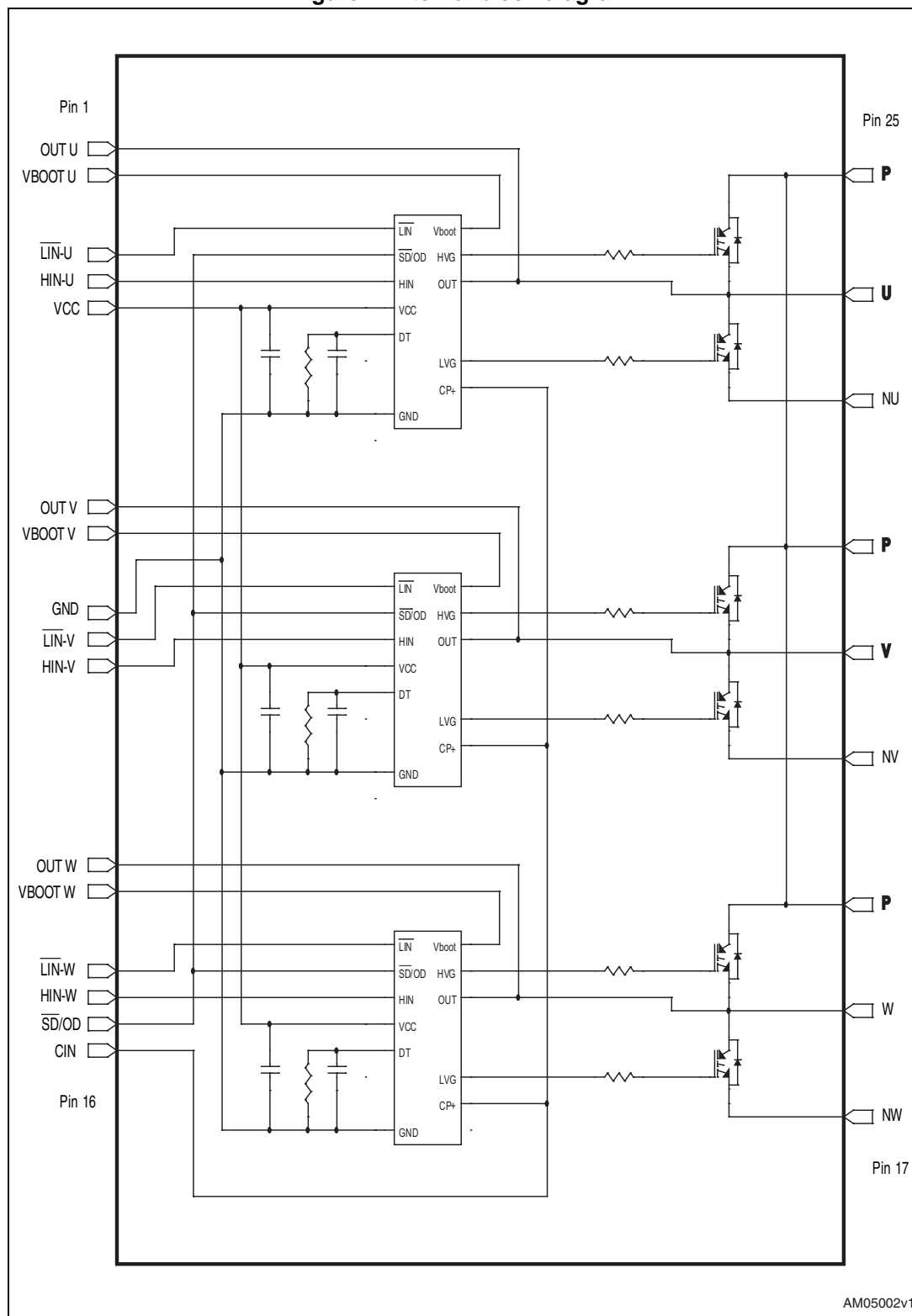
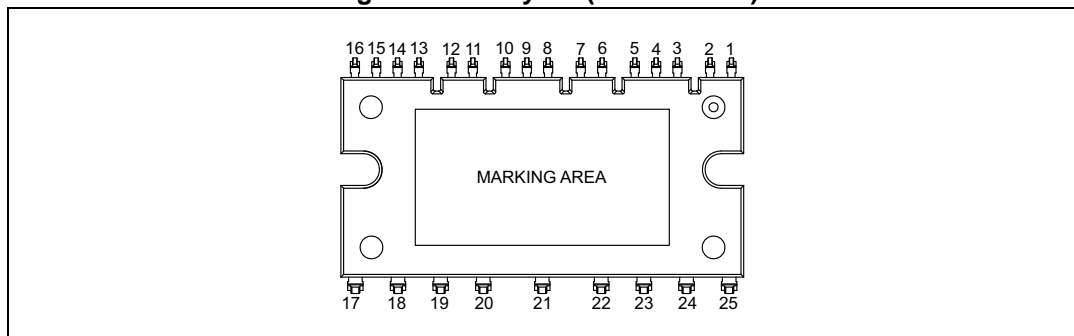


Table 2. Pin description

Pin n°	Symbol	Description
1	OUT <sub>U</sub>	High side reference output for U phase
2	V <sub>boot U</sub>	Bootstrap voltage for U phase
3	LIN <sub>U</sub>	Low side logic input for U phase
4	HIN <sub>U</sub>	High side logic input for U phase
5	V <sub>CC</sub>	Low voltage power supply
6	OUT <sub>V</sub>	High side reference output for V phase
7	V <sub>boot V</sub>	Bootstrap voltage for V phase
8	GND	Ground
9	LIN <sub>V</sub>	Low side logic input for V phase
10	HIN <sub>V</sub>	High side logic input for V phase
11	OUT <sub>W</sub>	High side reference output for W phase
12	V <sub>boot W</sub>	Bootstrap voltage for W phase
13	LIN <sub>W</sub>	Low side logic input for W phase
14	HIN <sub>W</sub>	High side logic input for W phase
15	$\overline{\text{SD}} / \text{OD}$	Shut down logic input (active low) / open drain (comparator output)
16	CIN	Comparator input
17	N <sub>W</sub>	Negative DC input for W phase
18	W	W phase output
19	P	Positive DC input
20	N <sub>V</sub>	Negative DC input for V phase
21	V	V phase output
22	P	Positive DC input
23	N <sub>U</sub>	Negative DC input for U phase
24	U	U phase output
25	P	Positive DC input

Figure 2. Pin layout (bottom view)



## 2 Electrical ratings

### 2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
$V_{PN}$	Supply voltage applied between P - $N_U$ , $N_V$ , $N_W$	450	V
$V_{PN(surge)}$	Supply voltage (surge) applied between P - $N_U$ , $N_V$ , $N_W$	500	V
$V_{CES}$	Each IGBT collector emitter voltage ( $V_{IN}^{(1)} = 0$ )	600	V
$\pm I_C^{(2)}$	Each IGBT continuous collector current at $T_C = 25^\circ\text{C}$	14	A
$\pm I_{CP}^{(3)}$	Each IGBT pulsed collector current	30	A
$P_{TOT}$	Each IGBT total dissipation at $T_C = 25^\circ\text{C}$	42	W
$t_{scw}$	Short circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_J = 125^\circ\text{C}$ , $V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN(1)} = 0 \div 5\text{ V}$	5	$\mu\text{s}$

1. Applied between  $HIN_i$ ,  $\overline{LIN}_i$  and  $G_{ND}$  for  $i = U, V, W$

2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature

Table 4. Control part

Symbol	Parameter	Min.	Max.	Unit
$V_{OUT}$	Output voltage applied between $OUT_U$ , $OUT_V$ , $OUT_W$ - GND	$V_{boot} - 21$	$V_{boot} + 0.3$	V
$V_{CC}$	Low voltage power supply	- 0.3	21	V
$V_{CIN}$	Comparator input voltage	- 0.3	$V_{CC} + 0.3$	V
$V_{boot}$	Bootstrap voltage	- 0.3	620	V
$V_{IN}$	Logic input voltage applied between $HIN$ , $\overline{LIN}$ and GND	- 0.3	15	V
$V_{SD/OD}$	Open drain voltage	- 0.3	15	V
$dV_{OUT}/dt$	Allowed output slew rate		50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
$V_{ISO}$	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ sec.}$ )	2500	V
$T_j$	Power chips operating junction temperature	- 40 to 150	$^\circ\text{C}$
$T_C$	Module case operation temperature	- 40 to 125	$^\circ\text{C}$

## 2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case single IGBT	3	°C/W
	Thermal resistance junction-case single diode	5.5	°C/W

### 3 Electrical characteristics

$T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

**Table 7. Inverter part**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0 \div 5\text{ V}$ , $I_C = 7\text{ A}$	-	2.1	2.5	V
		$V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0 \div 5\text{ V}$ , $I_C = 7\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$	-	1.8		
$I_{CES}$	Collector-cut off current ( $V_{IN}^{(1)} = 0$ "logic state")	$V_{CE} = 550\text{ V}$ , $V_{CC} = V_{Boot} = 15\text{ V}$	-		150	$\mu\text{A}$
$V_F$	Diode forward voltage	$V_{IN}^{(1)} = 0$ "logic state", $I_C = 7\text{ A}$	-		2.1	V
<b>Inductive load switching time and energy</b>						
$t_{on}$	Turn-on time	$V_{DD} = 300\text{ V}$ , $V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0 \div 5\text{ V}$ , $I_C = 7\text{ A}$ (see <a href="#">Figure 5</a> )	-	270		ns
$t_{c(on)}$	Crossover time (on)		-	130		
$t_{off}$	Turn-off time		-	520		
$t_{c(off)}$	Crossover time (off)		-	140		
$t_{rr}$	Reverse recovery time		-	130		
$E_{on}$	Turn-on switching losses		-	150		$\mu\text{J}$
$E_{off}$	Turn-off switching losses		-	110		

1. Applied between  $HIN_i$ ,  $\overline{LIN_i}$  and  $G_{ND}$  for  $i = U, V, W$  ( $\overline{LIN}$  inputs are active-low).

**Note:**  $t_{ON}$  and  $t_{OFF}$  include the propagation delay time of the internal drive.  $t_{C(ON)}$  and  $t_{C(OFF)}$  are the switching time of IGBT itself under the internally given gate driving condition.

The figure contains two timing diagrams, (a) and (b), illustrating the switching characteristics of a MOSFET.

**(a) turn-on:** This diagram shows the transition from a low state to a high state. The input voltage  $V_{IN}$  rises from a low level to a high level. The output voltage  $V_{CE}$  starts at a high level and falls as the MOSFET turns on. The collector current  $I_C$  starts at zero and rises to a peak value of  $100\% I_C$ . Key time intervals are marked:  $t_{ON}$  is the time from the start of the input rise to the point where  $V_{CE}$  has fallen to  $10\% V_{CE}$ ;  $t_{C(ON)}$  is the time from the point where  $V_{CE}$  is at  $10\% V_{CE}$  to the point where  $I_C$  has reached  $90\% I_C$ .

**(b) turn-off:** This diagram shows the transition from a high state to a low state. The input voltage  $V_{IN}$  falls from a high level to a low level. The output voltage  $V_{CE}$  starts at a low level and rises as the MOSFET turns off. The collector current  $I_C$  starts at a peak value of  $100\% I_C$  and falls to zero. Key time intervals are marked:  $t_{OFF}$  is the time from the start of the input fall to the point where  $V_{CE}$  has risen to  $10\% V_{CE}$ ;  $t_{C(OFF)}$  is the time from the point where  $V_{CE}$  is at  $10\% V_{CE}$  to the point where  $I_C$  has reached  $10\% I_C$ .





### 3.1 Control part

**Table 8. Low voltage power supply ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC\_hys}$	$V_{CC}$ UV hysteresis		1.2	1.5	1.8	V
$V_{CC\_thON}$	$V_{CC}$ UV turn ON threshold		11.5	12	12.5	V
$V_{CC\_thOFF}$	$V_{CC}$ UV turn OFF threshold		10	10.5	11	V
$I_{qccu}$	Undervoltage quiescent supply current	$V_{CC} = 10\text{ V}$ $\overline{SD}/OD = 5\text{ V}$ ; $\overline{LIN} = 5\text{ V}$ ; $H_{IN} = 0$ , $C_{IN} = 0$			450	$\mu\text{A}$
$I_{qcc}$	Quiescent current	$V_{CC} = 15\text{ V}$ $\overline{SD}/OD = 5\text{ V}$ ; $\overline{LIN} = 5\text{ V}$ $H_{IN} = 0$ , $C_{IN} = 0$			3.5	mA
$V_{ref}$	Internal comparator (CIN) reference voltage		0.5	0.54	0.58	V

**Table 9. Bootstrapped voltage ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BS\_hys}$	$V_{BS}$ UV hysteresis		1.2	1.5	1.8	V
$V_{BS\_thON}$	$V_{BS}$ UV turn ON threshold		11.1	11.5	12.1	V
$V_{BS\_thOFF}$	$V_{BS}$ UV turn OFF threshold		9.8	10	10.6	V
$I_{QBSU}$	Undervoltage $V_{BS}$ quiescent current	$V_{BS} < 9\text{ V}$ $\overline{SD}/OD = 5\text{ V}$ ; $\overline{LIN}$ and $H_{IN} = 5\text{ V}$ ; $C_{IN} = 0$		70	110	$\mu\text{A}$
$I_{QBS}$	$V_{BS}$ quiescent current	$V_{BS} = 15\text{ V}$ $\overline{SD}/OD = 5\text{ V}$ ; $\overline{LIN}$ and $H_{IN} = 5\text{ V}$ ; $C_{IN} = 0$		200	300	$\mu\text{A}$
$R_{DS(on)}$	Bootstrap driver on resistance	LVG ON		120		W

**Table 10. Logic inputs ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{il}$	Low logic level voltage		0.8		1.1	V
$V_{ih}$	High logic level voltage		1.9		2.25	V
$I_{HINh}$	HIN logic "1" input bias current	$H_{IN} = 15\text{ V}$	110	175	260	$\mu\text{A}$
$I_{HINI}$	HIN logic "0" input bias current	$H_{IN} = 0\text{ V}$			1	$\mu\text{A}$
$I_{LINI}$	$\overline{LIN}$ logic "1" input bias current	$\overline{LIN} = 0\text{ V}$	3	6	20	$\mu\text{A}$
$I_{LINh}$	$\overline{LIN}$ logic "0" input bias current	$\overline{LIN} = 15\text{ V}$			1	$\mu\text{A}$
$I_{SDh}$	$\overline{SD}$ logic "0" input bias current	$\overline{SD} = 15\text{ V}$	30	120	300	$\mu\text{A}$
$I_{SDl}$	$\overline{SD}$ logic "1" input bias current	$\overline{SD} = 0\text{ V}$			3	$\mu\text{A}$
Dt	Dead time	see <a href="#">Figure 7</a>		600		ns

Table 11. Sense comparator characteristics ( $V_{CC} = 15\text{ V}$  unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{ib}$	Input bias current	$V_{CIN} = 1\text{ V}$			3	$\mu\text{A}$
$V_{ol}$	Open drain low level output voltage	$I_{od} = 3\text{ mA}$			0.5	V
$t_{d\_comp}$	Comparator delay	$\overline{SD}/OD$ pulled to 5 V through 100 k $\Omega$ resistor		90	130	ns
SR	Slew rate	$C_L = 180\text{ pF}$ ; $R_{pu} = 5\text{ k}\Omega$		60		V/ $\mu\text{sec}$
$t_{sd}$	Shut down to high / low side driver propagation delay	$V_{OUT} = 0$ , $V_{boot} = V_{CC}$ , $V_{IN} = 0$ to 3.3 V	50	125	200	ns
$t_{isd}$	Comparator triggering to high / low side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin $CIN_i$	50	200	250	

Table 12. Truth table

Condition	Logic input ( $V_I$ )			Output	
	$\overline{SD}/OD$	$\overline{LIN}$	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X	X	L	L
Interlocking half-bridge tri-state	H	L	H	L	L
0 "logic state" half-bridge tri-state	H	H	L	L	L
1 "logic state" low side direct driving	H	L	L	H	L
1 "logic state" high side direct driving	H	H	H	L	H

Note: X: don't care

Figure 5. Maximum  $I_{C(RMS)}$  current vs. switching frequency <sup>(1)</sup>

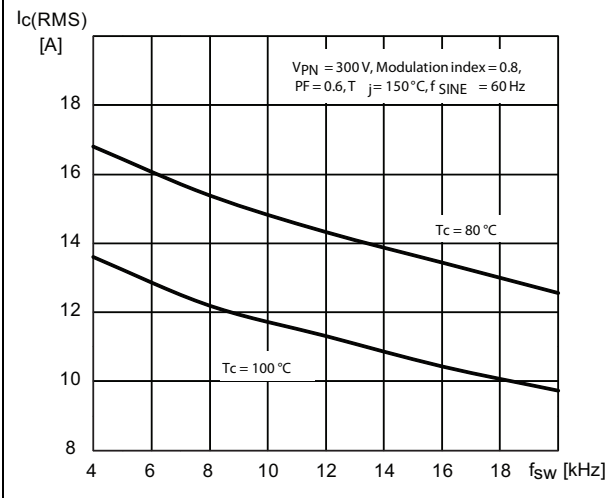
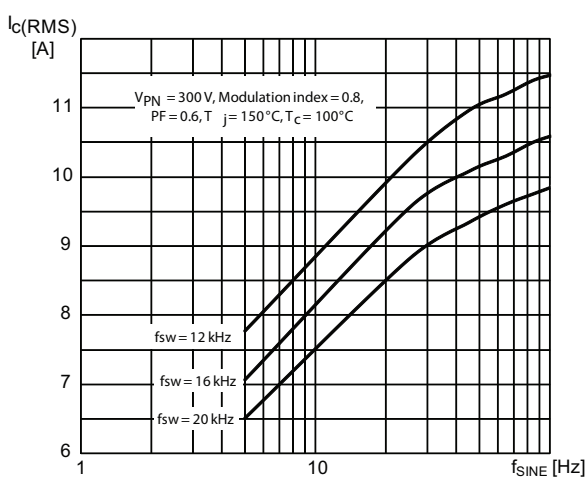


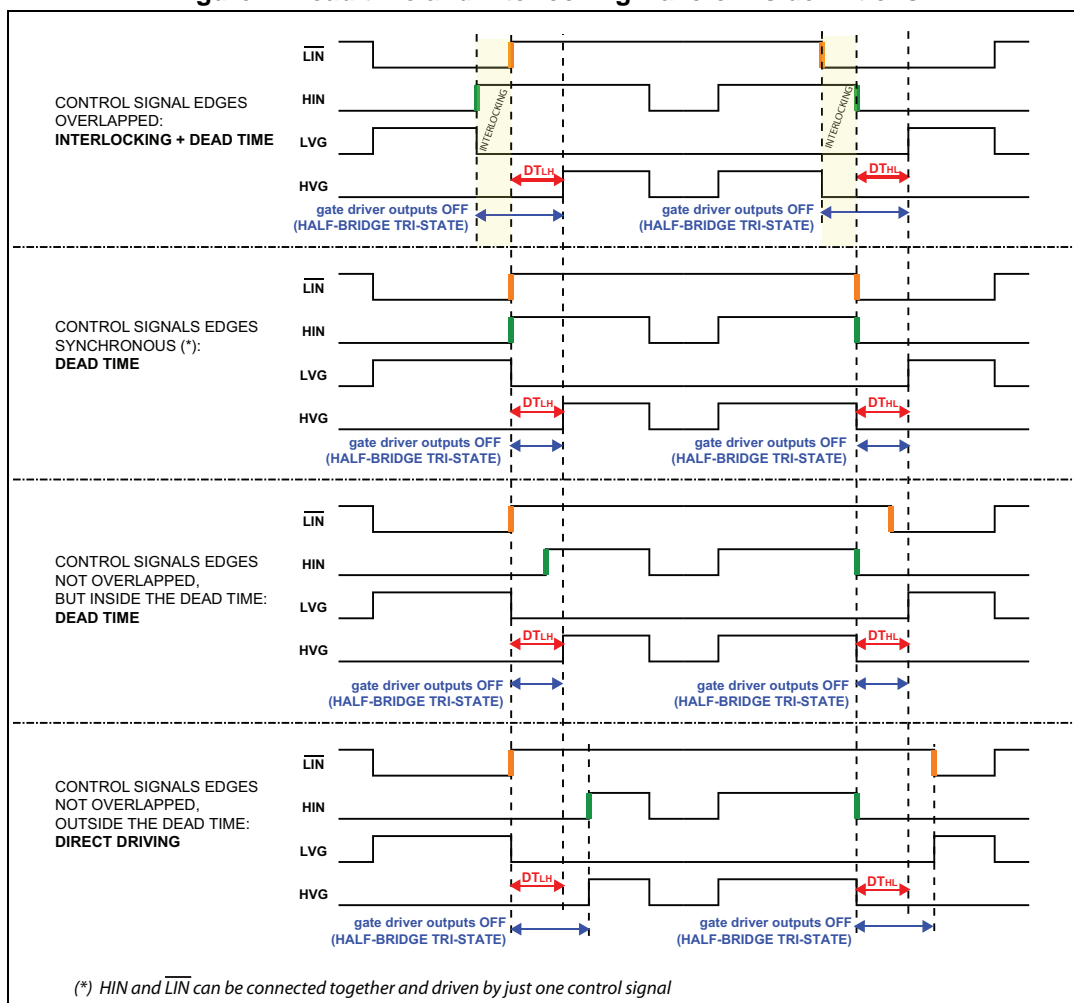
Figure 6. Maximum  $I_{C(RMS)}$  current vs.  $f_{SINE}$  <sup>(1)</sup>



1. Simulated curves refer to typical IGBT parameters and maximum  $R_{thj-c}$ .

## 3.2 Waveform definitions

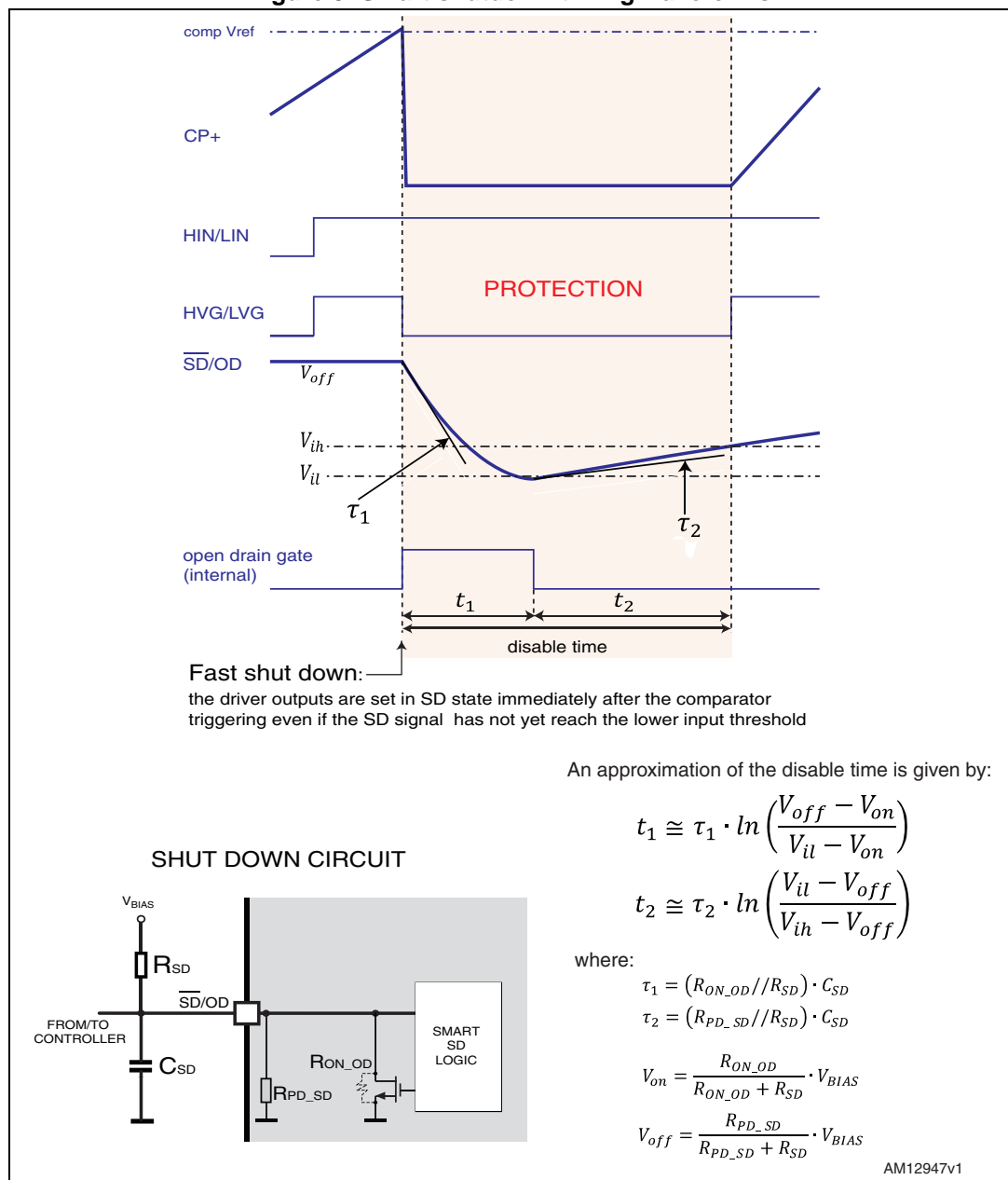
Figure 7. Dead time and interlocking waveforms definitions



## 4 Smart shutdown function

The STGIPS14K60 integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference  $V_{ref}$  connected to the inverting input, while the non-inverting input, available on pin (CIN), can be connected to an external shunt resistor in order to implement a simple over-current protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the halfbridge in tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the DMOS connected to the open-drain output (pin  $\overline{SD/OD}$ ) is turned on by the internal logic which holds it on until the shutdown voltage is lower than the logic input lower threshold ( $V_{il}$ ). Finally the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.

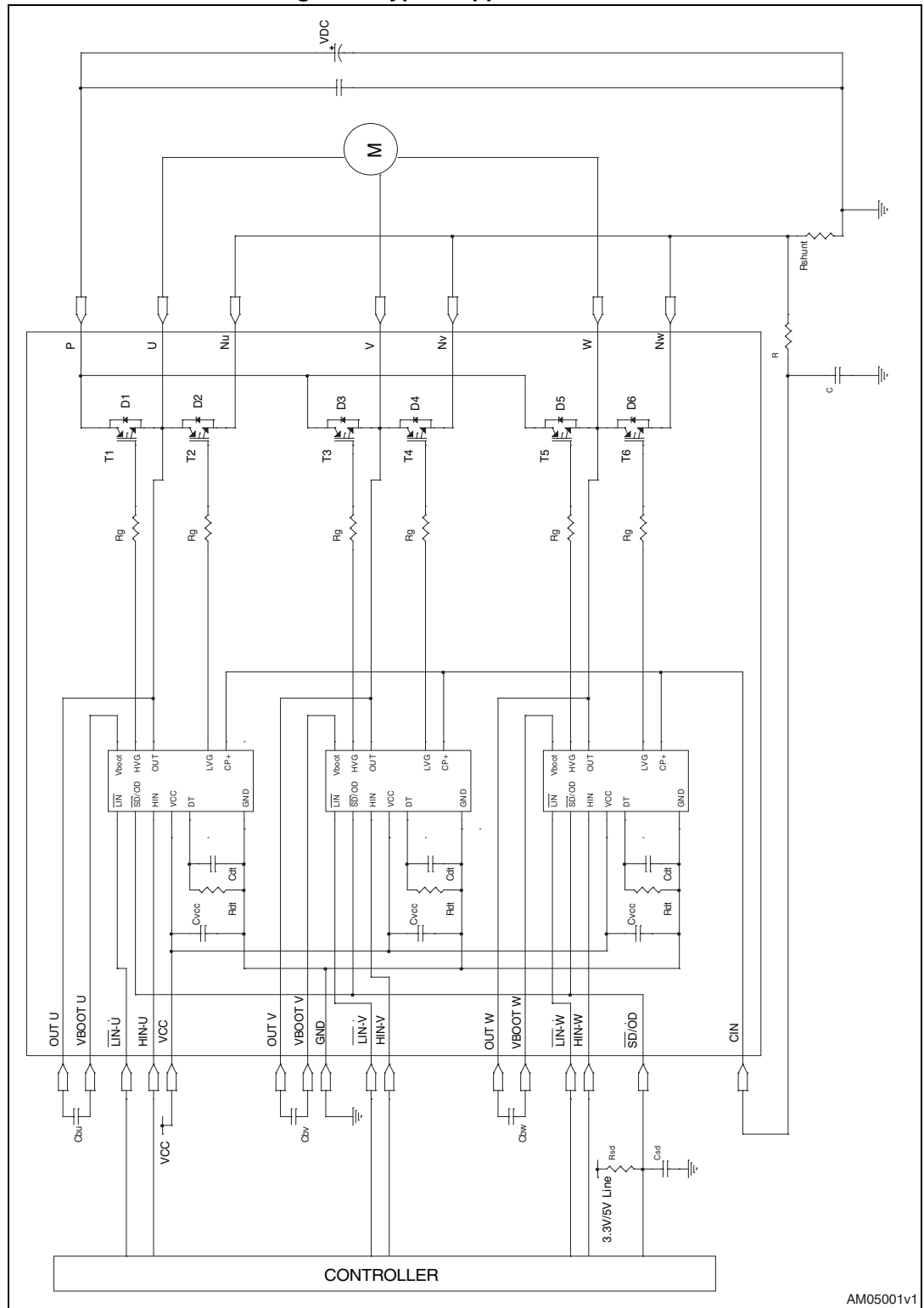
Figure 8. Smart shutdown timing waveforms



Note: Please refer to [Table 11](#) for internal propagation delay time details.

## 5 Applications information

### Figure 9. Typical application circuit



## 5.1 Recommendations

- Input signal HIN is active high logic. A 85 k $\Omega$  (typ.) pull down resistor is built-in for each high side input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- Input signal /LIN is active low logic. A 720 k $\Omega$  (typ.) pull-up resistor, connected to an internal 5 V regulator through a diode, is built-in for each low side input.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The  $\overline{\text{SD}}/\text{OD}$  signal should be pulled up to 5 V / 3.3 V with an external resistor (see [Section 4: Smart shutdown function](#) for detailed info).

**Table 13. Recommended operating conditions**

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{PN}$	Supply voltage	Applied between P-Nu, Nv, Nw		300	400	V
$V_{CC}$	Control supply voltage	Applied between $V_{CC}$ -GND	13.5	15	18	V
$V_{BS}$	High side bias voltage	Applied between $V_{BOOTi}$ - $\text{OUT}_i$ for $i = U, V, W$	13		18	V
$t_{\text{dead}}$	Blanking time to prevent Arm-short	For each input signal	1			$\mu\text{s}$
$f_{\text{PWM}}$	PWM input signal	$-40^\circ\text{C} < T_c < 100^\circ\text{C}$ $-40^\circ\text{C} < T_j < 125^\circ\text{C}$			20	kHz
$T_c$	Case operation temperature				100	$^\circ\text{C}$

*Note:* For further details refer to AN3338.



## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

### 6.1 SDIP-25L package information

Figure 10. SDIP-25L package outline

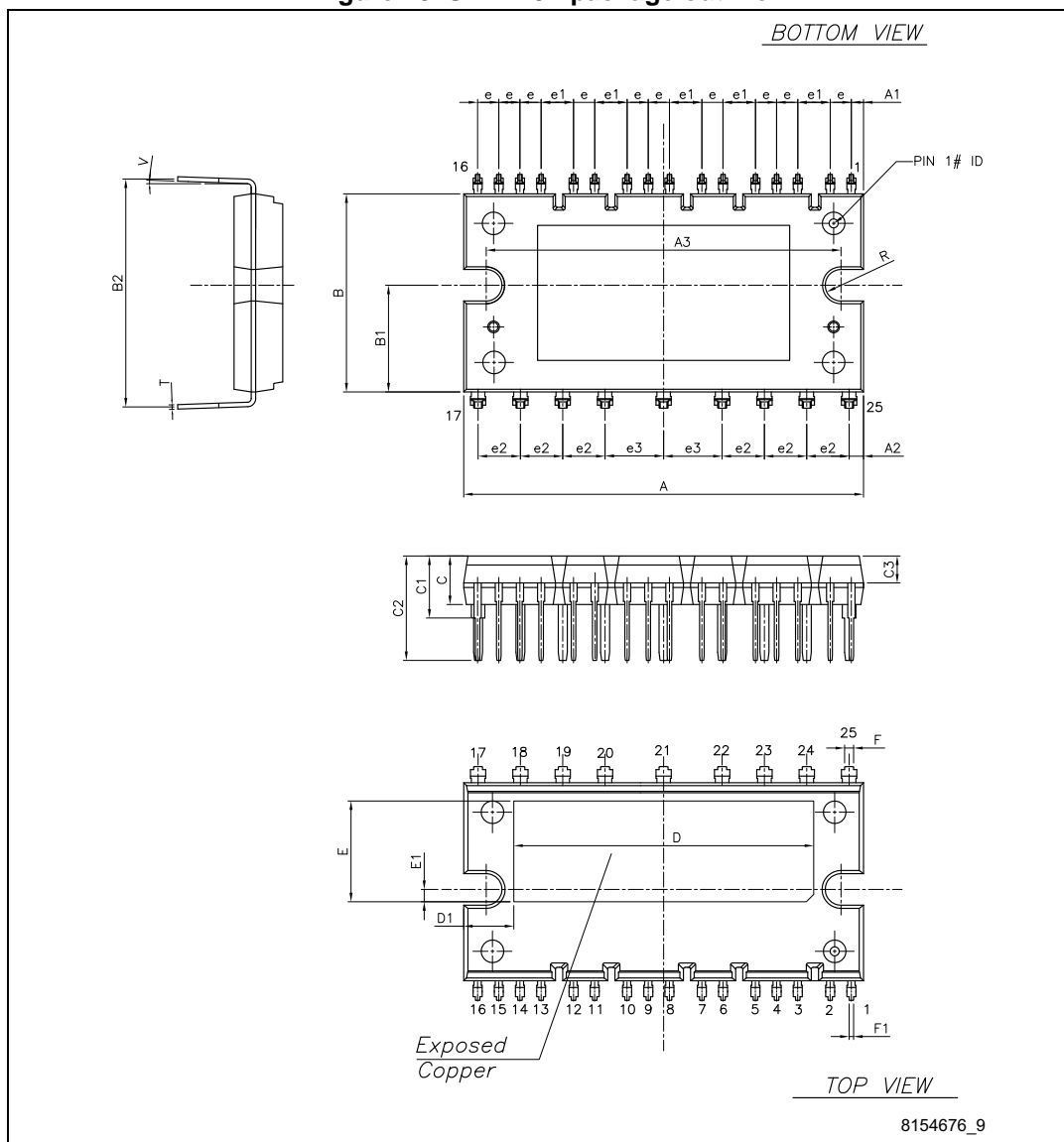
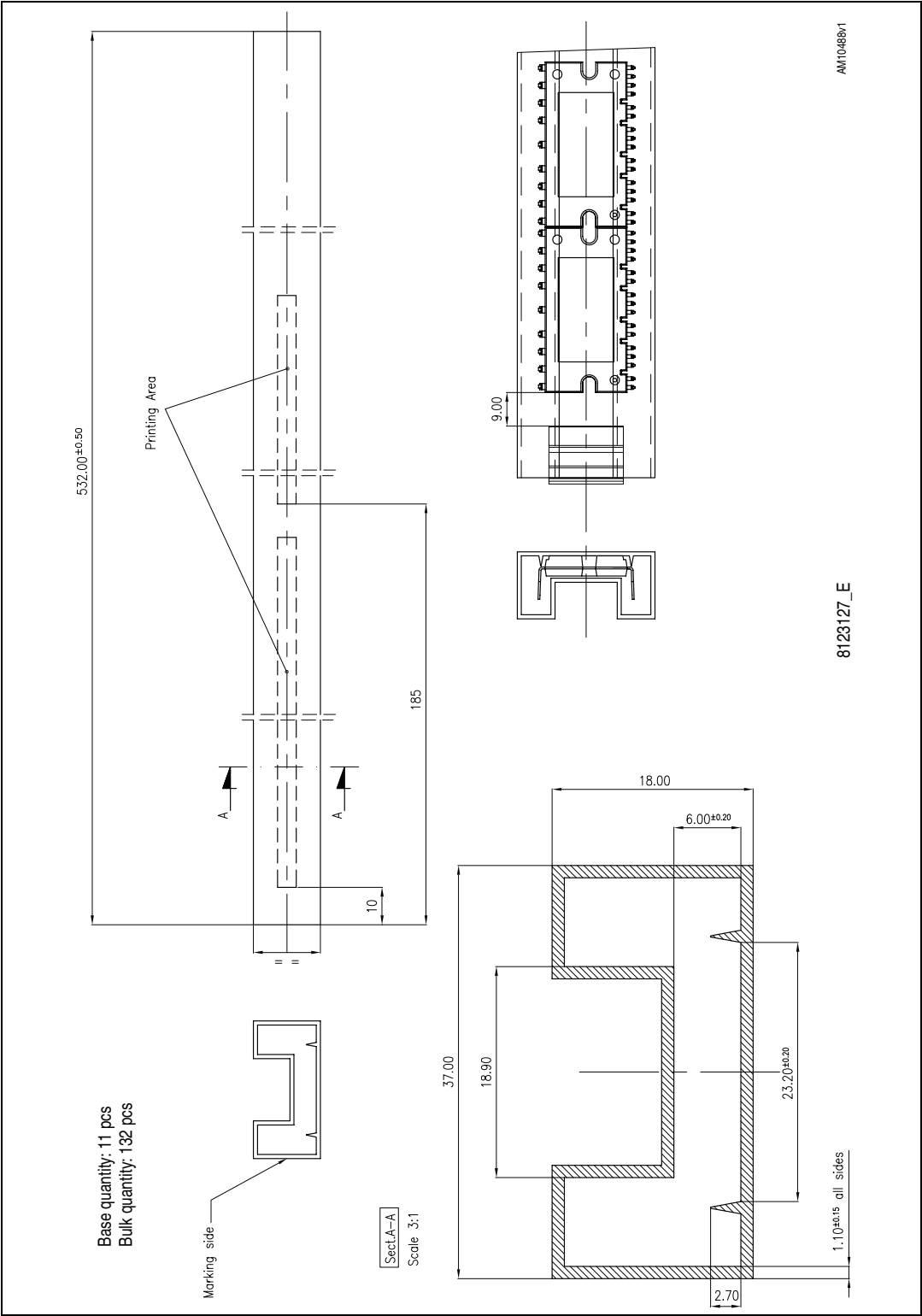


Table 14. SDIP-25L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	43.90	44.40	44.90
A1	1.15	1.35	1.55
A2	1.40	1.60	1.80
A3	38.90	39.40	39.90
B	21.50	22.00	22.50
B1	11.25	11.85	12.45
B2	24.83	25.23	25.63
C	5.00	5.40	6.00
C1	6.50	7.00	7.50
C2	11.20	11.70	12.20
C3	2.90	3.00	3.10
e	2.15	2.35	2.55
e1	3.40	3.60	3.80
e2	4.50	4.70	4.90
e3	6.30	6.50	6.70
D		33.30	
D1		5.55	
E		11.20	
E1		1.40	
F	0.85	1.00	1.15
F1	0.35	0.50	0.65
R	1.55	1.75	1.95
T	0.45	0.55	0.65
V	0°		6°

6.2 Packing information

Figure 11. SDIP-25L packing information (dimensions are in mm.)



## 7 Revision history

**Table 15. Document revision history**

Date	Revision	Changes
25-Jun-2009	1	Initial release.
05-Aug-2009	2	Reduced $V_{CE(sat)}$ value on <a href="#">Table 7</a> .
15-Jun-2010	3	Document status promoted from preliminary data to datasheet. Updated package mechanical data, <a href="#">Table 7: Inverter part</a> , <a href="#">Figure 5: Maximum <math>I_C(RMS)</math> current vs. switching frequency</a> and <a href="#">Figure 6: Maximum <math>I_C(RMS)</math> current vs. <math>f_{SINE}</math> (1)</a> . Minor text changes to improve readability.
08-Nov-2010	4	Updated <a href="#">Table 3</a> , <a href="#">5</a> , <a href="#">8</a> , <a href="#">9</a> , <a href="#">10</a> and <a href="#">Table 11</a> . Modified: <a href="#">Figure 5</a> and <a href="#">Figure 6</a> .
09-Mar-2011	5	Updated title with SLLIMM™ in cover page, added SDIP-25L tube dimensions <a href="#">Figure 11 on page 19</a> .
04-Nov-2011	6	Updated title with SLLIMM™ (small low-loss intelligent molded module) IPM, 3-phase inverter - 14 A, 600 V short-circuit rugged IGBT in cover page and SDIP-25L mechanical data <a href="#">Table 14 on page 17</a> , <a href="#">Figure 10 on page 17</a> .
28-Aug-2012	7	Modified: Min. and Max. value <a href="#">Table 4 on page 5</a> . Updated: <a href="#">Figure 11 on page 19</a> . Added: <a href="#">Figure 12 on page 20</a> .
02-May-2013	8	Updated: <a href="#">Figure 3 on page 8</a> . Modified: <a href="#">Section 4</a> and <a href="#">Figure 8 on page 14</a> .
15-Apr-2015	9	Text edits and formatting changes throughout document Updated <a href="#">Figure 2: Pin layout (bottom view)</a> Updated <a href="#">Section 6: Package information</a>

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