HMC637ALP5E

v02.0418

GaAs pHEMT MMIC 1 WATT POWER AMPLIFIER, DC - 6 GHz

Typical Applications

The HMC637ALP5E wideband PA is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military & Space
- Test Instrumentation
- Fiber Optics

Features

P1dB Output Power: +29 dBm

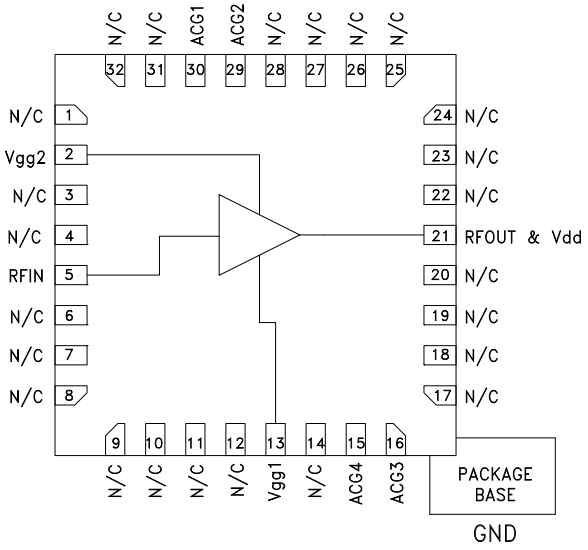
Gain: 13 dB

Output IP3: +44 dBm

50 Ohm Matched Input/Output

32 Lead 5x5mm Lead SMT Package: 25 mm^2

Functional Diagram



General Description

The HMC637ALP5E is a GaAs MMIC pHEMT Distributed Power Amplifier which operates between DC and 6 GHz. The amplifier provides 13 dB of gain, +44 dBm output IP3 and +29 dBm of output power at 1 dB gain compression while requiring 400 mA from a +12V supply. Gain flatness is excellent at ±0.75 dB from DC - 6 GHz making the HMC637ALP5E ideal for EW, ECM, Radar and test equipment applications. The HMC637ALP5E amplifier I/Os are internally matched to 50 Ohms and the 5x5 mm QFN package is compatible with high volume SMT assembly equipment.

Electrical Specifications, T_A = +25° C, Vdd= +12V, Vgg2= +5V, Idd= 400 mA[1]

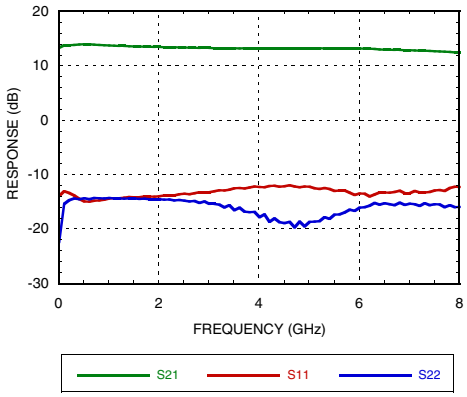
Parameter	Frequency	Min.	Typ.	Max.	Units
Gain	DC - 6.0 GHz	12	13		dB
Gain Flatness	DC - 6.0 GHz		±0.75		dB
Gain Variation Over Temperature	DC - 6.0 GHz		0.015		dB/ °C
Input Return Loss	DC - 6.0 GHz		12		dB
Output Return Loss	DC - 6.0 GHz		15		dB
Output Power for 1 dB Compression (P1dB)	DC - 6.0 GHz	27	29		dBm
Saturated Output Power (Psat)	DC - 6.0 GHz		31		dBm
Output Third Order Intercept (OIP3)[2]	DC - 6.0 GHz		44		dBm
Noise Figure	DC - 2.0 GHz 2.0 - 6.0 GHz		12 5		dB dB
Supply Current (Idd)		320	400	480	mA

[1] Adjust Vgg1 between -2 to 0V to achieve Idd= 400 mA typical.

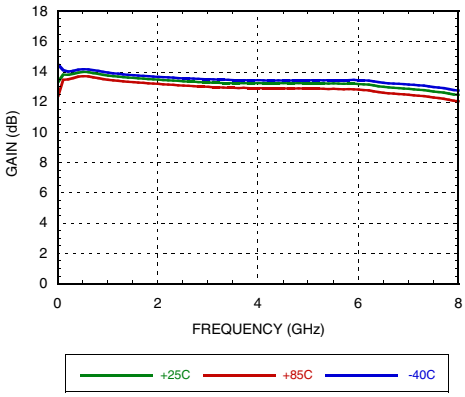
[2] Two-Tone Output Power = +10 dBm Each Tone, 1 MHz Spacing.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

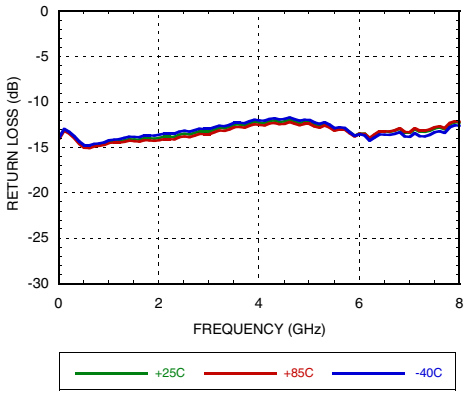
Gain & Return Loss



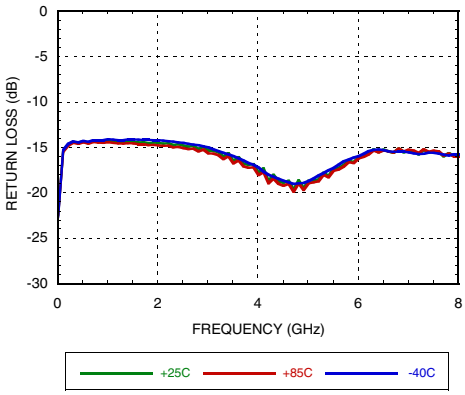
Gain vs. Temperature



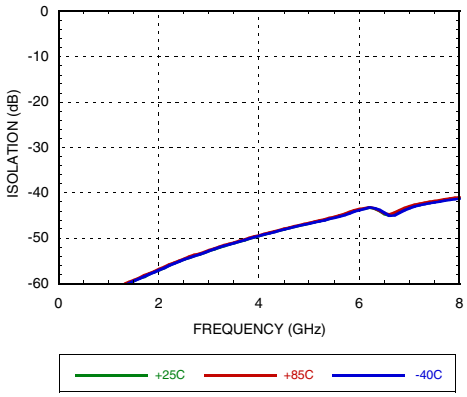
Input Return Loss vs. Temperature



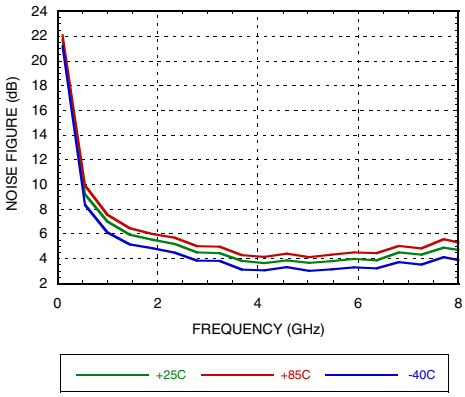
Output Return Loss vs. Temperature



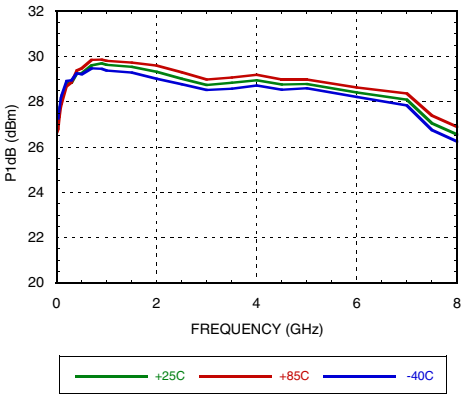
Reverse Isolation vs. Temperature



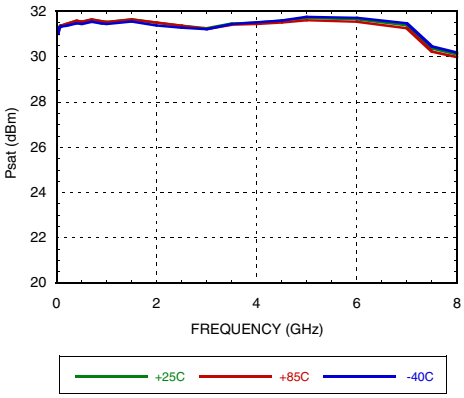
Noise Figure vs. Temperature



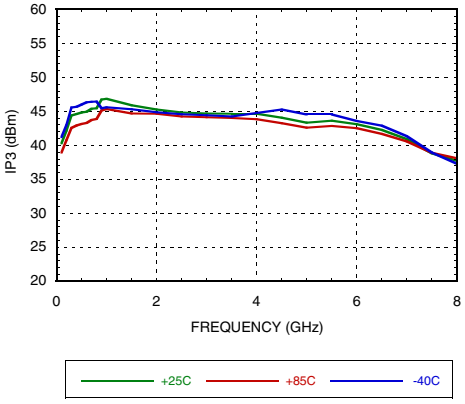
P1dB vs. Temperature



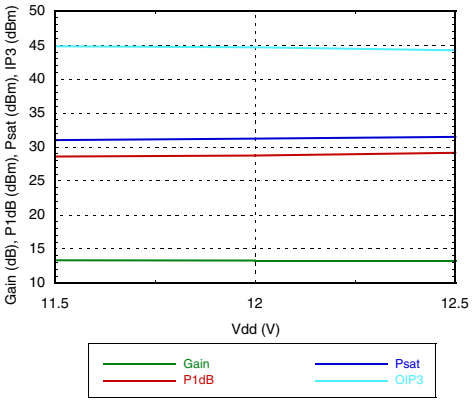
Psat vs. Temperature



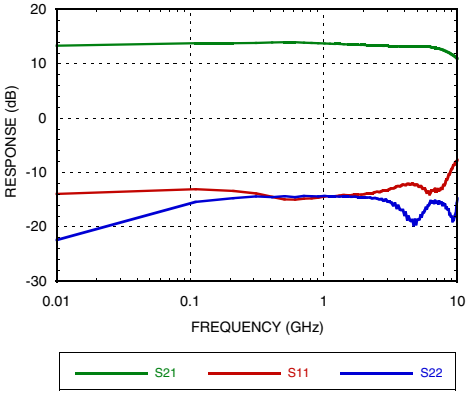
Output IP3 vs. Temperature



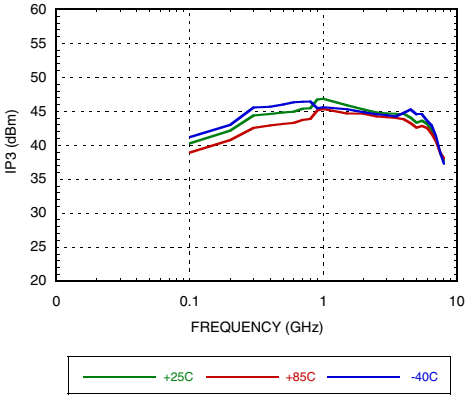
Gain, Power & Output IP3 vs. Supply Voltage @ 3 GHz, Fixed Vgg



Gain & Return Loss vs. Frequency, Log Scale



Output IP3 vs. Temperature, Log Scale



Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+14 Vdc
Gate Bias Voltage (Vgg1)	-3 to 0 Vdc
Gate Bias Voltage (Vgg2)	+4 to +7 Vdc
RF Input Power (RFIN)(Vdd = +12 Vdc)	+25 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 95 mW/°C above 85 °C)	8.6 W
Thermal Resistance (channel to ground paddle)	10.5 °C/W
Storage Temperature	-65 to 150 °C
Operating Temperature	-40 to 85 °C
ESD Sensitivity (HBM)	Class 1B

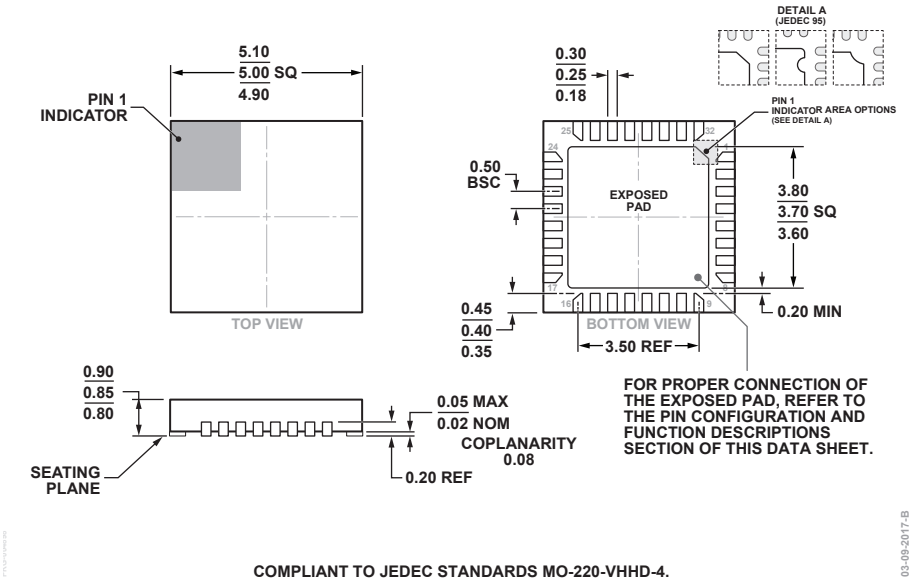
Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)[1]
11.5	400
12.0	400
12.5	400

[1] Vgg1 set intitially for nominal bias condition of Vdd = +12 V and Vgg2 = +5V to achieve Idd = 400 mA typical. Then adjusting Vdd +/- 0.5 V from 12V to measure Idd variation.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-4.

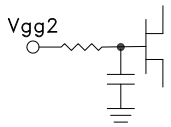
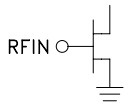
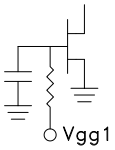
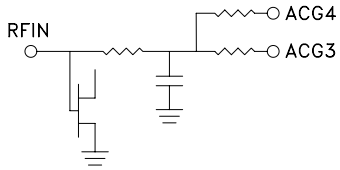
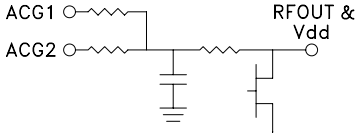
32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm and 0.85 mm Package Height
(HCP-32-1)
Dimensions shown in millimeters.

Package Information

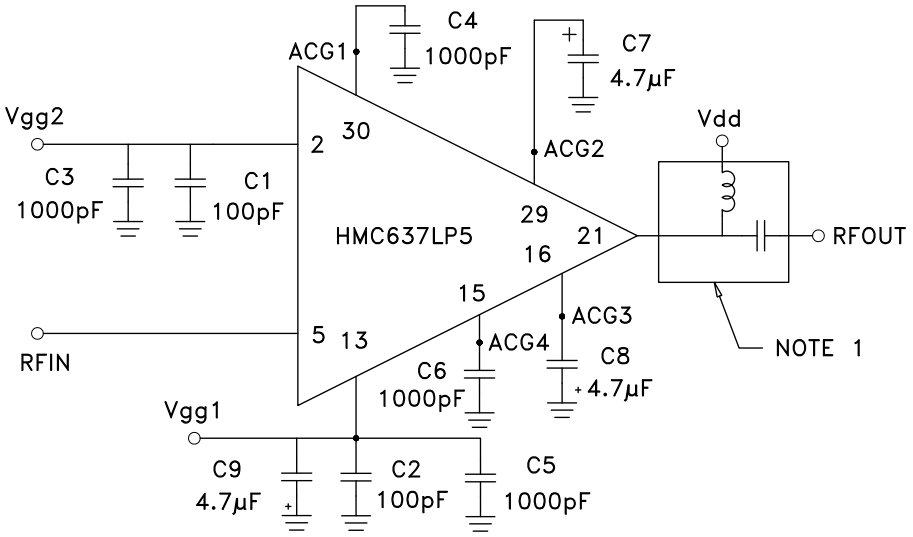
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC637ALP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3 [1]	H637A XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 4, 6 - 12, 14, 17, 18, 19, 20, 22 - 28, 31, 32	N/C	No connection. These pins may be connected to RF ground. Performance will not be affected.	
2	Vgg2	Gate Control 2 for amplifier. +5V should be applied to Vgg2 for nominal operation. Attach bypass capacitor per application circuit herein.	
5	RFIN	This pad is DC coupled and matched to 50 Ohms.	
13	Vgg1	Gate Control 1 for amplifier. Attach bypass capacitor per application circuit herein. Please follow "MMIC Amplifier Biasing Procedure" Application Note.	
15	ACG4	Low frequency termination. Attach bypass capacitor per application circuit herein.	
16	ACG3		
21	RFOUT & Vdd	RF output for amplifier. Connect the DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
29	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein.	
30	ACG1		
Ground Paddle	GND	Ground paddle must be connected to RF/DC ground.	

Application Circuit

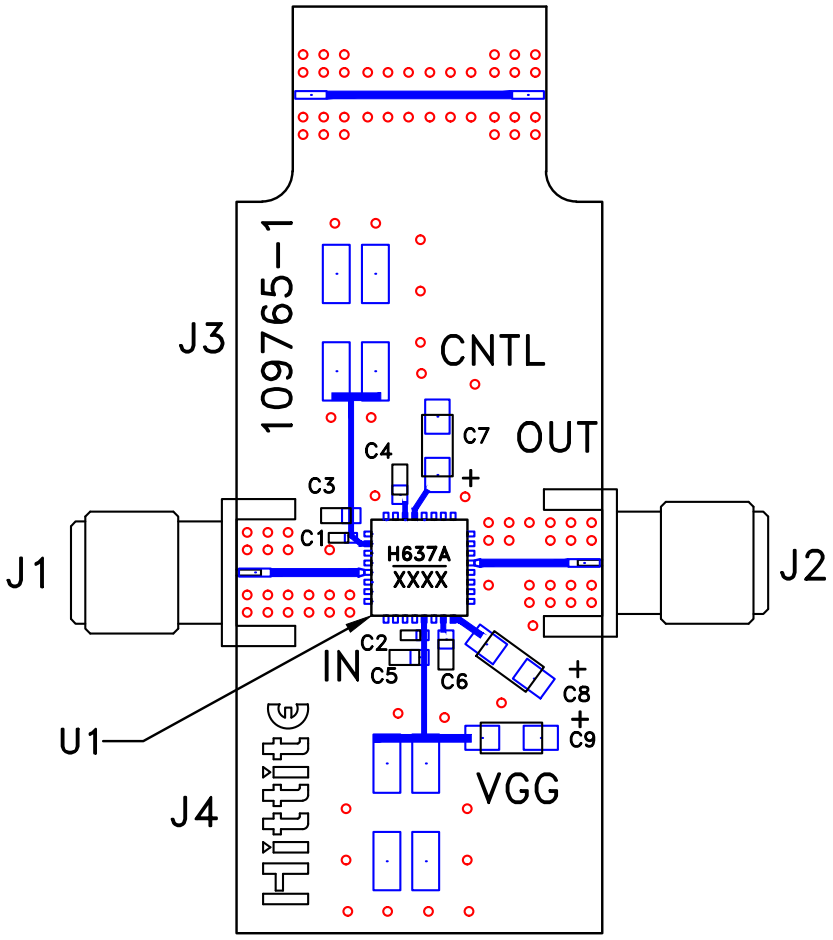


NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

NOTE 2: Power Up Bias Sequence
A) Set Vgg1 to -2V
B) Set Vdd to +12V
C) Set Vgg2 to +5V
D) Adjust Vgg1 to achieve Idd for 400 mA

Power Down Sequence
A) Remove Vgg2 Bias
B) Remove Vdd Bias
C) Remove Vgg1 Bias

Evaluation PCB



List of Materials for Evaluation PCB EV1HMC637ALP5 [1]

Item	Description
J1 - J2	SRI SMA Connector
J3 - J4	2mm Molex Header
C1, C2	100 pF Capacitor, 0402 Pkg.
C3 - C6	1000 pF Capacitor, 0603 Pkg.
C7 - C9	4.7 µF Capacitor, Tantalum
U1	HMC637ALP5E
PCB [2]	109765 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Analog Devices, upon request.