DS25BR100 / DS25BR101 3.125 Gbps LVDS Buffer with Transmit Pre-Emphasis and Receive Equalization

Check for Samples: DS25BR100

FEATURES

- **DC - 3.125 Gbps Low Jitter, High Noise Immunity, Low Power Operation**
- **Receive Equalization Reduces ISI Jitter Due to Media Loss**
- **Transmit Pre-Emphasis Drives Lossy Backplanes and Cables**
- **On-Chip 100Ω Input and Output Termination:**
  - **Minimizes Insertion and Return Losses**
  - **Reduces Component Count**
  - **Minimizes Board Space**
- **DS25BR101 Eliminates On-Chip Input Termination for Added Design Flexibility**
- **7 kV ESD on LVDS I/O Pins Protects Adjoining Components**
- **Small 3 mm x 3 mm WSON-8 Space Saving Package**

APPLICATIONS

- **Clock and Data Buffering**
- **Metallic Cable Driving and Equalization**
- **FR-4 Equalization**

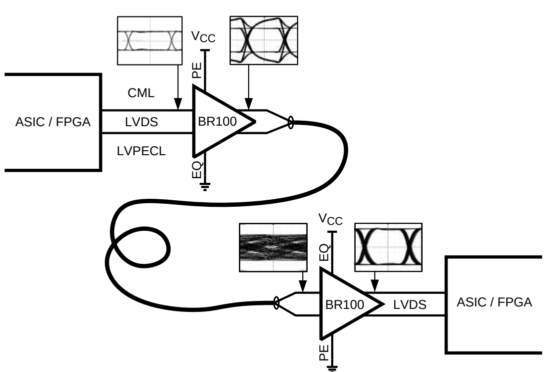
DESCRIPTION

The DS25BR100 and DS25BR101 are single channel 3.125 Gbps LVDS buffers optimized for high-speed signal transmission over lossy FR-4 printed circuit board backplanes and balanced metallic cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

The DS25BR100 and DS25BR101 feature transmit pre-emphasis (PE) and receive equalization (EQ), making them ideal for use as a repeater device. Other LVDS devices with similar IO characteristics include the following products. The DS25BR120 features four levels of pre-emphasis for use as an optimized driver device, while the DS25BR110 features four levels of equalization for use as an optimized receiver device. The DS25BR150 is a buffer/repeater with the lowest power consumption and does not feature transmit pre-emphasis nor receive equalization.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires minimal space on the board while the flow-through pinout allows easy board layout. On the DS25BR100 the differential input and output is internally terminated with a 100Ω resistor to lower return losses, reduce component count and further minimize board space. For added design flexibility the 100Ω input terminations on the DS25BR101 have been eliminated. This elimination enables a designer to adjust the termination for custom interconnect topologies and layout.

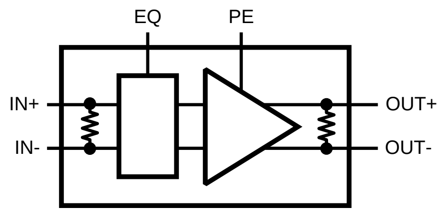
Typical Application



Device Information

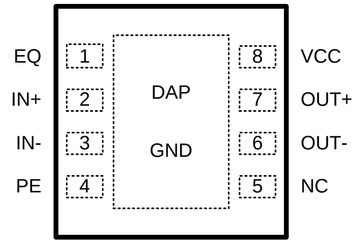
Device	Function	Termination Option	Available Signal Conditioning
DS25BR100	Buffer / Repeater	Internal 100Ω for LVDS inputs	2 Levels: PE and EQ
DS25BR101	Buffer / Repeater	External termination required	2 Levels: PE and EQ
DS25BR110	Receiver	Internal 100Ω for LVDS inputs	4 Levels: EQ
DS25BR120	Driver	Internal 100Ω for LVDS inputs	4 Levels: PE
DS25BR150	Buffer / Repeater	Internal 100Ω for LVDS inputs	None

Block Diagram



DS25BR101 eliminates 100Ω input termination.

Pin Diagram



PIN DESCRIPTIONS

Pin Name	Pin Name	Pin Type	Pin Description
EQ	1	Input	Equalizer select pin.
IN+	2	Input	Non-inverting LVDS input pin.
IN-	3	Input	Inverting LVDS input pin.
PE	4	Input	Pre-emphasis select pin.
NC	5	NA	"NO CONNECT" pin.
OUT-	6	Output	Inverting LVDS output pin.
OUT+	7	Output	Non-inverting LVDS Output pin.
VCC	8	Power	Power supply pin.
GND	DAP	Power	Ground pad (DAP - die attach pad).

Control Pins (PE and EQ) Truth Table

EQ	PE	Equalization Level	Pre-emphasis Level
0	0	Low (Approx. 4 dB at 1.56 GHz)	Off
0	1	Low (Approx. 4 dB at 1.56 GHz)	Medium (Approx. 6 dB at 1.56 GHz)
1	0	Medium (Approx. 8 dB at 1.56 GHz)	Off
1	1	Medium (Approx. 8 dB at 1.56 GHz)	Medium (Approx. 6 dB at 1.56 GHz)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage (V_{CC})		−0.3V to +4V
LVCMOS Input Voltage (EQ, PE)		−0.3V to (V_{CC} + 0.3V)
LVDS Input Voltage (IN+, IN−)		−0.3V to +4V
Differential Input Voltage |VID| (DS25BR100)		1V
LVDS Differential Input Voltage (DS25BR101)		V_{CC} + 0.6V
LVDS Output Voltage (OUT+, OUT−)		−0.3V to (V_{CC} + 0.3V)
LVDS Differential Output Voltage ((OUT+) - (OUT−))		0V to 1V
LVDS Output Short Circuit Current Duration		5 ms
Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range	Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	NGQ0008A Package	2.08W
	Derate NGQ0008A Package	16.7 mW/°C above +25°C
Package Thermal Resistance	θ_{JA}	+60.0°C/W
	θ_{JC}	+12.3°C/W
ESD Susceptibility	HBM (3)	≥7 kV
	MM (4)	≥250V
	CDM (5)	≥1250V

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID}) (DS25BR100 only)			1.0	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified[1][2][3]

Parameter		Test Conditions	Min	Typ	Max	Units
LVCMOS INPUT DC SPECIFICATIONS (EQ, PE)						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V V_{CC} = 3.6V		0	±10	μA
I_{IL}	Low Level Input Current	V_{IN} = GND V_{CC} = 3.6V		0	±10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA, V_{CC} = 0V		-0.9	−1.5	V
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	R_L = 100Ω	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current[4]	OUT to GND, PE = 0		-35	-55	mA
		OUT to V_{CC}, PE = 0		7	55	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
LVDS INPUT DC SPECIFICATIONS (IN+, IN-)						
V_{ID}	Input Differential Voltage[5]		0		1	V
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V or V_{CC}-0.05V		0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100 mV	0.05		V_{CC} - 0.05	V
I_{IN}	Input Current	V_{IN} = GND or 3.6V V_{CC} = 3.6V or 0.0V		±1	±10	μA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R_{IN}	Input Termination Resistor[6]	Between IN+ and IN-		100		Ω
SUPPLY CURRENT						
I_{CC}	Supply Current	EQ = 0, PE = 0		35	43	mA

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.
(5) Input Differential Voltage (V_{ID}) The DS25BR100 limits input amplitude to 1 volt. The DS25BR101 supports any V_{ID} within the supply voltage to GND range.
(6) Input Termination Resistor (R_{IN}) The DS25BR100 provides an integrated 100 ohm input termination for the high speed LVDS pair. The DS25BR101 eliminates this internal termination.

AC Electrical Characteristics[1]

Over recommended operating supply and temperature ranges unless otherwise specified[2][3]

Parameter		Test Conditions		Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-)							
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$			350	465	ps
t_{PLHD}	Differential Propagation Delay Low to High				350	465	ps
t_{SKD1}	Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$[4]				45	100	ps
t_{SKD2}	Part to Part Skew[5]				45	150	ps
t_{LHT}	Rise Time	$R_L = 100\Omega$			80	150	ps
t_{HLT}	Fall Time				80	150	ps
JITTER PERFORMANCE WITH PE = OFF AND EQ = LOW[6][7]							
t_{RJ1A}	Random Jitter (RMS Value) Input Test Channel D[8]	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ) PE = 0, EQ = 0	2.5 Gbps		0.5	1	ps
t_{RJ2A}			3.125 Gbps		0.5	1	ps
t_{DJ1A}	Deterministic Jitter (Peak to Peak) Input Test Channel D[9]	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ) PE = 0, EQ = 0	2.5 Gbps		1	16	ps
t_{DJ2A}			3.125 Gbps		11	31	ps
t_{TJ1A}	Total Jitter (Peak to Peak) Input Test Channel D[10]	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ) PE = 0, EQ = 0	2.5 Gbps		0.03	0.09	UI_{P-P}
t_{TJ2A}			3.125 Gbps		0.06	0.14	UI_{P-P}
JITTER PERFORMANCE WITH PE = OFF AND EQ = MEDIUM[6][7]							
t_{RJ1B}	Random Jitter (RMS Value) Input Test Channel E[8]	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ) PE = 0, EQ = 1	2.5 Gbps		0.5	1	ps
t_{RJ2B}			3.125 Gbps		0.5	1	ps
t_{DJ1B}	Deterministic Jitter (Peak to Peak) Input Test Channel E[9]	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ) PE = 0, EQ = 1	2.5 Gbps		10	29	ps
t_{DJ2B}			3.125 Gbps		27	43	ps
t_{TJ1B}	Total Jitter (Peak to Peak) Input Test Channel E[10]	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ) PE = 0, EQ = 1	2.5 Gbps		0.07	0.12	UI_{P-P}
t_{TJ2B}			3.125 Gbps		0.12	0.17	UI_{P-P}

(1) Specification is ensured by characterization and is not tested in production.
(2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(4) t_{SKD1}, $\lvert t_{PLHD} - t_{PHLD} \rvert$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) t_{SKD2}, Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(6) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(7) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(8) Measured on a clock edge with a histogram and an acummulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
(9) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
(10) Measured on an eye diagram with a histogram and an acummulation of 3500 histogram hits. Input stimulus jitter is subtracted.

AC Electrical Characteristics[1] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified[2][3]

Parameter		Test Conditions		Min	Typ	Max	Units
JITTER PERFORMANCE WITH PE = MEDIUM AND EQ = LOW[11][12]							
t_{RJ1C}	Random Jitter (RMS Value) Input Test Channel D Output Test Channel B[13]	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ) PE = 1, EQ = 0	2.5 Gbps		0.5	1	ps
t_{RJ2C}			3.125 Gbps		0.5	1	ps
t_{DJ1C}	Deterministic Jitter (Peak to Peak) Input Test Channel D Output Test Channel B[14]	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ) PE = 1, EQ = 0	2.5 Gbps		29	57	ps
t_{DJ2C}			3.125 Gbps		29	51	ps
t_{TJ1C}	Total Jitter (Peak to Peak) Input Test Channel D Output Test Channel B[15]	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ) PE = 1, EQ = 0	2.5 Gbps		0.10	0.19	UI_{P-P}
t_{TJ2C}			3.125 Gbps		0.13	0.22	UI_{P-P}
JITTER PERFORMANCE WITH PE = MEDIUM AND EQ = MEDIUM[11][12]							
t_{RJ1D}	Random Jitter (RMS Value) Input Test Channel E Output Test Channel B[13]	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ) PE = 1, EQ = 1	2.5 Gbps		0.5	1.1	ps
t_{RJ2D}			3.125 Gbps		0.5	1	ps
t_{DJ1D}	Deterministic Jitter (Peak to Peak) Input Test Channel E Output Test Channel B[14]	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ) PE = 1, EQ = 1	2.5 Gbps		41	77	ps
t_{DJ2D}			3.125 Gbps		46	98	ps
t_{TJ1D}	Total Jitter (Peak to Peak) Input Test Channel E Output Test Channel B[15]	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ) PE = 1, EQ = 1	2.5 Gbps		0.13	0.20	UI_{P-P}
t_{TJ2D}			3.125 Gbps		0.19	0.30	UI_{P-P}

(11) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(12) Input Differential Voltage (V_{ID}) The DS25BR100 limits input amplitude to 1 volt. The DS25BR101 supports any V_{ID} within the supply voltage to GND range.
(13) Measured on a clock edge with a histogram and an acummulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
(14) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
(15) Measured on an eye diagram with a histogram and an acummulation of 3500 histogram hits. Input stimulus jitter is subtracted.

Typical Performance Characteristics

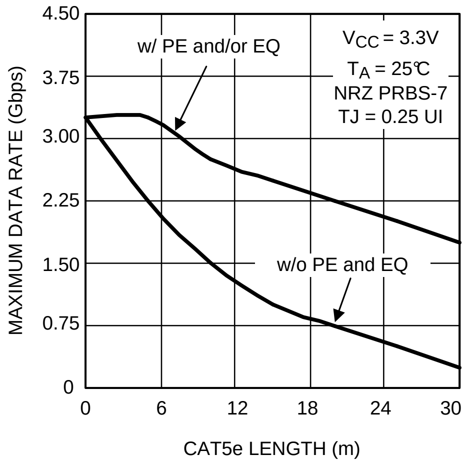


Figure 1. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length

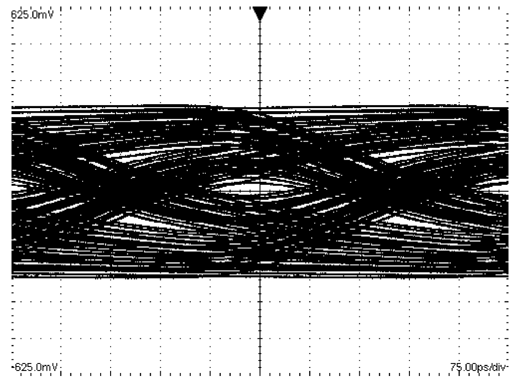


Figure 2. A 2.5 Gbps NRZ PRBS-7 After 60" Differential FR-4 Stripline V:125 mV / DIV, H:75 ps / DIV

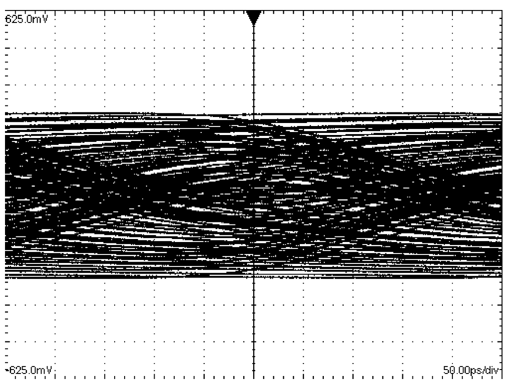


Figure 3. A 3.125 Gbps NRZ PRBS-7 After 60" Differential FR-4 Stripline V:125 mV / DIV, H:50 ps / DIV

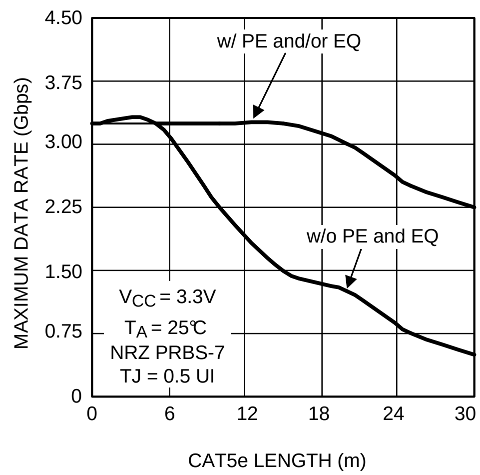


Figure 4. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length

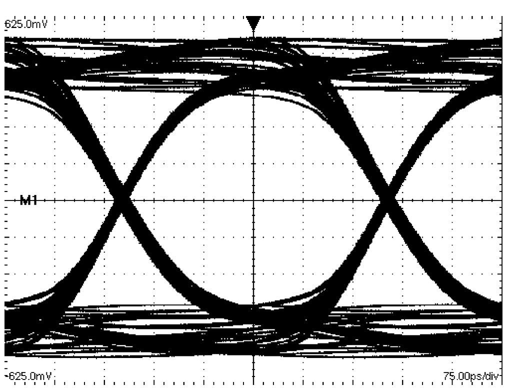


Figure 5. An Equalized (with PE and EQ) 2.5 Gbps NRZ PRBS-7 After The 40" Input and 20" Output Differential Stripline (Figure 16) V:125 mV / DIV, H:75 ps / DIV

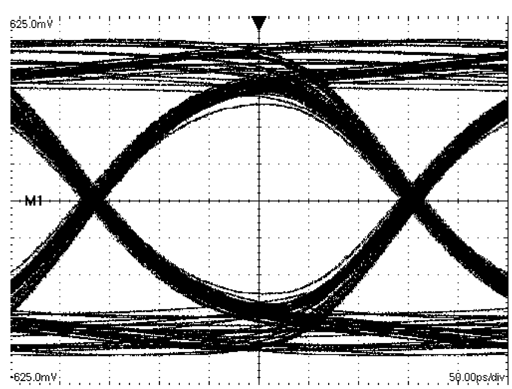


Figure 6. An Equalized (with PE and EQ) 3.125 Gbps NRZ PRBS-7 After The 40" Input and 20" Output Differential Stripline (Figure 16) V:125 mV / DIV, H:50 ps / DIV

Typical Performance Characteristics (continued)

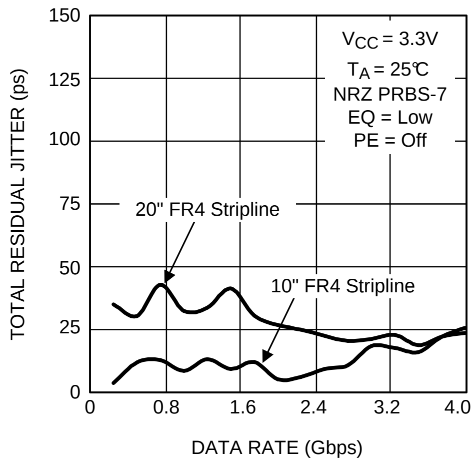


Figure 7. Total Jitter as a Function of Data Rate

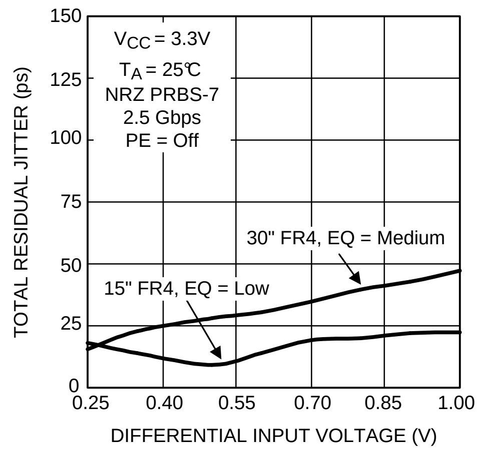


Figure 8. Total Jitter as a Function of Input Amplitude

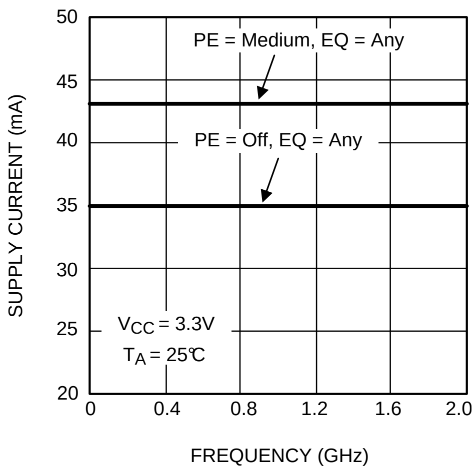


Figure 9. Power Supply Current as a Function of Frequency

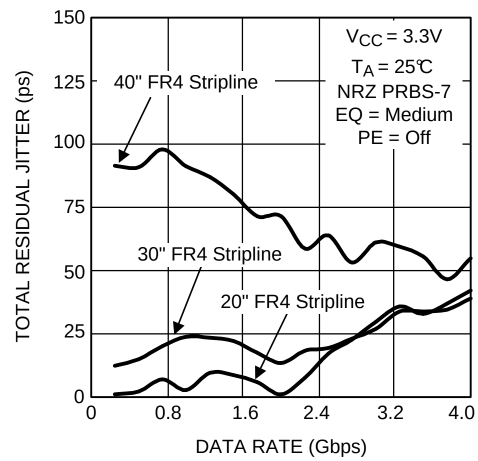


Figure 10. Total Jitter as a Function of Data Rate

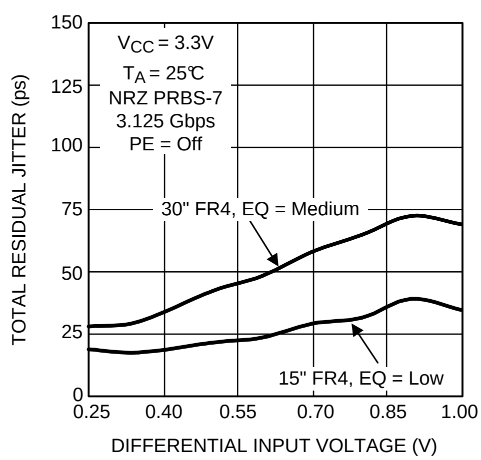


Figure 11. Total Jitter as a Function of Input Amplitude

APPLICATION INFORMATION

DC Test Circuits

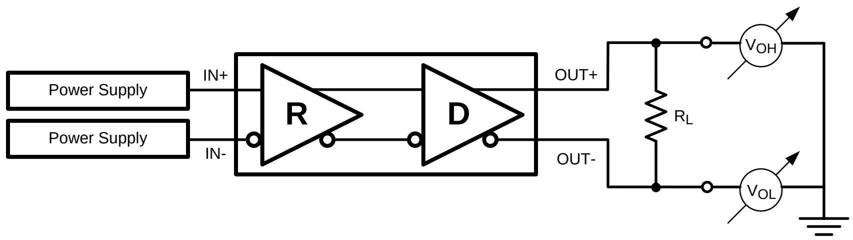


Figure 12. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

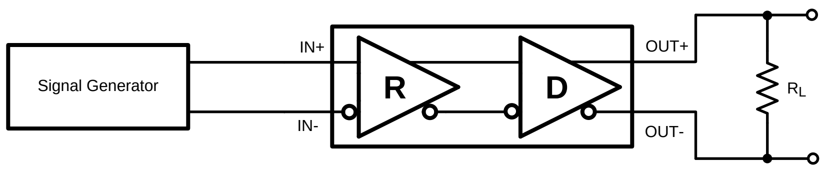


Figure 13. Differential Driver AC Test Circuit

NOTE

DS25BR101 requires external 100Ω input termination.

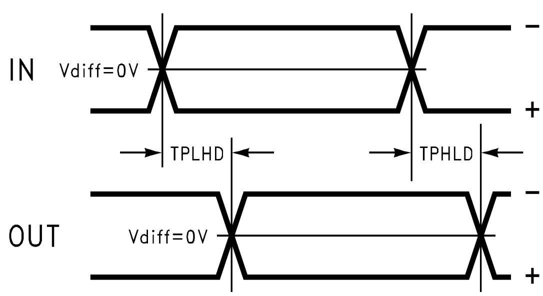


Figure 14. Propagation Delay Timing Diagram

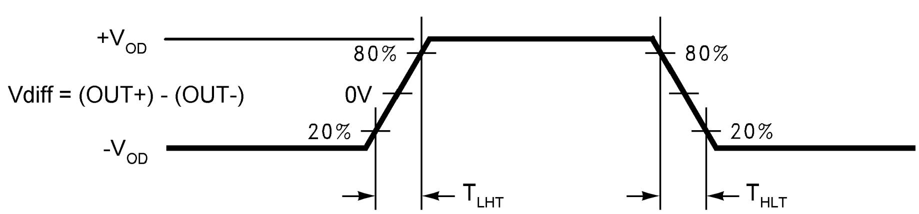


Figure 15. LVDS Output Transition Times

Pre-Emphasis and Equalization Test Circuits

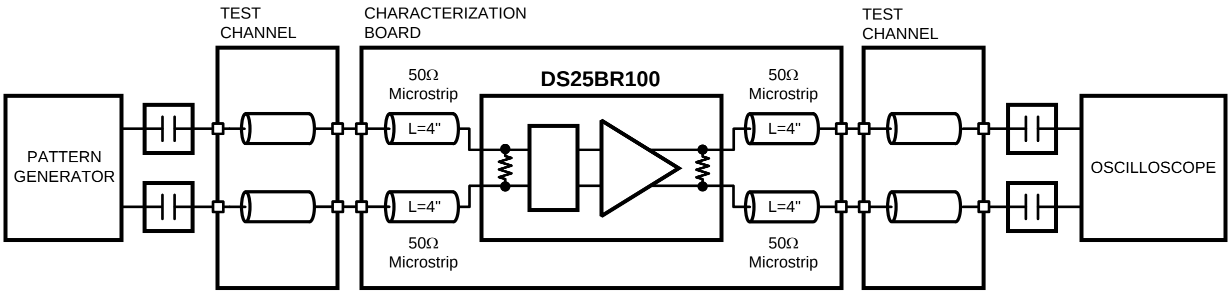


Figure 16. Pre-emphasis and Equalization Performance Test Circuit

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NOTE

DS25BR101 requires external 100Ω input termination.

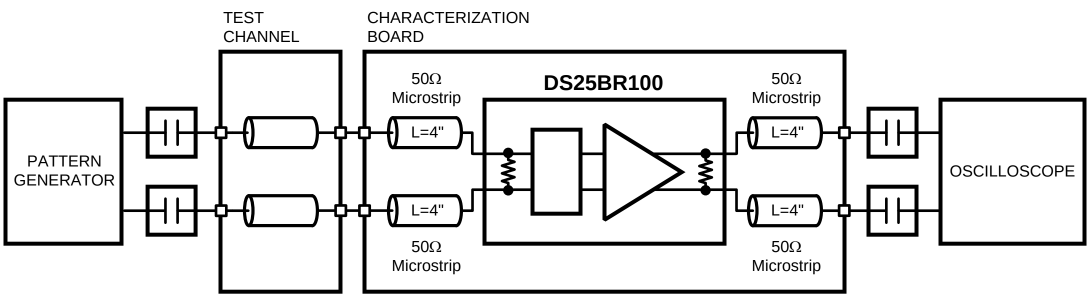

Figure 17. Equalization Performance Test Circuit

NOTE

DS25BR101 requires external 100Ω input termination.

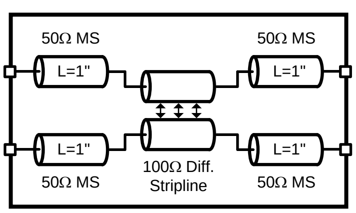

Figure 18. Test Channel Description

Test Channel Loss Characteristics

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

Test Channel	Length (inches)	Insertion Loss (dB)					
		500 MHz	750 MHz	1000 MHz	1250 MHz	1500 MHz	1560 MHz
A	10	-1.2	-1.7	-2.0	-2.4	-2.7	-2.8
B	20	-2.6	-3.5	-4.1	-4.8	-5.5	-5.6
C	30	-4.3	-5.7	-7.0	-8.2	-9.4	-9.7
D	15	-1.6	-2.2	-2.7	-3.2	-3.7	-3.8
E	30	-3.4	-4.5	-5.6	-6.6	-7.7	-7.9
F	60	-7.8	-10.3	-12.4	-14.5	-16.6	-17.0

Device Operation

INPUT INTERFACING

The DS25BR100/101 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR100/101 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers.

The DS25BR100 inputs are internally terminated with a 100Ω resistor for optimal device performance, reduced component count, and minimum board space. External input terminations on the DS25BR101 need to be placed as close as possible to the device inputs to achieve equivalent AC performance. It is recommended to use SMT resistors sized 0402 or smaller and to keep the mounting distance to the DS25BR101 pins under 200 mils.

When using the DS25BR101 in a limited multi-drop topology, any transmission line stubs should be kept very short to minimize any negative effects on signal quality. A single termination resistor or resistor network that matches the differential line impedance should be used. If DS25BR101 input pairs from two separate devices are to be connected to a single differential output, it is recommended to mount the DS25BR101 devices directly opposite of each other. One on top of the PCB and the other directly under the first on the bottom of the PCB keeps the distance between inputs equal to the PCB thickness.

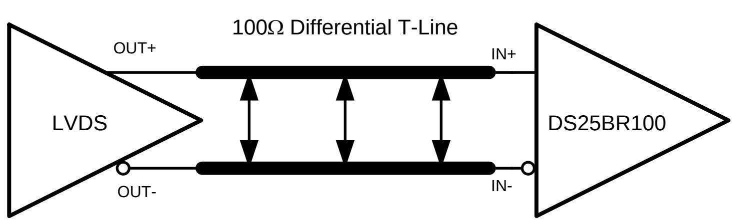

Figure 19. Typical LVDS Driver DC-Coupled Interface to DS25BR100 Input

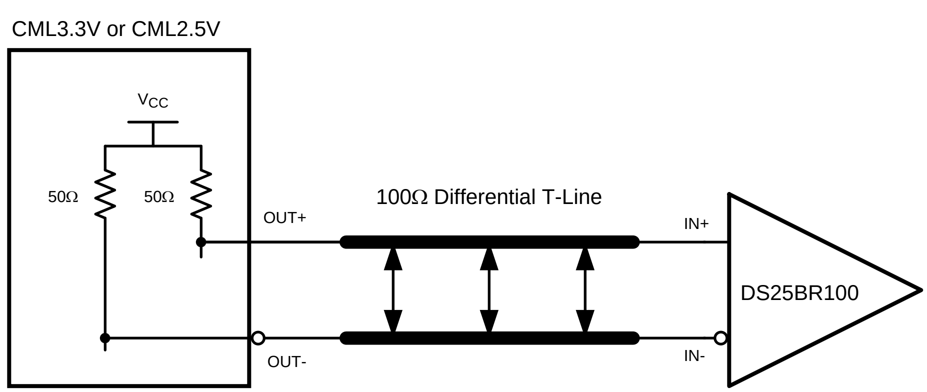

Figure 20. Typical CML Driver DC-Coupled Interface to DS25BR100 Input

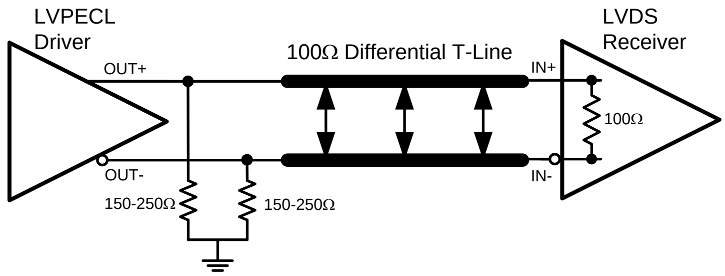

Figure 21. Typical LVPECL Driver DC-Coupled Interface to DS25BR100 Input

NOTE

DS25BR101 requires external 100Ω input termination.

OUTPUT INTERFACING

The DS25BR100/101 outputs signals are compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates the typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check the respective receiver's datasheet prior to implementing the suggested interface implementation.

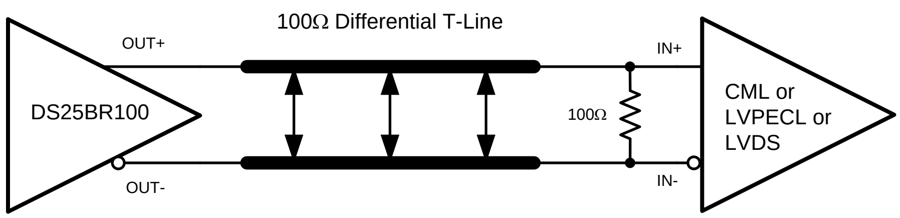

Figure 22. Typical Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS25BR100TSD/NOPB	ACTIVE	WSON	NGQ	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2R100	Samples
DS25BR101TSD/NOPB	ACTIVE	WSON	NGQ	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2R101	Samples
DS25BR101TSDE/NOPB	ACTIVE	WSON	NGQ	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2R101	Samples
DS25BR101TSDX/NOPB	ACTIVE	WSON	NGQ	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2R101	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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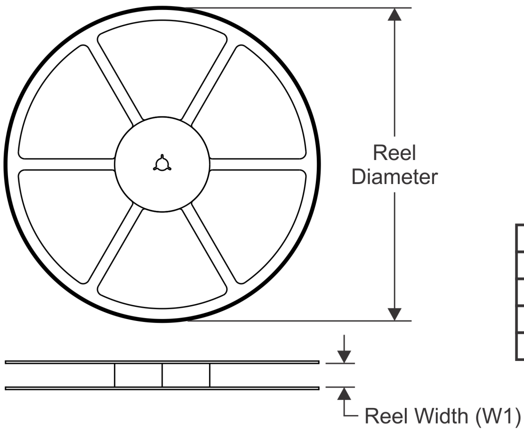
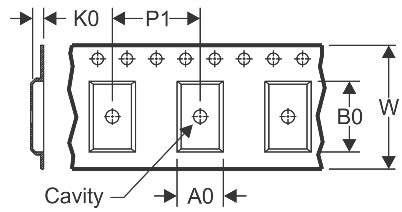
TAPE AND REEL INFORMATION

REEL DIMENSIONS

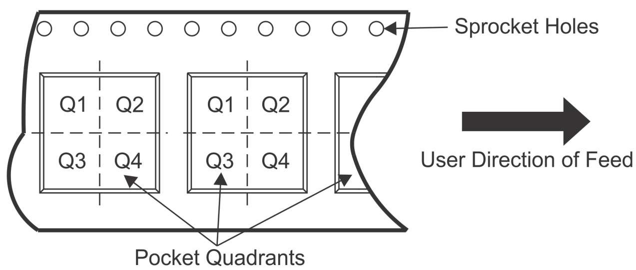


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

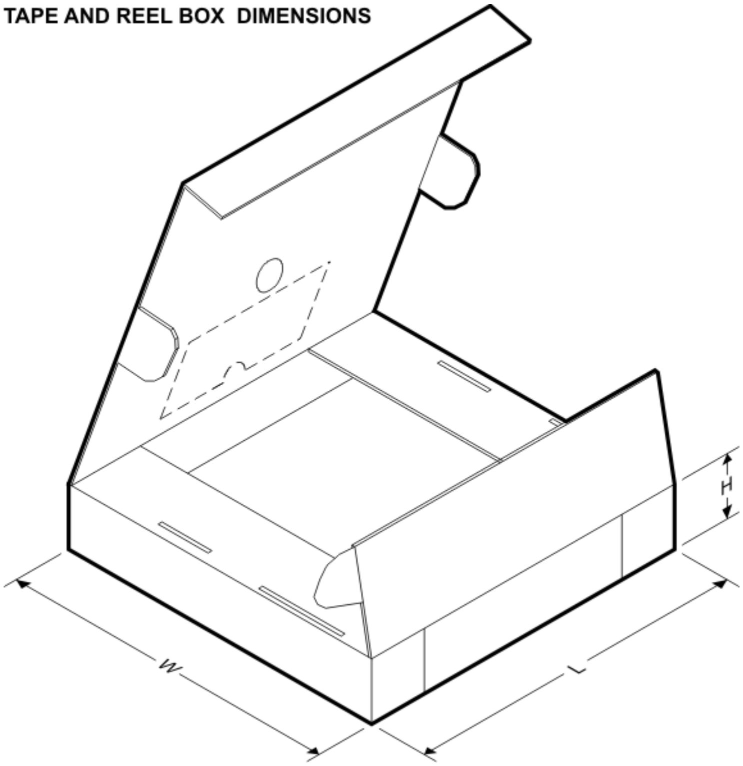
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

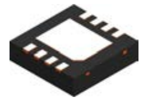
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25BR100TSD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS25BR101TSD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS25BR101TSDE/NOPB	WSON	NGQ	8	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS25BR101TSDX/NOPB	WSON	NGQ	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

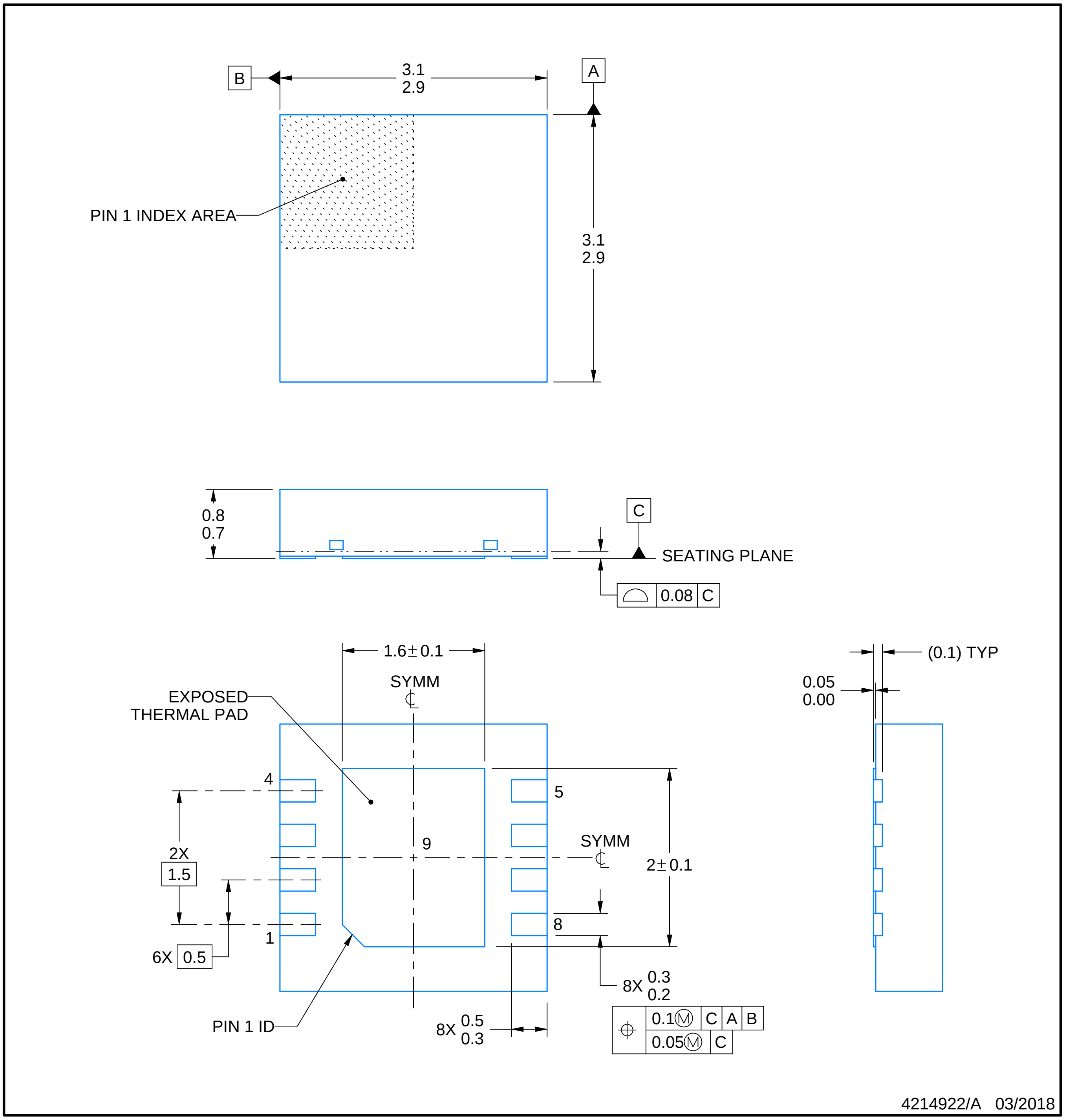
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

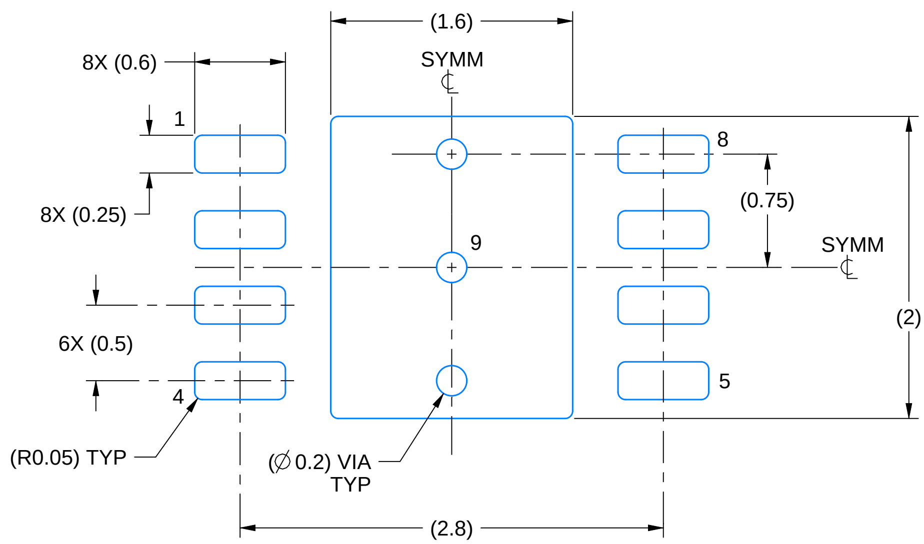
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25BR100TSD/NOPB	WSON	NGQ	8	1000	210.0	185.0	35.0
DS25BR101TSD/NOPB	WSON	NGQ	8	1000	210.0	185.0	35.0
DS25BR101TSDE/NOPB	WSON	NGQ	8	250	210.0	185.0	35.0
DS25BR101TSDX/NOPB	WSON	NGQ	8	4500	367.0	367.0	35.0



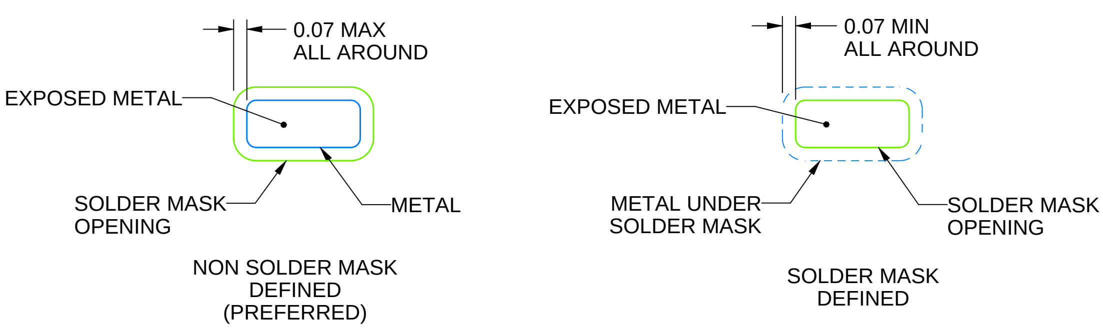


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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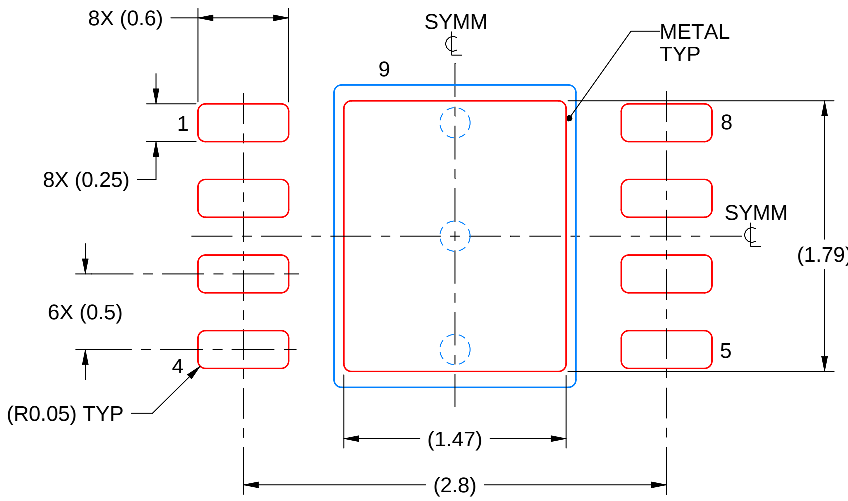
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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