FEATURES

• **Single Power Supply Operation**
- Low voltage range: 2.3 V - 3.6 V

• **Memory Organization**
- Pm25LD040: 512K x 8 (4 Mbit)

• **Cost Effective Sector/Block Architecture**
- 4Mb : Uniform 4KByte sectors / Eight uniform 64KByte blocks

• **Low standby current 1uA (Typ)**
• **Serial Peripheral Interface (SPI) Compatible**
- Supports single- or dual-output
- Supports SPI Modes 0 and 3
- Maximum 33 MHz clock rate for normal read
- Maximum 100 MHz clock rate for fast read

• **Page Program (up to 256 Bytes) Operation**
- Typical 2 ms per page program
• **Sector, Block or Chip Erase Operation**
- Maximum 10ms sector, block or chip erase

• **Low Power Consumption**
- Typical 10 mA active read current
- Typical 15 mA program/erase current

• **Hardware Write Protection**
- Protect and unprotect the device from write operation by Write Protect (WP#) Pin

• **Software Write Protection**
- The Block Protect (BP2, BP1, BP0) bits allow partial or entire memory to be configured as read-only

• **High Product Endurance**
- Guaranteed 200,000 program/erase cycles per single sector
- Minimum 20 years data retention

• **Industrial Standard Pin-out and Package**
- 8-pin 150mil SOIC
- 8-pin 208mil SOIC
- 8-pin 300mil PDIP
- 8-contact WSON
- 8-pin 150mil VVSOP
- Lead-free (Pb-free), halogen-free package

GENERAL DESCRIPTION

The Pm25LD040 are 4Mbit Serial Peripheral Interface (SPI) Flash memories, providing single- or dual-output. The devices are designed to support a 33 MHz clock rate in normal read mode, and 100 MHz in fast read, the fastest in the industry. The devices use a single low voltage power supply, wide operating voltage ranging from 2.3 Volt to 3.6 Volt, to perform read, erase and program operations. The devices can be programmed in standard EPROM programmers.

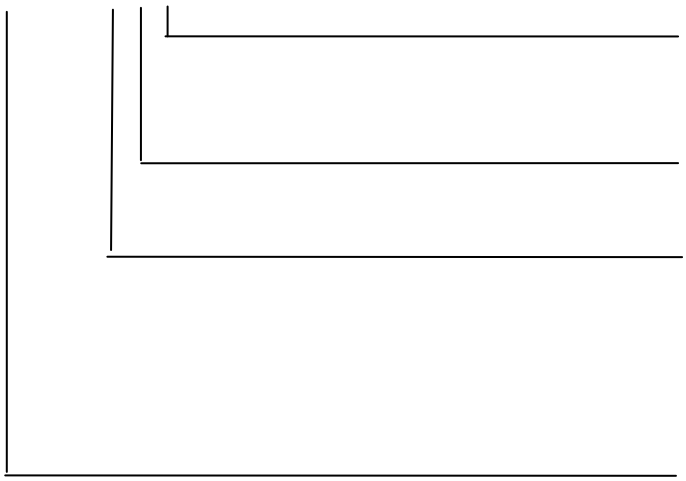
The Pm25LD040 are accessed through a 4-wire SPI Interface consisting of Serial Data Input/Output (SIO), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. They comply with all recognized command codes and operations. The dual-output fast read operation provides and effective serial data rate of 200MHz.

The devices support page program mode, where 1 to 256 bytes data can be programmed into the memory in one program operation. These devices are divided into uniform 4 KByte sectors or uniform 64 KByte blocks.

The Pm25LD040 are manufactured on pFLASH™'s advanced non-volatile technology. The devices are offered in 8-pin SOIC 150mil, 8-contact WSON, 8-pin VVSOP 150mil, 8-pin 208mil SOIC and 8-pin 300mil PDIP. The devices operate at wide temperatures between -40°C to +105°C.

PRODUCT ORDERING INFORMATION

Pm25LDxxx - S C E



Environmental Attribute
E = Lead-free (Pb-free) and Halogen- free package

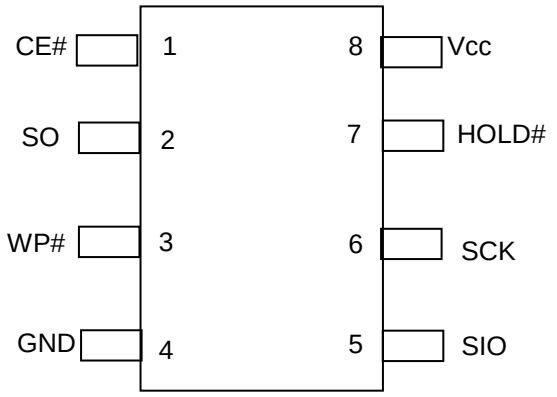
Temperature Range
C = Commercial Grade (-40°C to +105°C)

Package Type
S = 8-pin SOIC 150mil (8S)
B = 8-pin SOIC 208mil (8B)
P = 8-pin PDIP 300 mil (8P)
K = 8-contact WSON (8K)
E= 8-pin VVSOP 150mil (8E)

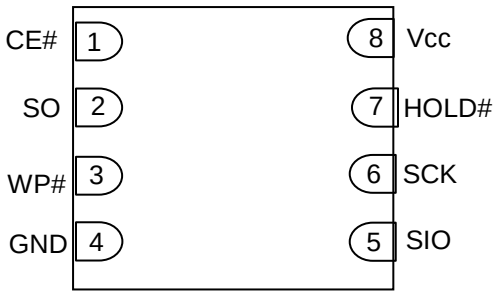
pFlash Device Number
Pm25LD040

Part Number	Operating Frequency (MHz)	Package	Temperature Range
Pm25LD040-SCE	100	8S 150mil SOIC	Commercial Grade (-40°C to +105°C)
Pm25LD040-KCE	100	8K WSON (Back Side Metal)	
Pm25LD040-PCE	100	8P 300mil PDIP	
Pm25LD040-BCE	100	8B 208mil SOIC	
Pm25LD040-ECE	100	8E 150mil VVSOP	

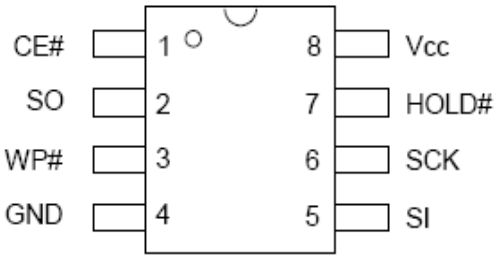
CONNECTION DIAGRAMS



8-Pin SOIC/VVSOP



8-Contact WSON

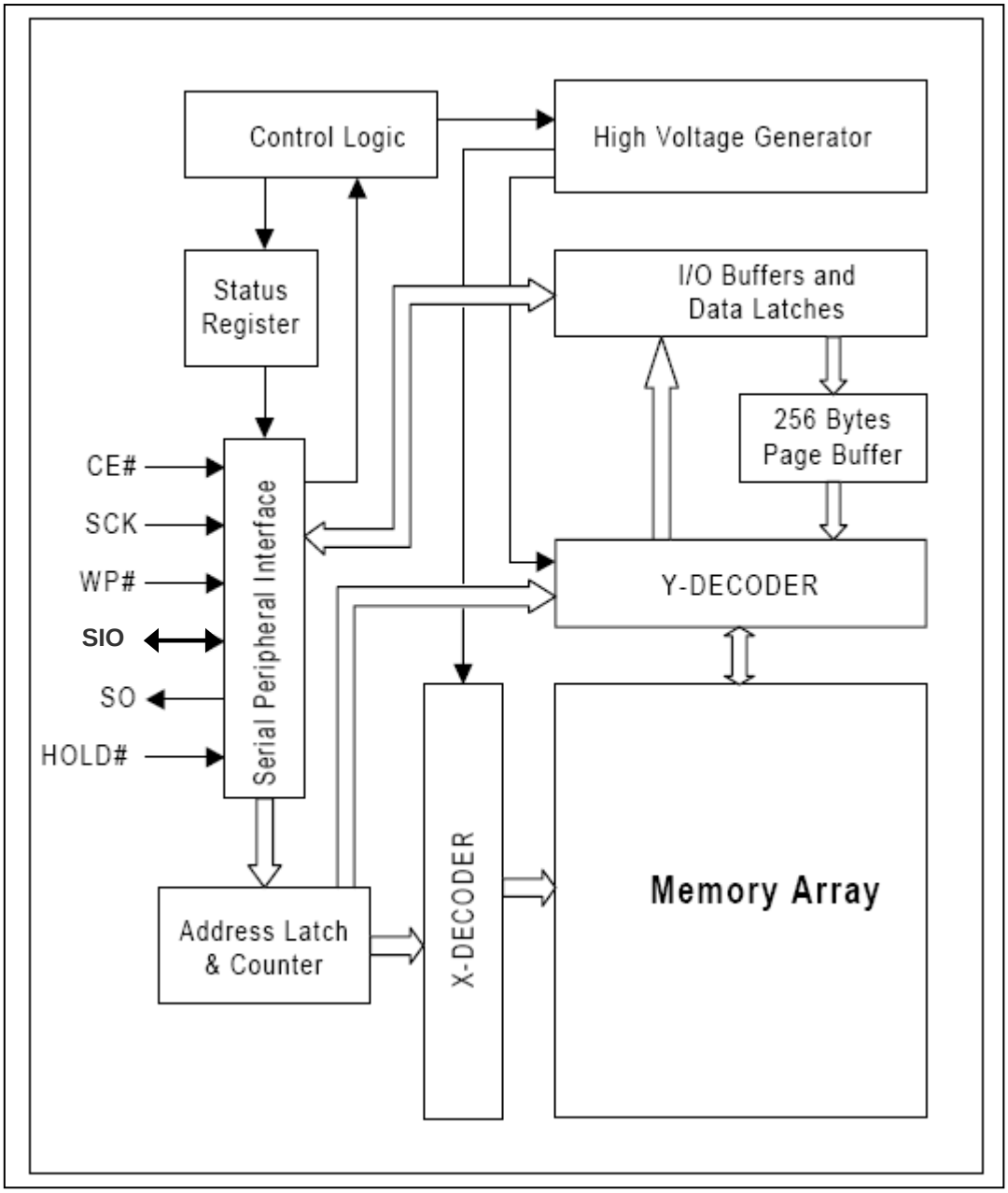


8-Pin PDIP

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Chip Enable: CE# low activates the devices internal circuitries for device operation. CE# high deselects the devices and switches into standby mode to reduce the power consumption. When a device is not selected, data will not be accepted via the serial input pin (SI), and the serial output pin (SO) will remain in a high impedance state.
SCK	INPUT	Serial Data Clock
SIO	INPUT/OUTPUT	Serial Data Input/Output
SO	OUTPUT	Serial Data Output
GND		Ground
Vcc		Device Power Supply
WP#	INPUT	Write Protect: A hardware program/erase protection for all or part of a memory array. When the WP# pin is low, memory array write-protection depends on the setting of BP2, BP1 and BP0 bits in the Status Register. When the WP# is high, the devices are not write-protected.
HOLD#	INPUT	Hold: Pause serial communication by the master device without resetting the serial sequence.

BLOCK DIAGRAM



SPI MODES DESCRIPTION

Multiple Pm25LD040 devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 1. The devices support either of two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

The difference between these two modes is the clock polarity when the SPI master is in Stand-by mode: the serial clock remains at "0" (SCK = 0) for Mode 0 and the clock remains at "1" (SCK = 1) for Mode 3. Please refer to Figure 2. For both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 1. Connection Diagram among SPI Master and SPI Slaves (Memory Devices)

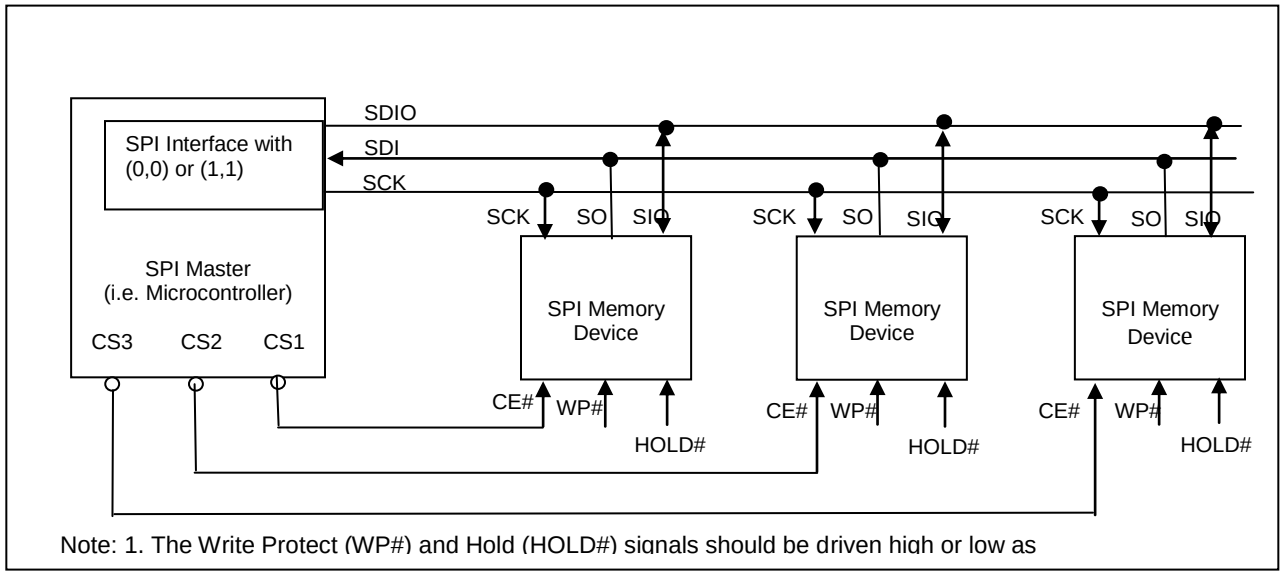
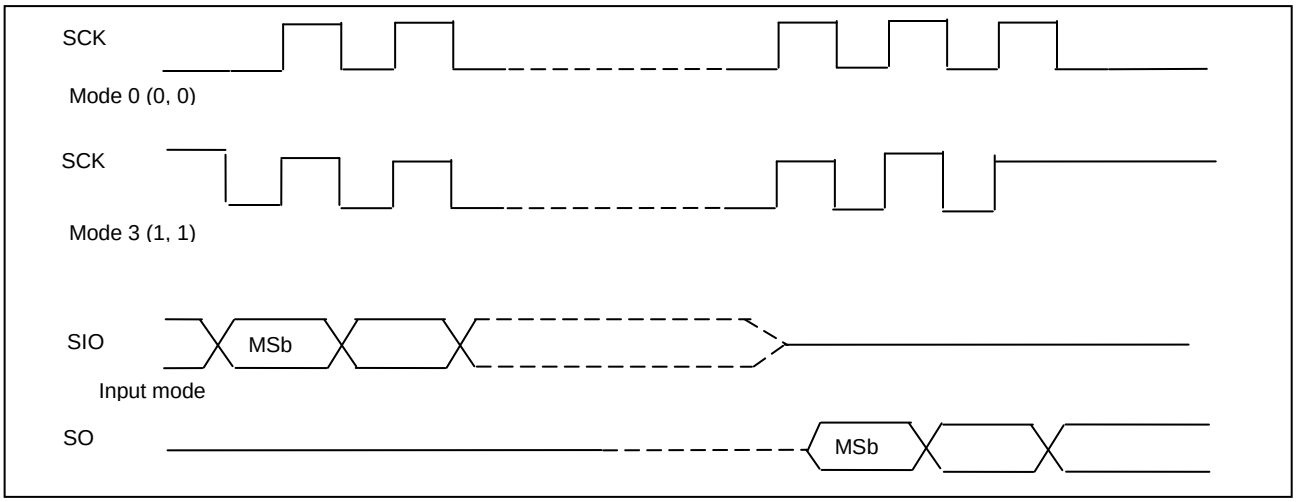


Figure 2. SPI Modes Supported



SYSTEM CONFIGURATION

The Pm25LD040 devices are designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of the Motorola MC68HCxx series of microcontrollers or any SPI interface-equipped system controllers. The devices have two superset features that can be enabled through specific software instructions and the Configuration Register:

Memory Density	Block No.	Block Size (KBytes)	Sector No.	Sector Size (KBytes)	Address Range
4 Mbit	Block 0	64	Sector 0	4	000000h - 000FFFh
			Sector 1	4	001000h - 001FFFh
			:	:	:
			Sector 15	4	00F000h - 00FFFFh
	Block 1	64	Sector 16	4	010000h - 010FFFh
			Sector 17	4	011000h - 011FFFh
			:	:	:
			Sector 31	4	01F000h - 01FFFFh
	:	:	:	:	:
	Block 3	64	:	4	030000h – 03FFFFh
	Block 4	64	:	4	040000h – 04FFFFh
	:	:	:	:	:
	:	:	:	:	:
	Block 7	64	:	4	070000h – 07FFFFh

Table 1. Block/Sector Addresses of Pm25LD040

REGISTERS (CONTINUED)

STATUS REGISTER

Refer to Tables 5 and 6 for Status Register Format and Status Register Bit Definitions.

The BP0, BP1, BP2, and SRWD are volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value of the BP2, BP1, BP0 were set to “0” and SRWD bits was set to “0” at factory. Once a “0” or “1”is written, it will not be changed by device power-up or power-down, and can only be altered by the next WRSR instruction. The Status Register can be read by the Read Status Register (RDSR). Refer to Table 10 for Instruction Set.

The function of Status Register bits are described as follows:

WIP bit: The Write In Progress (WIP) bit is read-only, and can be used to detect the progress or completion of a program or erase operation. When the WIP bit is “0”, the device is ready for a write status register, program or erase operation. When the WIP bit is “1”, the device is busy.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When the WEL is “0”, the write enable latch is disabled, and all write operations, including write status register, page program, sector erase, block and chip erase operations are inhibited. When the WEL bit is “1”, write operations are allowed. The WEL bit is set by a Write Enable (WREN) instruction. Each write register, program and erase instruction must be preceded by a WREN instruction. The WEL bit can be reset by a Write Disable (WRDI) instruction. It will automatically be the reset after the completion of a write instruction.

BP2, BP1, BP0 bits: The Block Protection (BP2, BP1, BP0) bits are used to define the portion of the memory area to be protected. Refer to Tables 7, 8 and 9 for the Block Write Protection bit settings. When a defined combination of BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operation to that area will be inhibited. Note: a Chip Erase (CHIP_ER) instruction is executed successfully only if all the Block Protection Bits are set as “0”s.

SRWD bit: The Status Register Write Disable (SRWD) bit operates in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to “0”, the Status Register is not write-protected. When the SRWD is set to “1” and the WP# is pulled low (V_{IL}), the volatile bits of Status Register (SRWD, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to “1” and WP# is pulled high (V_{IH}), the Status Register can be changed by a WRSR instruction.

Table 5. Status Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SRWD1	Reserved		BP2	BP1	BP0	WEL	WIP
Default (flash bit)	0	0		0	0	0	0	0

REGISTERS (CONTINUED)

Table 6. Status Register Bit Definition

Bit	Name	Definition	Read-/Write	Non-Volatile bit
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready "1" indicates a write cycle is in progress and the device is busy	R	No
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled "1" indicates the device is write enabled (default)	R/W	No
Bit 2	BP0	Block Protection Bit: (See Table 7 and Table 8 for details) "0" indicates the specific blocks are not write-protected (default) "1" indicates the specific blocks are write-protected	R/W	Yes
Bit 3	BP1			
Bit 4	BP2			
Bits 5 - 6	N/A	Reserved: Always "0"s	N/A	
Bit 7	SRWD	Status Register Write Disable: (See Table 9 for details) "0" indicates the Status Register is not write-protected (default) "1" indicates the Status Register is write-protected	R/W	Yes

Table 8. Block Write Protect Bits for Pm25LD040

Status Register Bits			Protected Memory Area
BP2	**BP1**	**BP0**	**4 Mbit**
0	0	0	None
0	0	1	Upper eight (block : 7): 070000h - 07FFFFh
0	1	0	Upper quarter (two blocks :6 and 7): 060000h - 07FFFFh
0	1	1	Upper half (four blocks :4 to 7): 040000h - 07FFFFh
1	0	0	All Blocks (Block 0 to 7): 000000h - 07FFFFh
1	0	1	
1	1	0	
1	1	1	

REGISTERS (CONTINUED)

PROTECTION MODE

The Pm25LD040 have two types of write-protection mechanisms: hardware and software. These are used to prevent irrelevant operation in a possibly noisy environment and protect the data integrity.

HARDWARE WRITE-PROTECTION

The devices provide two hardware write-protection features:

a. When inputting a program, erase or write status register instruction, the number of clock pulse is checked to determine whether it is a multiple of eight before the executing. Any incomplete instruction command sequence will be ignored.

b. The Write Protection (WP#) pin provides a hardware write protection method for BP2, BP1, BP0 and SRWD in the Status Register. Refer to the STATUS REGISTER description.

c. Write inhibit is 1.8V, all write sequence will be ignored when Vcc drop to 1.8V and lower

SOFTWARE WRITE PROTECTION

The Pm25LD040 also provides two software write protection features:

a. Before the execution of any program, erase or write status register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If the WEL bit is not enabled first, the program, erase or write register instruction will be ignored.

b. The Block Protection (BP2, BP1, BP0) bits allow part or the whole memory area to be write-protected.

Table 9. Hardware Write Protection on Status Register

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

DEVICE OPERATION

The Pm25LD040 utilize an 8-bit instruction register. Refer to Table 10 Instruction Set for details of the Instructions and Instruction Codes. All instructions, addresses, and data are shifted in with the most significant bit (MSB) first on Serial Data Input (SIO). The input data on SIO is latched on the rising edge of Serial Clock (SCK) after Chip Enable (CE#) is driven low (V_{IL}). Every instruction sequence starts with a one-byte instruction code and is followed by address bytes, data bytes, or both address bytes and data bytes, depending on the type of instruction. CE# must be driven high (V_{IH}) after the last bit of the instruction sequence has been shifted in.

The timing for each instruction is illustrated in the following operational descriptions.

Table 10. Instruction Set

Instruction Name	Hex Code	Operation	Command Cycle	Maximum Frequency
RDID	ABh	Read Manufacturer and Product ID	4 Bytes	100 MHz
JEDEC ID READ	9Fh	Read Manufacturer and Product ID by JEDEC ID Command	1 Byte	100 MHz
RDMDID	90h	Read Manufacturer and Device ID	4 Bytes	100 MHz
WREN	06h	Write Enable	1 Byte	100 MHz
WRDI	04h	Write Disable	1 Byte	100 MHz
RDSR	05h	Read Status Register	1 Byte	100 MHz
WRSR	01h	Write Status Register	2 Bytes	100 MHz
READ	03h	Read Data Bytes from Memory at Normal Read Mode	4 Bytes	33 MHz
FAST_READ	0Bh	Read Data Bytes from Memory at Fast Read Mode	5 Bytes	100 MHz
FRDO	3Bh	Fast Read Dual Output	5 Bytes	100 MHz
PAGE_ PROG	02h	Page Program Data Bytes Into Memory	4 Bytes + 256B	100 MHz
SECTOR_ER	D7h/ 20h	Sector Erase	4 Bytes	100 MHz
BLOCK_ER	D8h	Block Erase	4 Bytes	100 MHz
CHIP_ER	C7h/ 60h	Chip Erase	1 Byte	100 MHz

HOLD OPERATION

HOLD# is used in conjunction with CE# to select the Pm25LD040. When the devices are selected and a serial sequence is underway, HOLD# can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, HOLD# is brought low while the SCK signal is low. To resume serial communication, HOLD# is brought high while the SCK signal is low (SCK may still toggle during HOLD). Inputs to Sl will be ignored while SO is in the high impedance state.

DEVICE OPERATION (CONTINUED)

RDID COMMAND (READ PRODUCT IDENTIFICATION) OPERATION

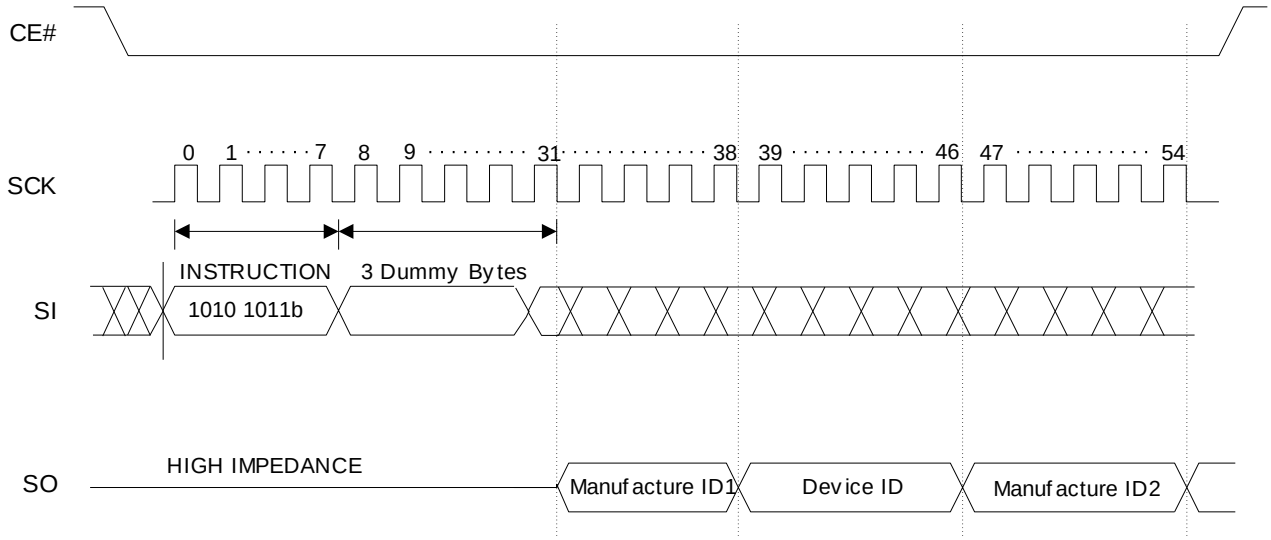
The Read Product Identification (RDID) instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not same as RDID or JEDEC ID instruction. It's not recommended to use for new design. For new design, please use RDID or JEDEC ID instruction.

The RDID instruction code is followed by three dummy bytes, each bit being latched-in on SIO during the rising edge of SCK. Then the first manufacturer ID (9Dh) is shifted out on SO with the MSB first, followed by the device ID and the second manufacturer ID (7Fh), each bit been shifted out during the falling edge of SCK. If the CE# stays low after the last bit of second manufacturer ID is shifted out, the manufacturer ID and device ID will be looping until the pulled high of CE# signal.

Table 11. Product Identification

Product Identification		Data
Manufacturer ID	First Byte	9Dh
	Second Byte	7Fh
Device ID:		
Pm25LD040		7E

Figure 3. Read Product Identification Sequence

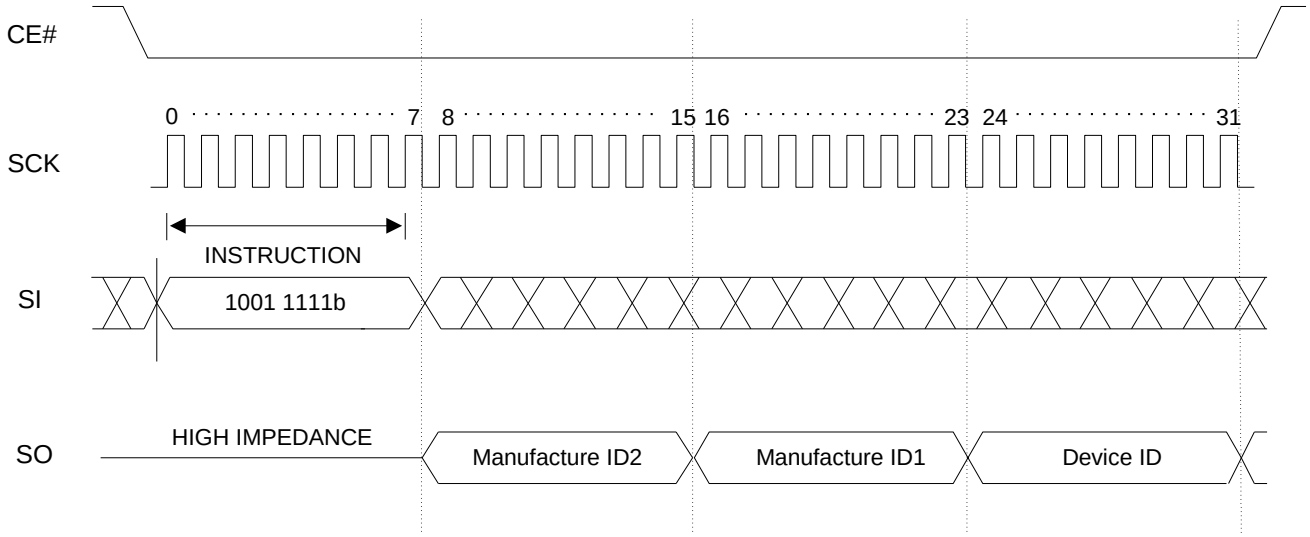


DEVICE OPERATION (CONTINUED)

JEDEC ID READ COMMAND (READ PRODUCT IDENTIFICATION BY JEDEC ID) OPERATION

The JEDEC ID READ instruction allows the user to read the manufacturer and product ID of devices. Refer to Table 11 Product Identification for pFlash Manufacturer ID and Device ID. After the JEDEC ID READ command is input, the second Manufacturer ID (7Fh) is shifted out on SO with the MSB first, followed by the first Manufacturer ID (9Dh) and the Device ID, each bit shifted out during the falling edge of SCK. If CE# stays low after the last bit of the Device ID is shifted out, the Manufacturer ID and Device ID will loop until CE# is pulled high.

Figure 4. Read Product Identification by JEDEC ID READ Sequence

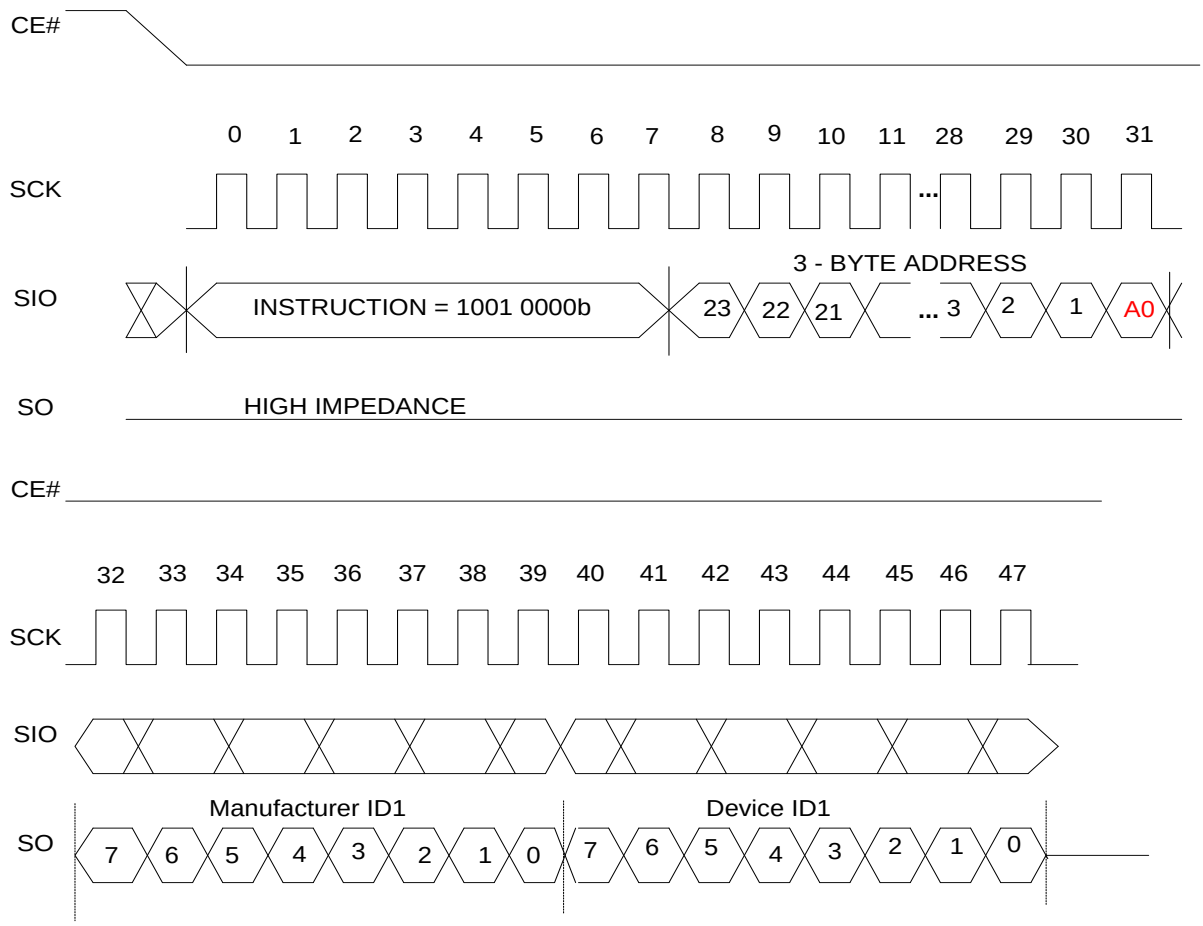


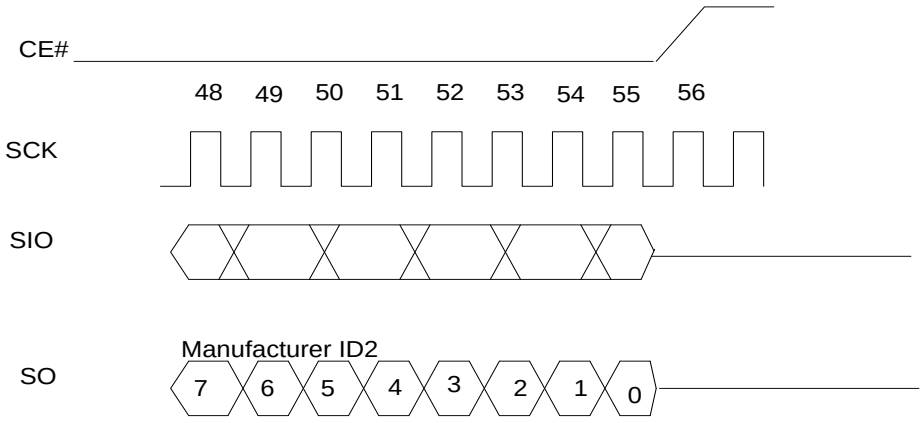
DEVICE OPERATION (CONTINUED)

RDMDID COMMAND (READ DEVICE MANUFACTURER AND DEVICE ID) OPERATION

The RDMDID instruction allows the user to read the manufacturer and product ID of devices. Refer to Table 11 Product Identification for pFlash Manufacturer ID and Device ID. The RDMDID command is input, followed by a 24-bit address pointing to an ID table. The table contains the first Manufacturer ID (9Dh) and the Device ID, and is shifted out on SO with the MSB first, each bit shifted out during the falling edge of SCK. If CE# stays low after the last bit of the Device ID is shifted out, the Manufacturer ID and Device ID will loop until CE# is pulled high.

Figure 5. Read Product Identification by RDMDID READ Sequence





Note :

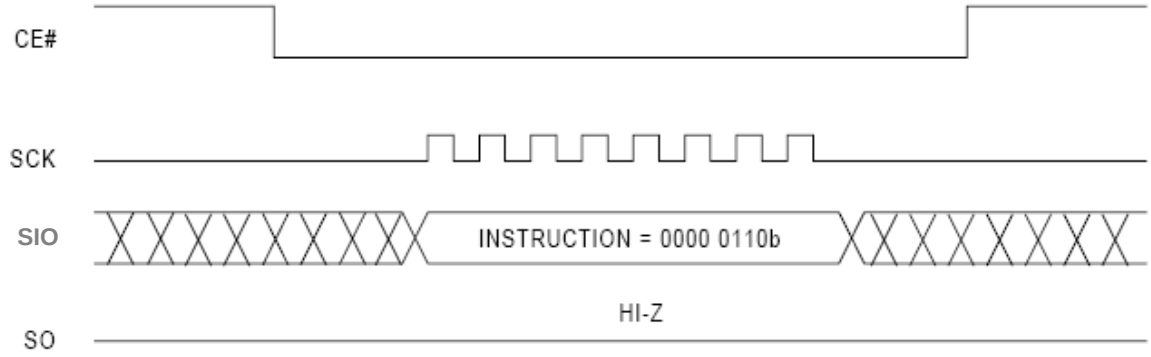
(1) ADDRESS A0 = 0, will output the 1st manufacture ID (9Dh) first -> device ID1 -> 2nd manufacture ID (7Fh)
ADDRESS A0 = 1, will output the device ID1 -> 1st manufacture ID (9D) -> 2nd manufacture ID (7Fh)

DEVICE OPERATION (CONTINUED)

WRITE ENABLE OPERATION

The Write Enable (WREN) instruction is used to set the Write Enable Latch (WEL) bit. The WEL bit of the Pm25LD040 is reset to the write –protected state after power-up. The WEL bit must be write enabled before any write operation, including sector, block erase, chip erase, page program and write status register operations. The WEL bit will be reset to the write-protect state automatically upon completion of a write operation. The WREN instruction is required before any above operation is executed.

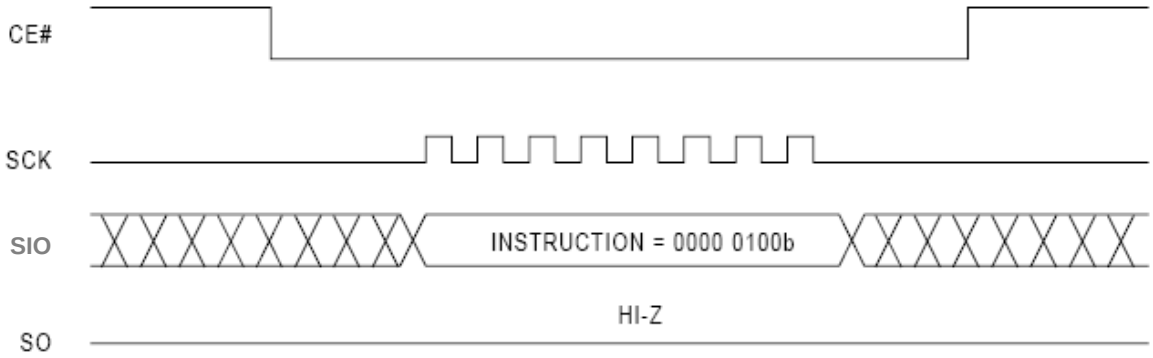
Figure 6. Write Enable Sequence



WRDI COMMAND (WRITE DISABLE) OPERATION

The Write Disable (WRDI) instruction resets the WEL bit and disables all write instructions. The WRDI instruction is not required after the execution of a write instruction, since the WEL bit is automatically reset.

Figure 7. Write Disable Sequence

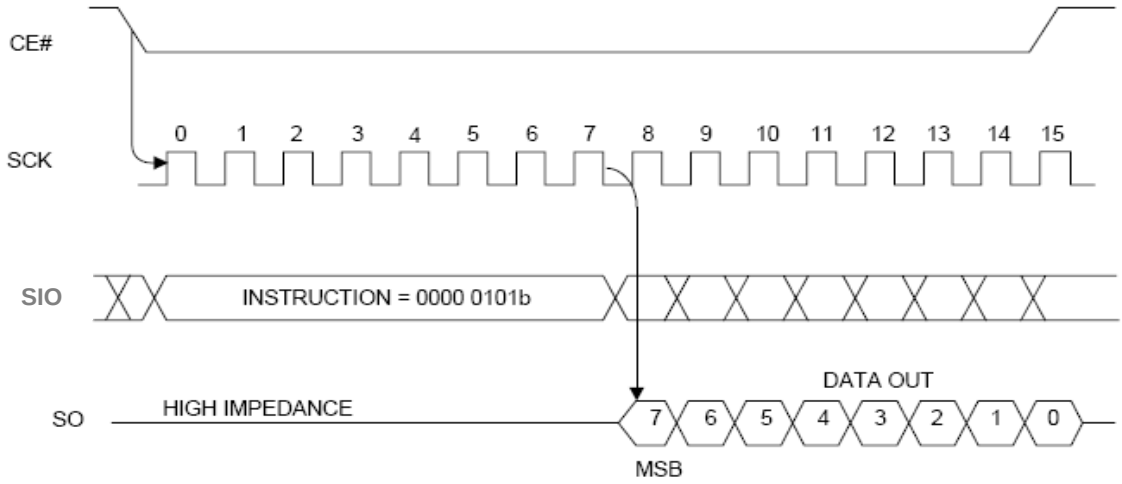


DEVICE OPERATION (CONTINUED)

RDSR COMMAND (READ STATUS REGISTER) OPERATION

The Read Status Register (RDSR) instruction provides access to the Status Register. During the execution of a program, erase or write status register operation, all other instructions will be ignored except the RDSR instruction, which can be used to check the progress or completion of an operation by reading the WIP bit of Status Register.

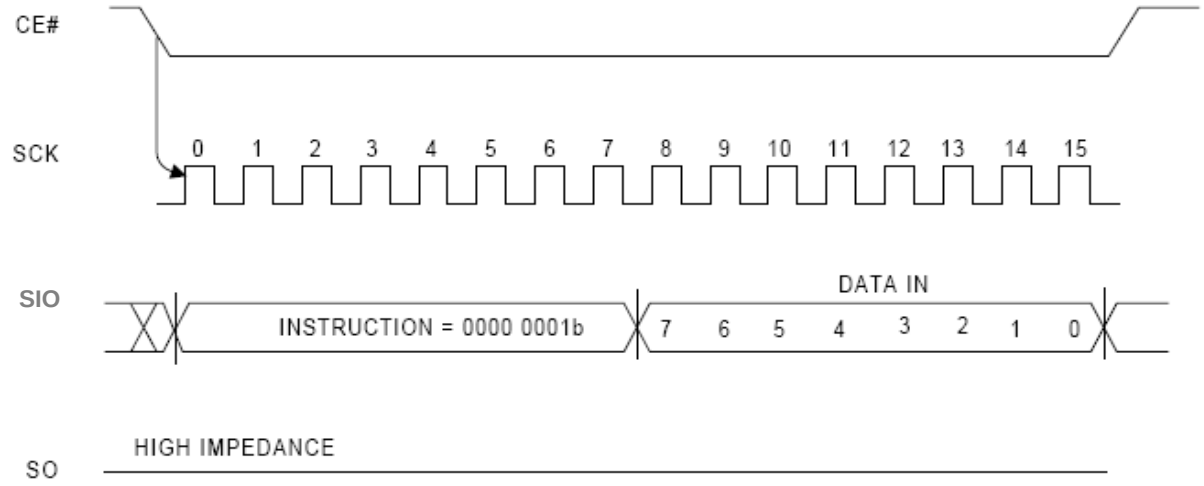
Figure 8. Read Status Register Sequence



WRSR COMMAND (WRITE STATUS REGISTER) OPERATION

The Write Status Register (WRSR) instruction allows the user to enable or disable the block protection and status register write protection features by writing “0”s or “1” s into the volatile BP2, BP1, BP0 and SRWD bits.

Figure 9. Write Status Register Sequence



READ COMMAND (READ DATA) OPERATION

The Read Data (READ) instruction is used to read memory data of a Pm25LD040 under normal mode running up to 33 MHz.

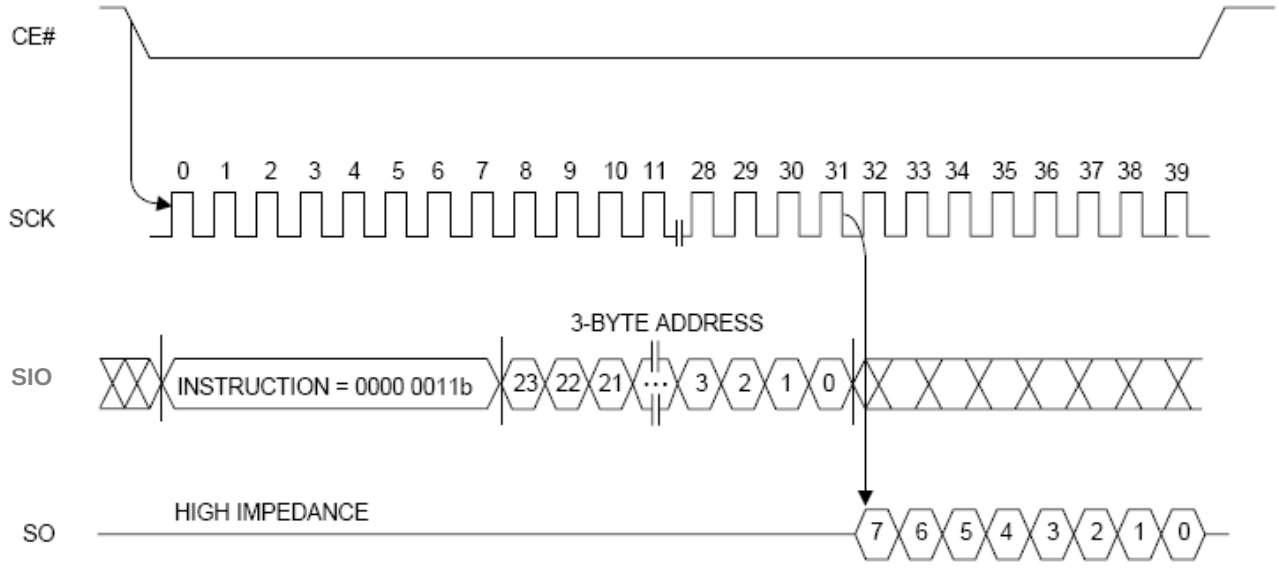
The READ instruction code is transmitted via the SI line, followed by three address bytes (A23 - A0) of the first memory location to be read. A total of 24 address bits are shifted in, but only A_{MS} (most significant address) - A0 are decoded. The remaining bits (A23 – A_{MS}) are ignored. The first byte addressed can be at any memory location. Upon completion, any data on the SI will be ignored. Refer to Table 12 for the related Address Key.

The first byte data (D7 - D0) addressed is then shifted out on the SO line, MSb first. A single byte of data, or up to the whole memory array, can be read out in one READ instruction. The address is automatically incremented after each byte of data is shifted out. The read operation can be terminated at any time by driving CE# high (V_{IH}) after the data comes out. When the highest address of the devices is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read in one continuous READ instruction.

Table 12. Address Key

Address	Pm25LD040
A_N (A_{MS} – A_0)	A18 - A0
Don't Care Bits	A23 – A19

Figure 12. Read Data Sequence



DEVICE OPERATION (CONTINUED)

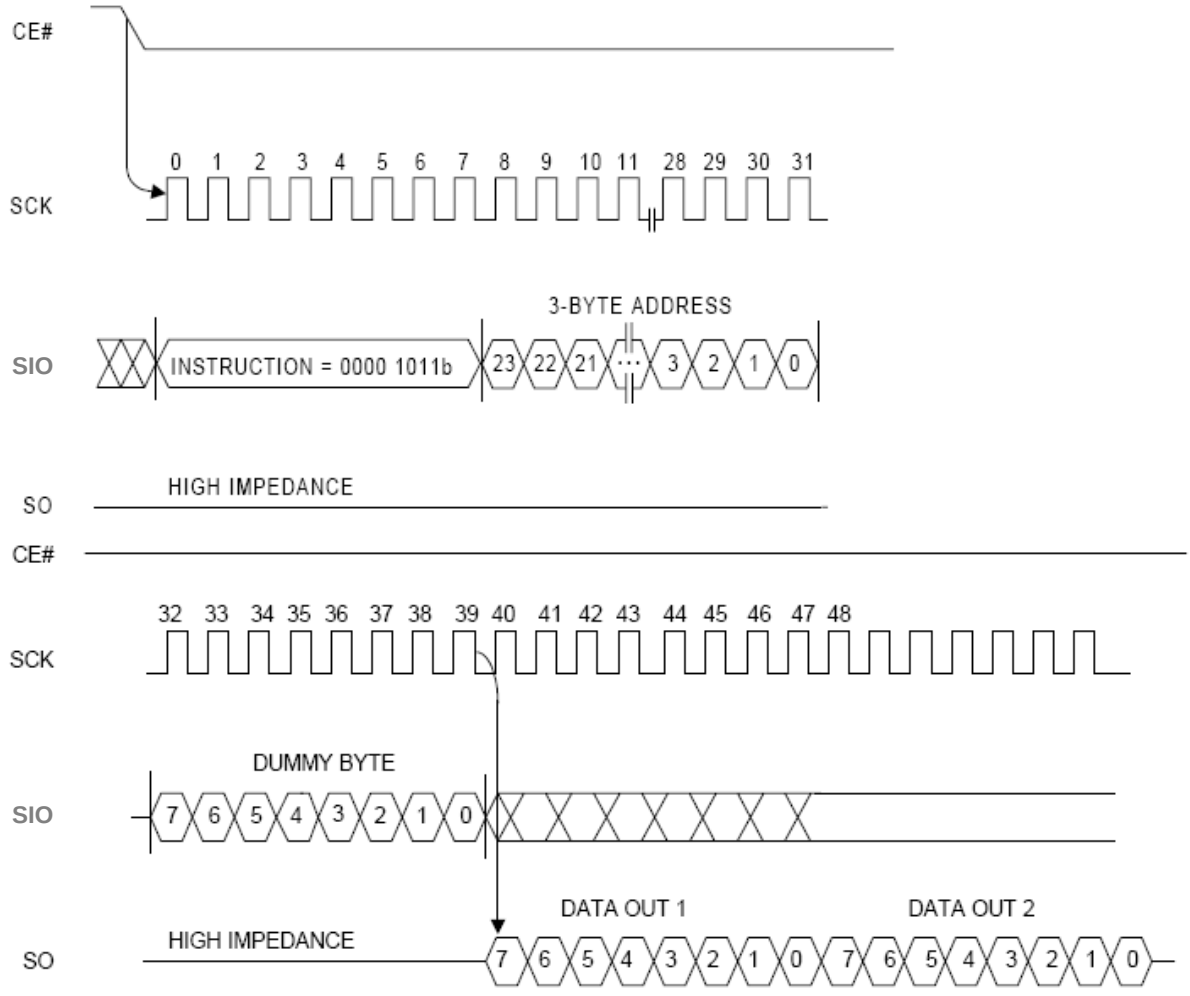
FAST_READ COMMAND (FAST READ DATA) OPERATION

The FAST_READ instruction is used to read memory data at up to a 100 MHz clock.

The FAST_READ instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SIO line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO line, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FAST_READ instruction. The FAST_READ instruction is terminated by driving CE# high (V_{IH}).

Figure 13. Fast Read Data Sequence



DEVICE OPERATION (CONTINUED)

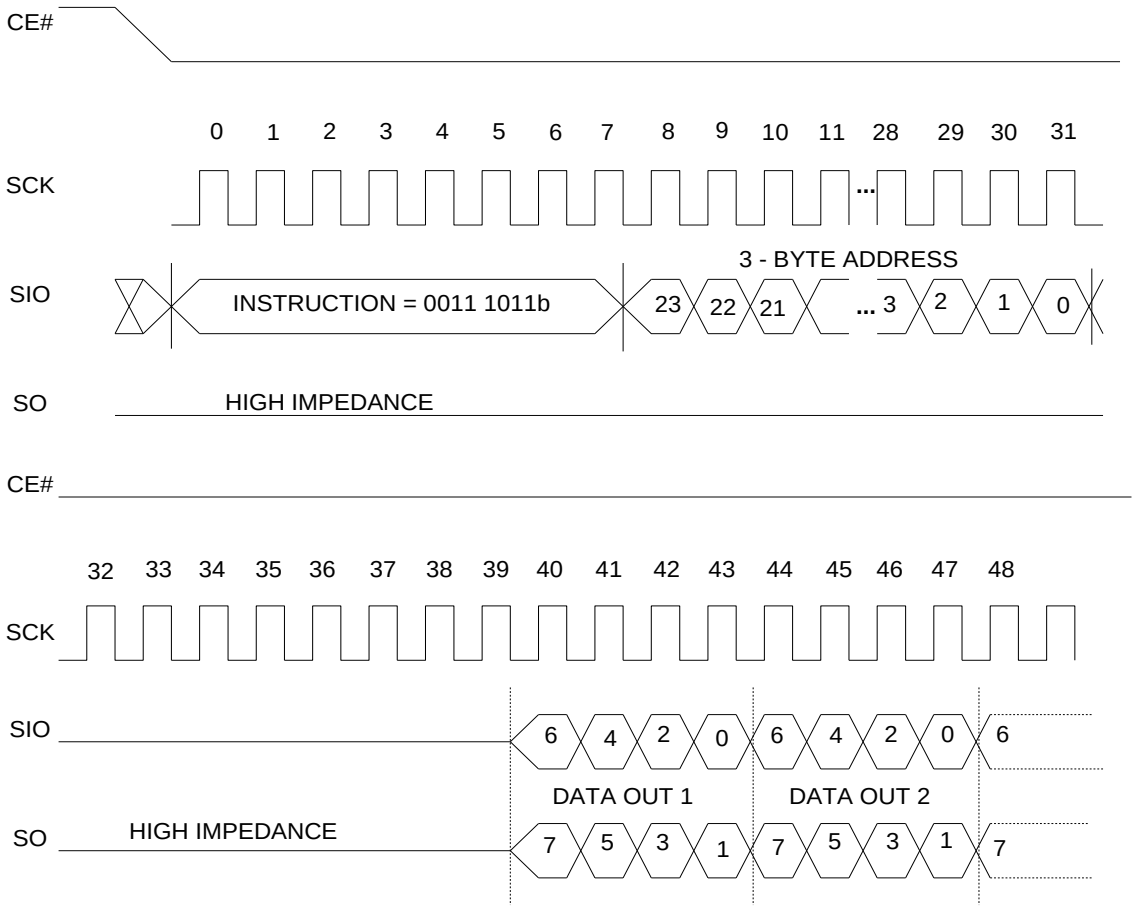
FRDO COMMAND (FAST READ DUAL OUTPUT) OPERATION

The FRDO instruction is used to read memory data on two output pins each at up to a 100 MHz clock.

The FRDO instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SIO line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO and SIO lines, with each pair of bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The first bit (MSb) is output on SO, while simultaneously the second bit is output on SIO.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDO instruction. FRDO instruction is terminated by driving CE# high (V_{IH}).

Figure 14. Fast Read Dual-Output Sequence



DEVICE OPERATION (CONTINUED)

PAGE_PROG COMMAND (PAGE PROGRAM) OPERATION

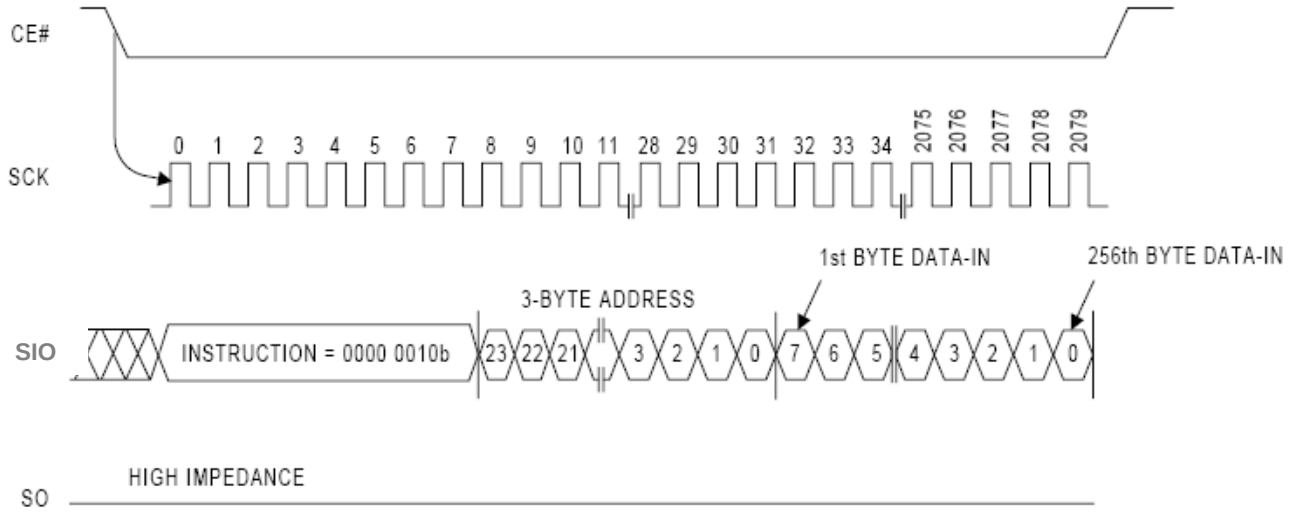
The Page Program (PAGE_PROG) instruction allows up to 256 bytes data to be programmed into memory in a single operation. The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP2, BP1, BP0) bits. A PAGE_PROG instruction which attempts to program into a page that is write-protected will be ignored. Before the execution of PAGE_PROG instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The PAGE_PROG instruction code, three address bytes and program data (1 to 256 bytes) are input via the SI line. Program operation will start immediately after the CE# is brought high, otherwise the PAGE_PROG instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. During a program operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is “1”, the program operation is still in progress. If WIP bit is “0”, the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page, the previously latched data are discarded, and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

Note: A program operation can alter “1”s into “0”s, but an erase operation is required to change “0”s back to “1”s. A byte cannot be reprogrammed without first erasing the whole sector or block.

Figure 15. Page Program Sequence



DEVICE OPERATION (CONTINUED)

ERASE OPERATION

The memory array of the Pm25LD040 is organized into uniform 4 KByte sectors or 64 KByte uniform blocks (a block consists of sixteen adjacent sectors).

Before a byte can be reprogrammed, the sector or block that contains the byte must be erased (erasing sets bits to “1”). In order to erase the devices, there are three erase instructions available: Sector Erase (SECTOR_ER), Block Erase (BLOCK_ER) and Chip Erase (CHIP_ER). A sector erase operation allows any individual sector to be erased without affecting the data in other sectors. A block erase operation erases any individual block. A chip erase operation erases the whole memory array of a device. A sector erase, block erase or chip erase operation can be executed prior to any programming operation.

SECTOR_ER COMMAND (SECTOR ERASE) OPERATION

A SECTOR_ER instruction erases a 4 KByte sector Before the execution of a SECTOR_ER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL bit is reset automatically after the completion of sector an erase operation.

A SECTOR_ER instruction is entered, after CE# is pulled low to select the device and stays low during the entire instruction sequence The SECTOR_ER instruction code, and three address bytes are input via SIO. Erase operation will start immediately after CE# is pulled high. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 14 for Sector Erase Sequence.

During an erase operation, all instruction will be ignored except the Read Status Register (RDSR) instruction. The progress or completion of the erase operation can be determined by reading the WIP bit in the Status Register using a RDSR instruction. If the WIP bit is “1”, the erase operation is still in progress. If the WIP bit is “0”, the erase operation has been completed.

BLOCK_ER COMMAND (BLOCK ERASE) OPERATION

A Block Erase (BLOCK_ER) instruction erases a 64 KByte block of the Pm25LD040. Before the execution of a BLOCK_ER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after the completion of a block erase operation.

The BLOCK_ER instruction code and three address bytes are input via SIO. Erase operation will start immediately after the CE# is pulled high, otherwise the BLOCK_ER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 15 for Block Erase Sequence.

CHIP_ER COMMAND (CHIP ERASE) OPERATION

A Chip Erase (CHIP_ER) instruction erases the entire memory array of a Pm25LD040. Before the execution of CHIP_ER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after completion of a chip erase operation.

The CHIP_ER instruction code is input via the SIO. Erase operation will start immediately after CE# is pulled high, otherwise the CHIP_ER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 16 for Chip Erase Sequence.

DEVICE OPERATION (CONTINUED)

Figure 16. Sector Erase Sequence

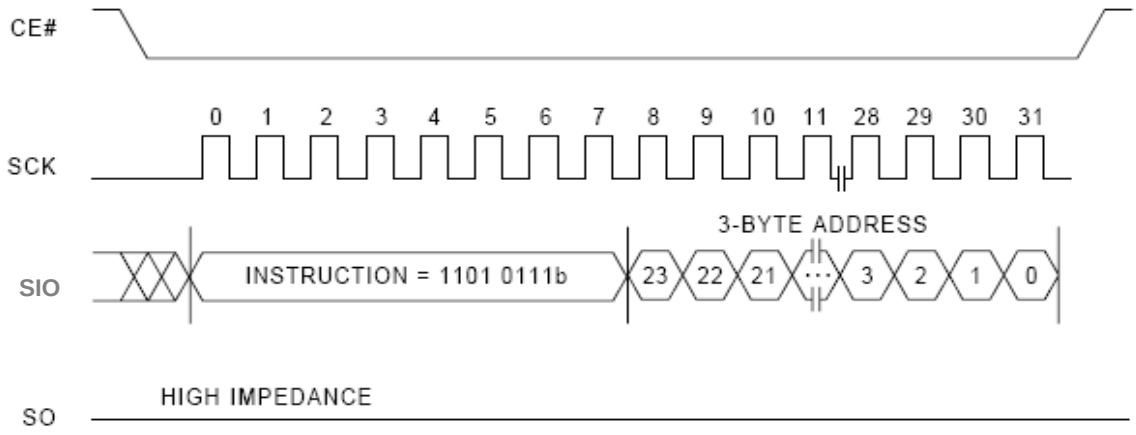


Figure 17. Block Erase Sequence

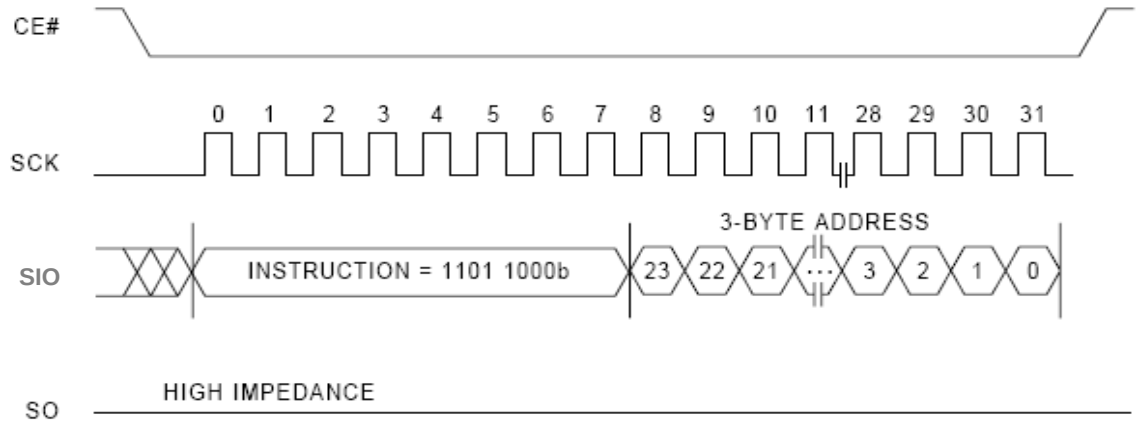
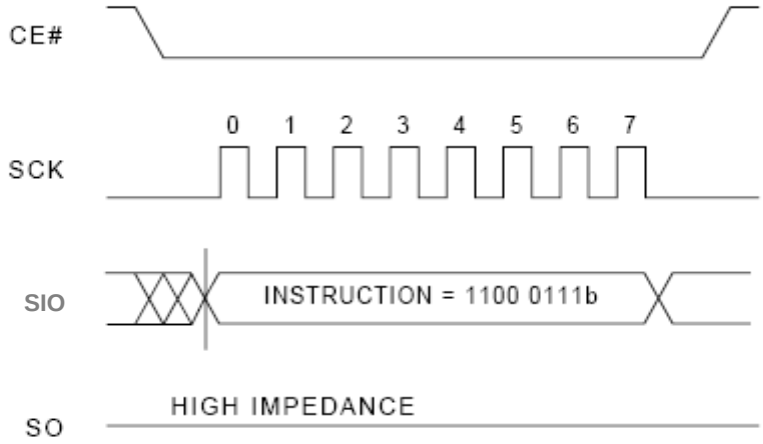


Figure 18. Chip Erase Sequence



ABSOLUTE MAXIMUM RATINGS (1)

Temperature Under Bias		-65°C to +125°C
Storage Temperature		-65°C to +125°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins (2)		-0.5 V to VCC + 0.5 V
All Output Voltage with Respect to Ground		-0.5 V to VCC + 0.5 V
VCC (2)		-0.5 V to +6.0 V

Notes:
1. Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. The functional operation of the device conditions that exceed those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

2. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot V_{CC} by + 2.0 V for a period of time not to exceed 20 ns. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may undershoot GND by -2.0 V for a period of time not to exceed 20 ns.

DC AND AC OPERATING RANGE

Part Number	**Pm25LD040**
Operating Temperature (Commercial Grade)	-40°C to105°C
Vcc Power Supply	2.3 V - 3.6 V

DC CHARACTERISTICS

Applicable over recommended operating range from:
T_{AC} = -40°C to +105°C, V_{CC} = 2.3 V to 3.6 V (unless otherwise noted).

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC1}	Vcc Active Read Current	V_{CC} = 3.6V at 33 MHz, SO = Open			10	15	mA
I_{CC2}	Vcc Program/Erase Current	V_{CC} = 3.6V at 33 MHz, SO = Open			15	30	mA
I_{SB1}	Vcc Standby Current CMOS	V_{CC} = 3.6V, CE# = V_{CC}				10	µA
I_{SB2}	Vcc Standby Current TTL	V_{CC} = 3.6V, CE# = V_{IH} to V_{CC}				3	mA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}				1	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 85°C				1	µA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input HIgh Voltage			0.7V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	2.3V < V_{CC} < 3.6V	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2			V

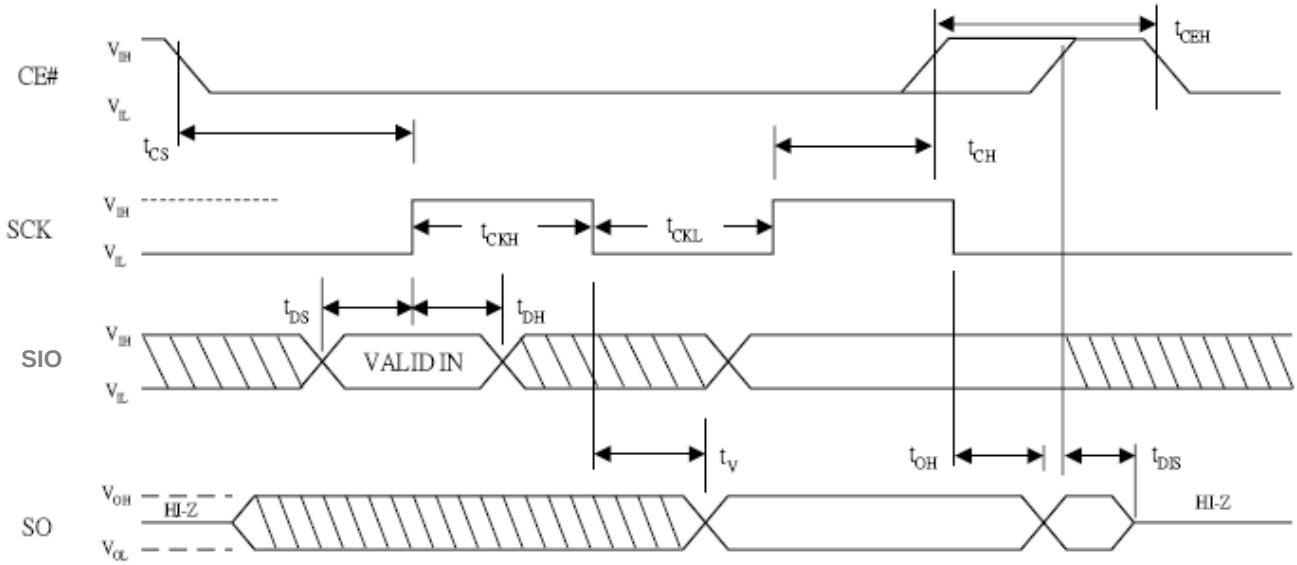
AC CHARACTERISTICS

Applicable over recommended operating range from T_A = -40°C to +105°C, V_{CC} = 2.3 V to 3.6 V
C_L = 1 TTL Gate and 10 pF (unless otherwise noted).

Symbol	Parameter	Min	Typ	Max	Units
f_{CT}	Clock Frequency for fast read mode	0		100	MHz
f_C	Clock Frequency for read mode	0		33	MHz
t_{RI}	Input Rise Time			8	ns
t_{FI}	Input Fall Time			8	ns
t_{CKH}	SCK High Time	4			ns
t_{CKL}	SCK Low Time	4			ns
t_{CEH}	CE# High Time	25			ns
t_{CS}	CE# Setup Time	10			ns
t_{CH}	CE# Hold Time	5			ns
t_{DS}	Data In Setup Time	2			ns
t_{DH}	Data in Hold Time	2			ns
t_{HS}	Hold Setup Time	15			ns
t_{HD}	Hold Time	15			ns
t_V	Output Valid			8	ns
t_{OH}	Output Hold Time Normal Mode	0			ns
t_{LZ}	Hold to Output Low Z			200	ns
t_{HZ}	Hold to Output High Z			200	ns
t_{DIS}	Output Disable Time			100	ns
t_{EC}	Secter/Block/Chip Erase Time			10	ms
t_{PP}	Page Program Time		2	5	ms
t_{VCS}	V_{CC} Set-up Time	50			μs
t_W	Write Status Register time (flash bit)			10	ms

AC CHARACTERISTICS (CONTINUED)

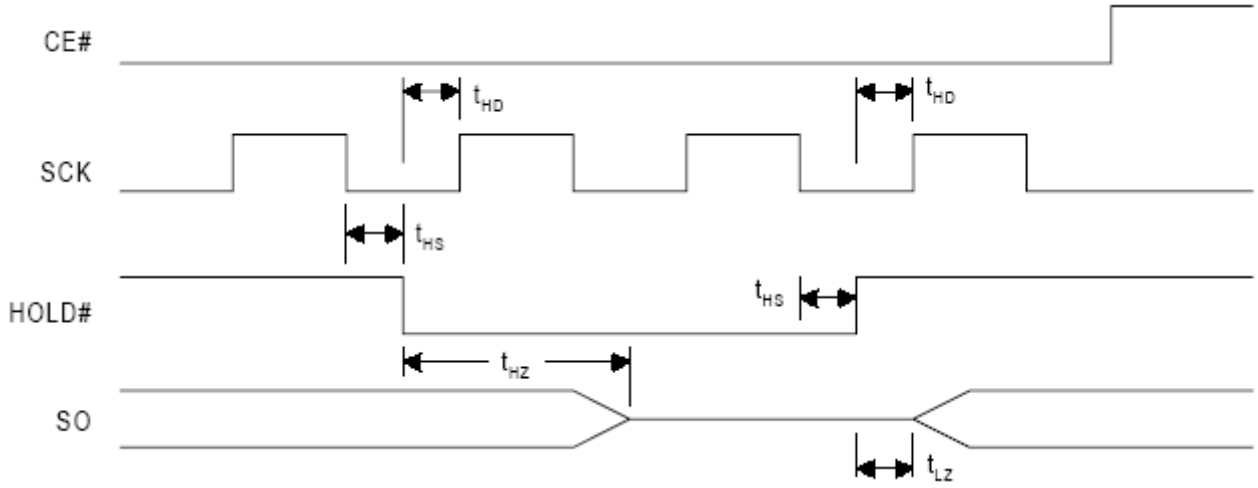
SERIAL INPUT/OUTPUT TIMING (1)



Note: 1. For SPI Mode 0 (0,0)

AC CHARACTERISTICS (CONTINUED)

HOLD TIMING

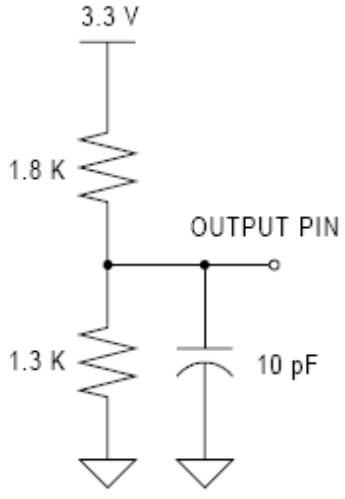


PIN CAPACITANCE (f = 1 MHz, T = 25°C)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: These parameters are characterized but not 100% tested.

OUTPUT TEST LOAD



INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

Note: 1. Input Pulse Voltage : 0.2Vcc to 0.8Vcc.
2. Input Timing Reference Voltages :
0.3Vcc to 0.7Vcc.
3. Output Timing Reference Voltage : Vcc/2.

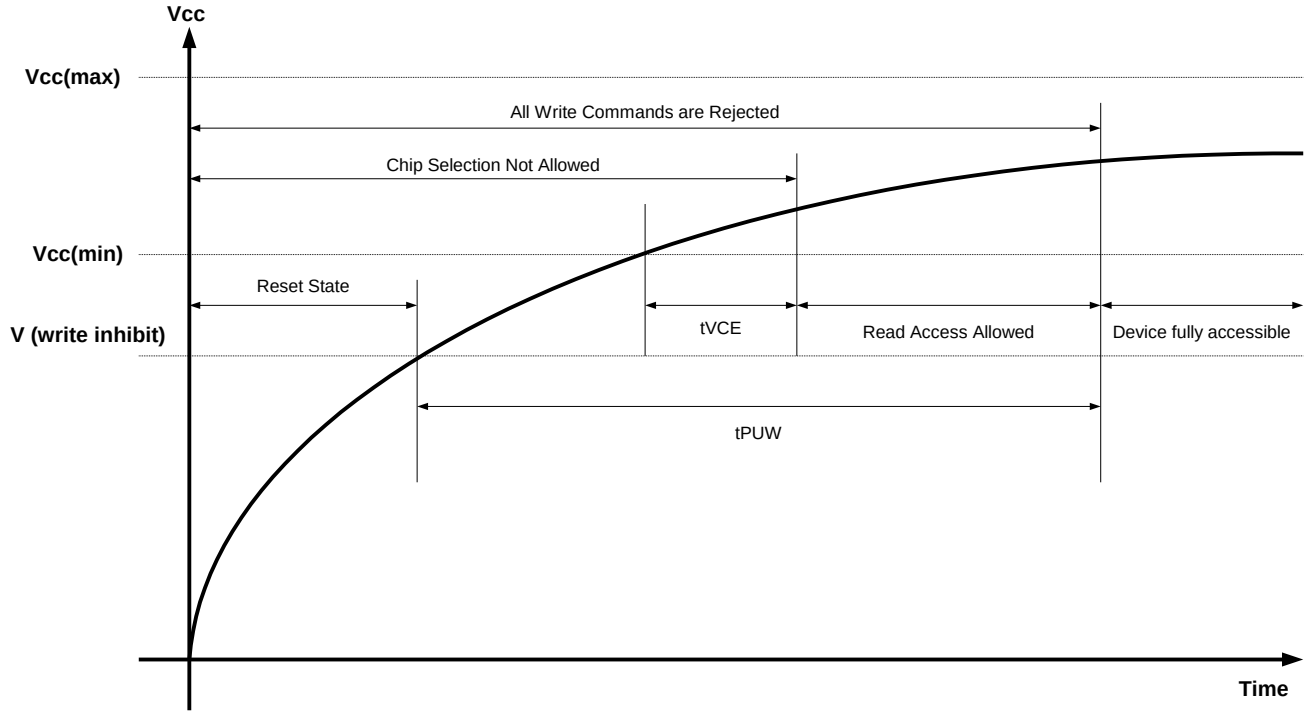
POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must not be selected (CE# must follow the voltage applied on Vcc) until Vcc reaches the correct value:
- Vcc(min) at Power-up, and then for a further delay of tVCE
- Vss at Power-down

Usually a simple pull-up resistor on CE# can be used to insure safe and proper Power-up and Power-down. To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while Vcc is less than the POR threshold value (Vwi) during power up, the device does not respond to any instruction until a time delay of tPUW has elapsed after the moment that Vcc rised above the VWI threshold. However, the correct operation of the device is not guaranteed if, by this time, Vcc is still below Vcc(min). No Write Status Register, Program or Erase instructions should be sent until the later of:
- tPUW after Vcc passed the VWI threshold
- tVCE after Vcc passed the Vcc(min) level

At Power-up, the device is in the following state:
- The device is in the Standby mode
- The Write Enable Latch (WEL) bit is reset

At Power-down, when Vcc drops from the operating voltage, to below the Vwi, all write operations are disabled
and the device does not respond to any write instruction.



Symbol	Parameter	Min.	Max.	Unit
t_{VCE} *1	Vcc(min) to CE# Low	10		us
t_{PUW} *1	Power-Up time delay to Write instruction	1	10	ms
V_{WI} *1	Write Inhibit Voltage	1.6	1.8	V
Note : *1. These parameters are characterized only.				

PROGRAM/ERASE PERFORMANCE

Parameter	Unit	Typ	Max	Remarks
Sector Erase Time	ms		10	From writing erase command to erase completion
Block Erase Time	ms		10	From writing erase command to erase completion
Chip Erase Time	ms		10	From writing erase command to erase completion
Page Programming Time	ms	2	5	From writing program command to program completion

Note: These parameters are characterized and are not 100% tested.

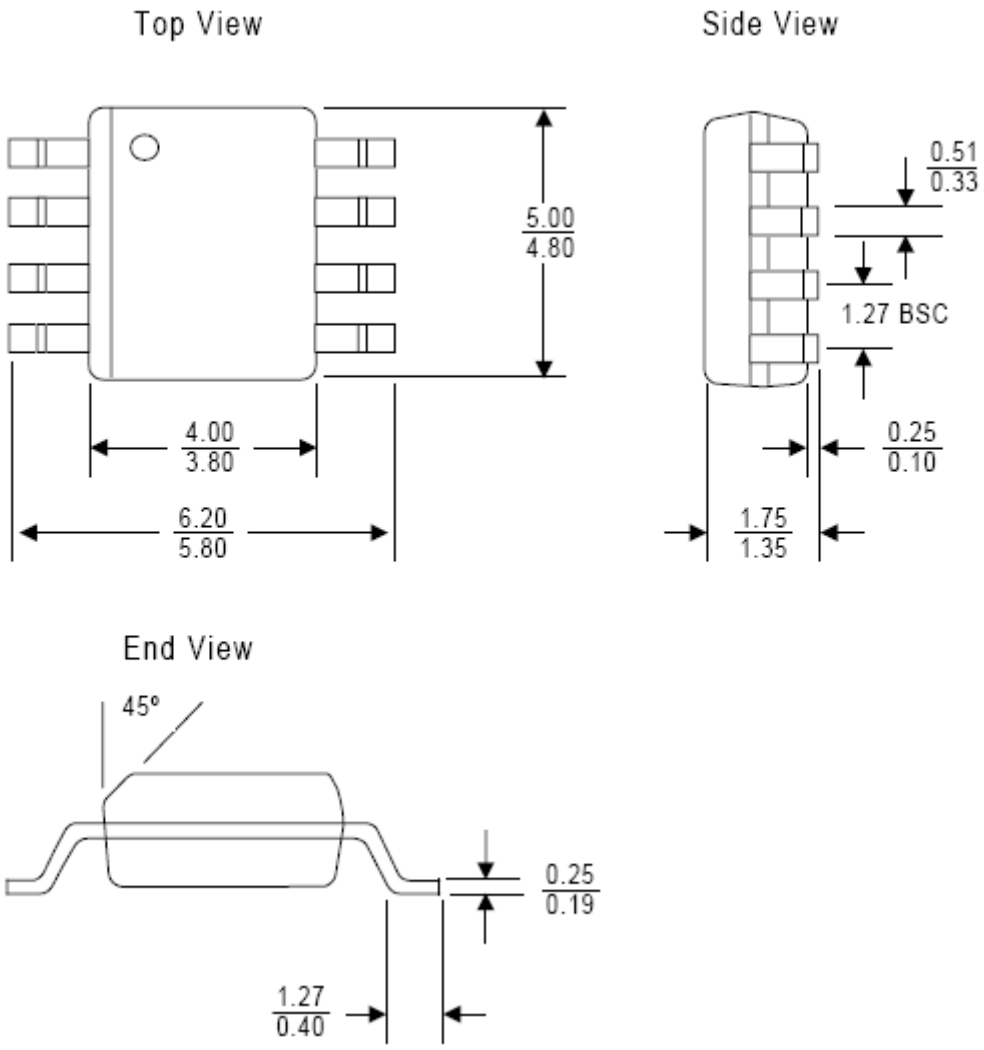
RELIABILITY CHARACTERISTICS

Parameter	Min	Typ	Unit	Test Method
Endurance	200,000		Cycles	JEDEC Standard A117
Data Retention	20		Years	JEDEC Standard A103
ESD - Human Body Model	2,000		Volts	JEDEC Standard A114
ESD - Machine Model	200		Volts	JEDEC Standard A115
Latch-Up	100 + I_{CC1}		mA	JEDEC Standard 78

Note: These parameters are characterized and are not 100% tested.

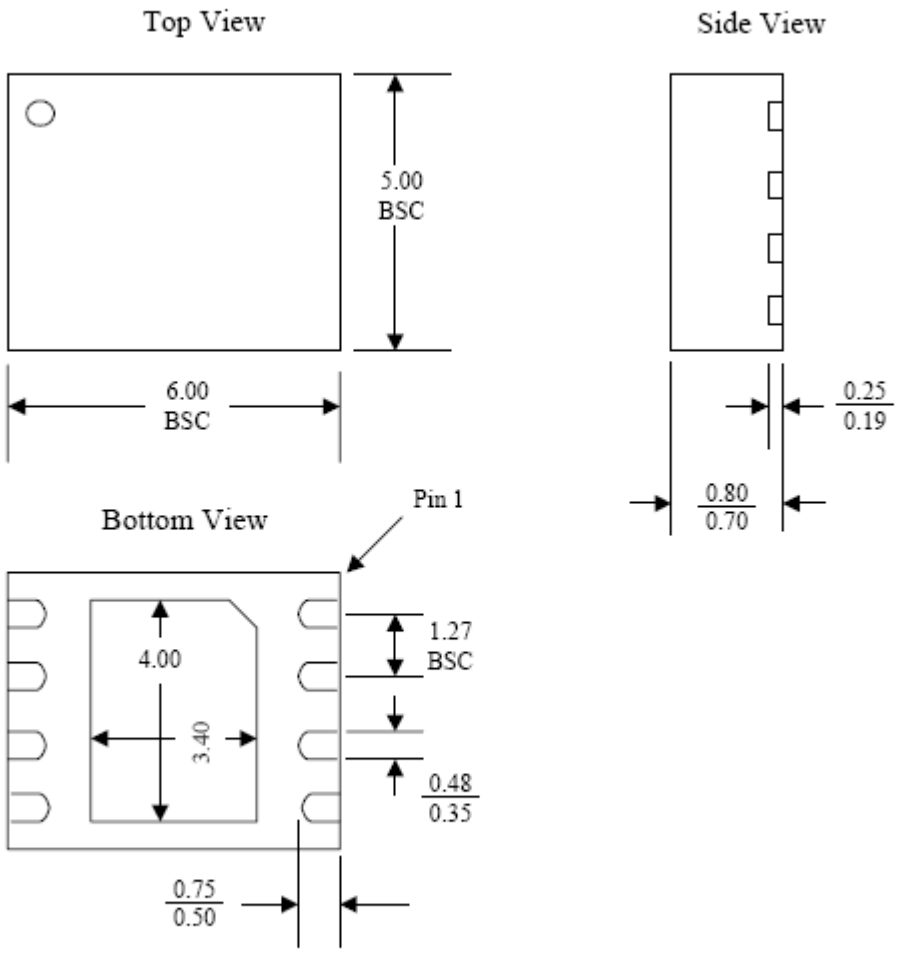
PACKAGE TYPE INFORMATION

8S
8-Pin JEDEC 150mil Broad Small Outline Integrated Circuit (SOIC) Package
(measure in millimeters)



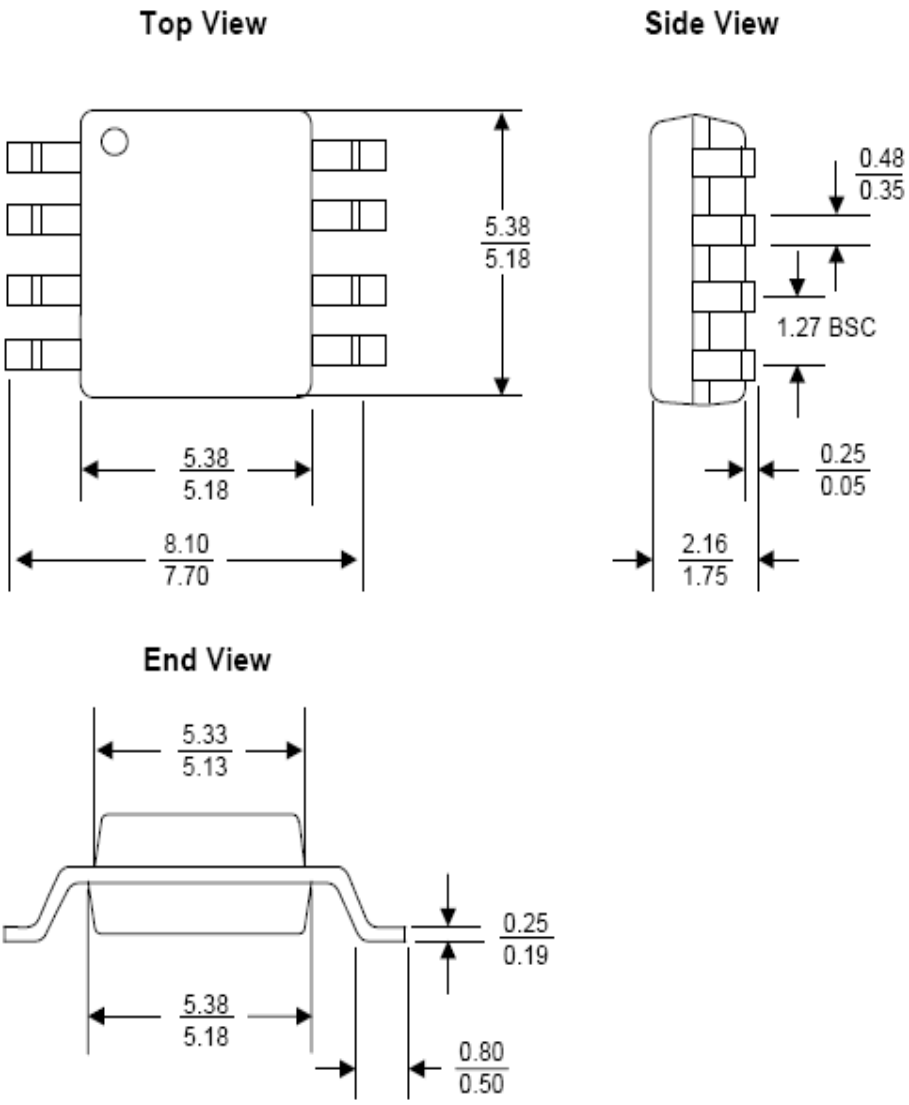
PACKAGE TYPE INFORMATION (CONTINUED)

8K
8-Contact Ulta-Thin Small Outline No-Lead (WSON) Package (measure in millimeters)



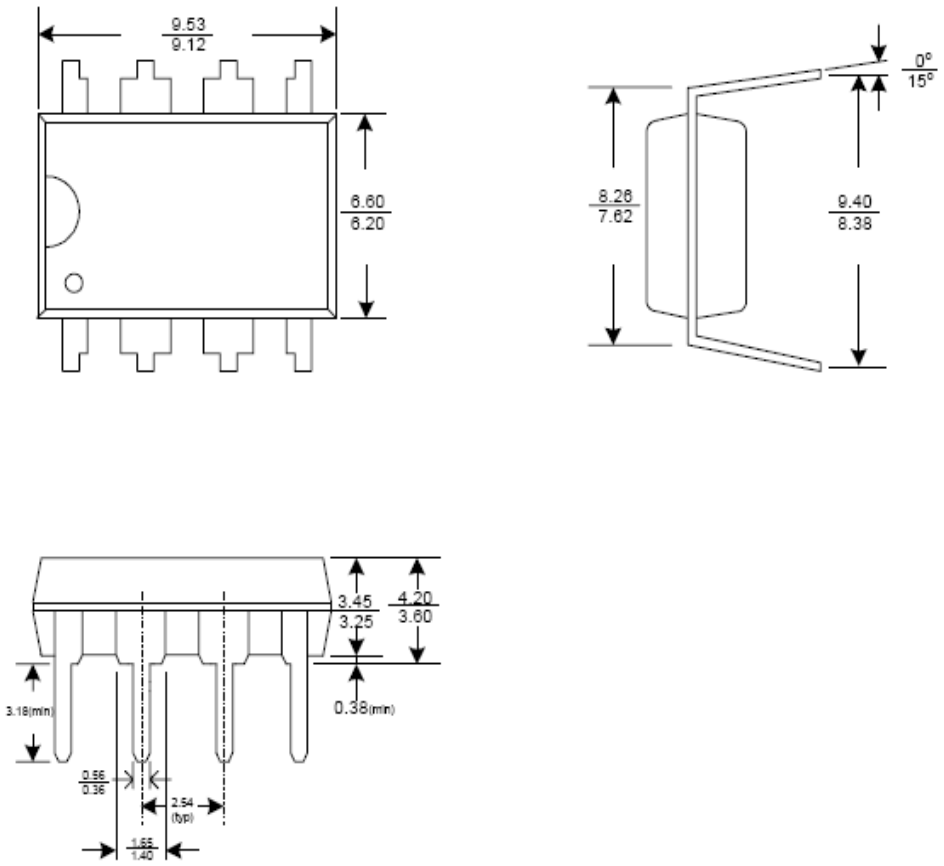
PACKAGE TYPE INFORMATION (CONTINUED)

8B
8-Pin JEDEC 208mil Broad Small Outline Integrated Circuit (SOIC) Package (measure in millimeters)



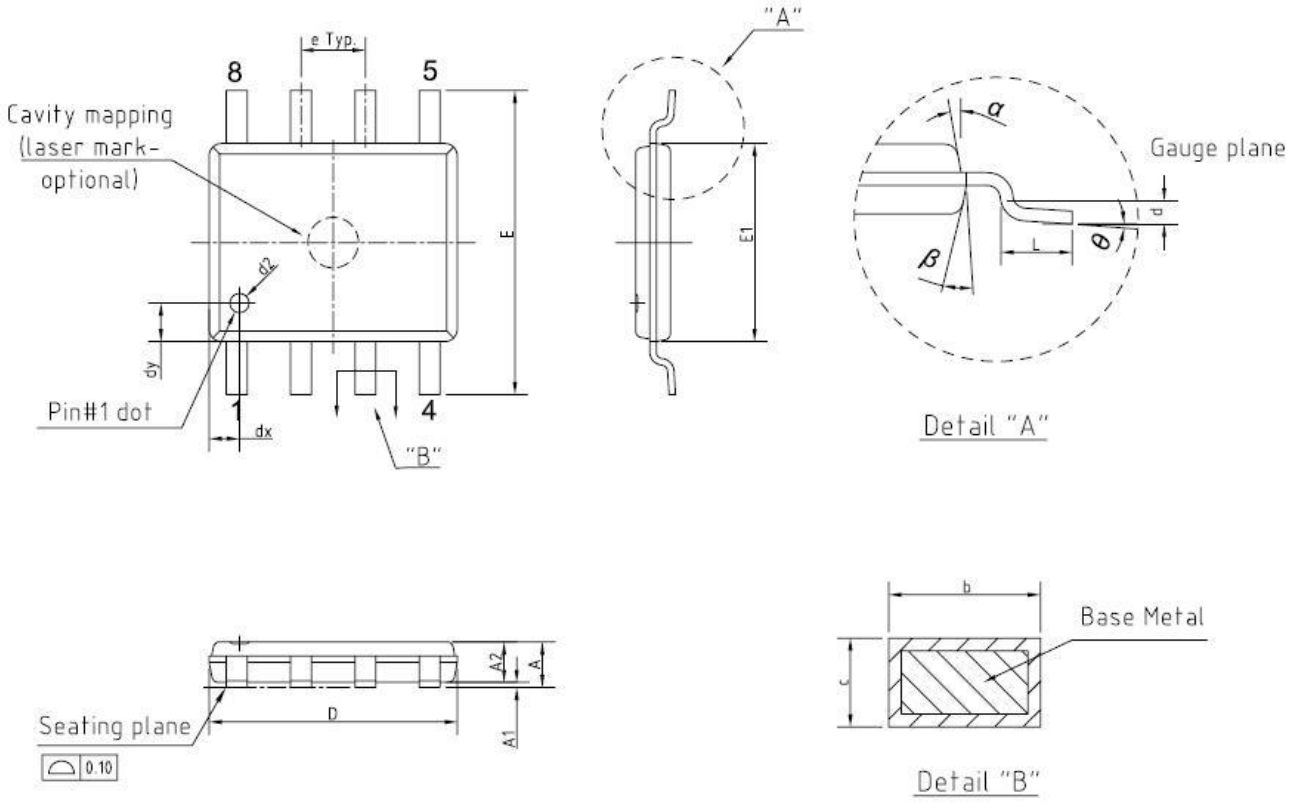
PACKAGE TYPE INFORMATION (CONTINUED)

8P
8-pin 300mil wide body, Plastic Dual In-Line Package PDIP (measure in millimeters)



PACKAGE TYPE INFORMATION (CONTINUED)

8E
8-pin VVSOP Package 150mil



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.88	---	---	34.6
A1	0.05	---	0.14	2.0	---	5.5
A2	0.63	---	0.74	24.8	---	29.1
b	0.33	0.41	0.51	13.0	16.1	20.1
c	0.13	---	0.18	5.1	---	7.1
D	4.80	4.90	5.00	189.0	192.9	196.9
d	---	0.25	---	---	10.0	---
d1	---	0.50typ	---	---	19.7typ	---
dx	---	0.60typ	---	---	23.6typ	---
dy	---	0.76typ	---	---	29.9typ	---
E	5.80	6.00	6.20	228.3	236.2	244.1
E1	3.80	3.90	4.00	149.6	153.5	157.5
e	---	1.27	---	---	50.0	---
L	0.41	0.71	1.27	16.1	28.0	50.0
α	---	10°	---	---	10°	---
β	---	10°	---	---	10°	---
θ	0°	---	10°	0°	---	10°

NOTES:
1. MOLD BODY DIMENSION DOES NOT INCLUDE END FLASH.
2. THE MOLDED END FLASH IS MAX. 0.15 mm.
3. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION / INTRUSION.

REVISION HISTORY

Date	Revision No.	Description of Changes	Page No.
October, 2007	0.0	Preliminary Product Specification	All
July, 2008	0.1	Add 4M in the datasheet	All
Jan, 2009	0.4	release the official version to customer	All
Feb, 2009	0.5	Remove 1M from the spec	All
Feb, 2009	0.6	1. Modify the erase time 15ms	1
March, 2009	0.7	1. Modify the device ID and instruction 2. Only for 4M flash 3. Modify the write inhibit from 2.0V to 2.1V	All All 9
September, 2009	0.8	1. Modify the program clock to 33MHz	10
October,2009	0.9	1. Optimize the erase time 10ms 2. Can meet the program clock 100MHz.	1 10
August, 2010	1.0	Modify the write inhibit to 1.8V	
June, 2012	1.1	Add the VVSOP package	1,2,33,34
October,2012	1.11	Revise VVSOP package	34