

HEX D-TYPE FLIP FLOPS WITH RESET

DESCRIPTION

The M74LS174P is a semiconductor integrated circuit containing 6 D-type edge-triggered flip-flop circuits with common clock input T and direct reset input $\overline{R_D}$ as well as discrete data input D.

FEATURES

- Positive edge-triggering
- Common clock and direct reset inputs for all 6 circuits
- Q and \overline{Q} outputs
- Wide operating temperature range ($T_A = -20 \sim +75^\circ C$)

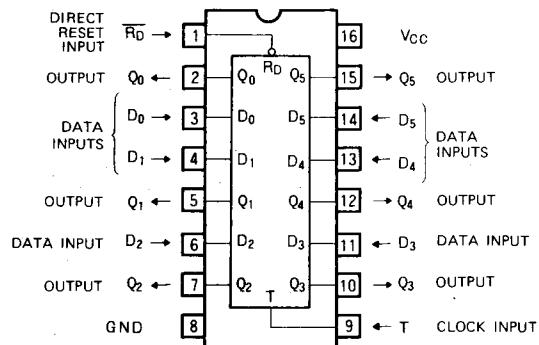
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change appears in the output Q in accordance with the function table. When $\overline{R_D}$ is low, all Q are low, regardless of the status of the other input signals. For use as a D-type flip-flop, keep $\overline{R_D}$ high.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTION TABLE (Note 1)

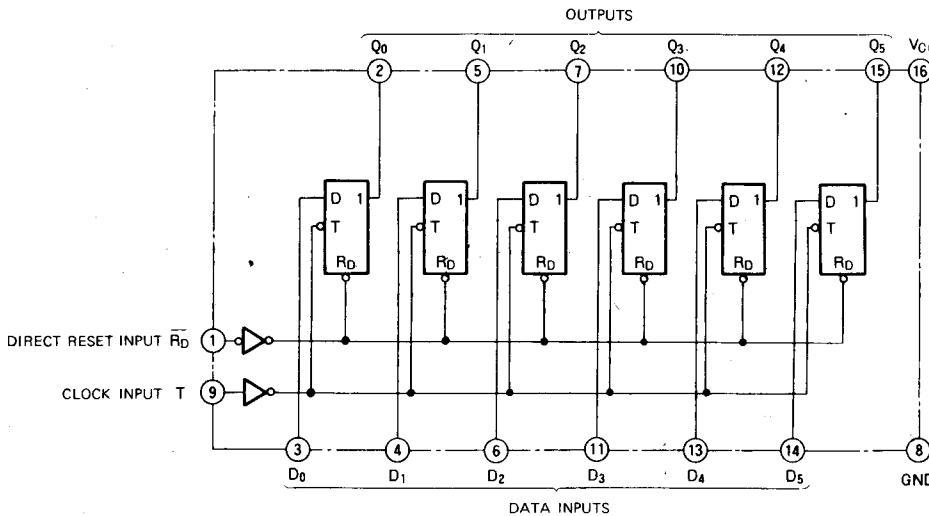
$\overline{R_D}$	T	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q^0

Note 1: ↑ : transition from low to high level

Q^0 : level of Q before the indicated steady-state input conditions were established

X : irrelevant

BLOCK DIAGRAM



HEX D-TYPE FLIP FLOPS WITH RESET**ABSOLUTE MAXIMUM RATINGS** ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		-0.5 ~ +7	V
V_I	Input voltage		-0.5 ~ +15	V
V_O	Output voltage	High-level state	-0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		-20 ~ +75	$^\circ\text{C}$
T_{stg}	Storage temperature range		-65 ~ +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High-level output current $V_{OH} \geq 2.7\text{V}$	0		-400	μA
I_{OL}	Low-level output current $V_{OL} \leq 0.4\text{V}$	0		4	mA
	$V_{OL} \leq 0.5\text{V}$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ *	Max		
V_{IH}	High-level input voltage		2			V	
V_{IL}	Low-level input voltage				0.8	V	
V_{IC}	Input clamp voltage	$V_{CC} = 4.75\text{V}$, $I_{IC} = -18\text{mA}$			-1.5	V	
V_{OH}	High-level output voltage	$V_{CC} = 4.75\text{V}$, $V_I = 0.8\text{V}$ $V_I = 2\text{V}$, $I_{OH} = -400\mu\text{A}$	2.7	3.4		V	
V_{OL}	Low-level output voltage	$V_{CC} = 4.75\text{V}$, $I_{OL} = 4\text{mA}$	0.25	0.4		V	
		$V_I = 0.8\text{V}$, $V_I = 2\text{V}$, $I_{OL} = 8\text{mA}$	0.35	0.5		V	
I_{IH}	High-level input current	$V_{CC} = 5.25\text{V}$, $V_I = 2.7\text{V}$			20	μA	
		$V_{CC} = 5.25\text{V}$, $V_I = 10\text{V}$			0.1	mA	
I_{IL}	Low-level input current	$V_{CC} = 5.25\text{V}$, $V_I = 0.4\text{V}$			-0.4	mA	
I_{OS}	Short-circuit output current Note 2	$V_{CC} = 5.25\text{V}$, $V_O = 0\text{V}$	-20		-100	mA	
I_{CC}	Supply current	$V_{CC} = 5.25\text{V}$ (Note 3)			16	26	mA

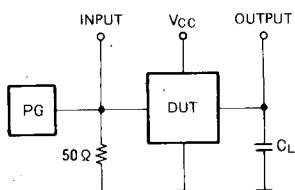
* : All typical values are at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with D, R_D inputs at 4.5V and a momentary ground, then 4.5V, applied to T input**SWITCHING CHARACTERISTICS** ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency		30	47		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output Q			10	30	ns
t_{PHL}	High-to-low-level output propagation time, from input R_D to output Q	$C_L = 15\text{pF}$ (Note 4)		10	30	ns
				11	35	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
 $PRR = 1\text{MHz}$, $t_r = 6\text{ns}$, $t_f = 6\text{ns}$, $t_w = 500\text{ns}$,
 $V_p = 3\text{V}_{p,p}$, $Z_0 = 50\Omega$

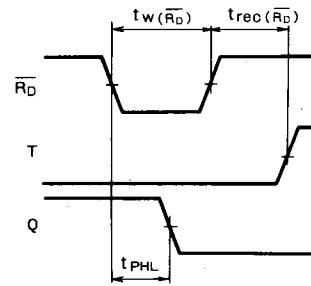
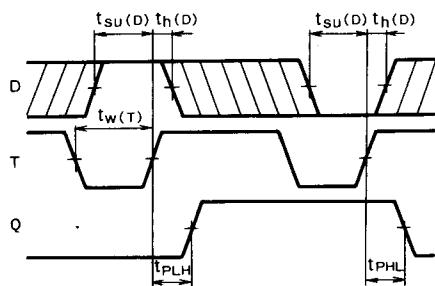
(2) C_L includes probe and jig capacitance.

HEX D-TYPE FLIP FLOPS WITH RESET

TIMING REQUIREMENTS ($V_{CC} = 5\text{ V}$, $T_a = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits	Unit
		Min	Typ	Max		
$t_w(T)$	Clock input T pulse width	20	4		ns	
$t_w(\bar{R}_D)$	Reset input \bar{R}_D pulse width	20	6		ns	
$t_{SU}(D)$	Setup time D to T	20	2		ns	
$t_h(D)$	Hold time D to T	5	0		ns	
$t_{REC}(\bar{R}_D)$	Recovery time \bar{R}_D to T	25	5		ns	

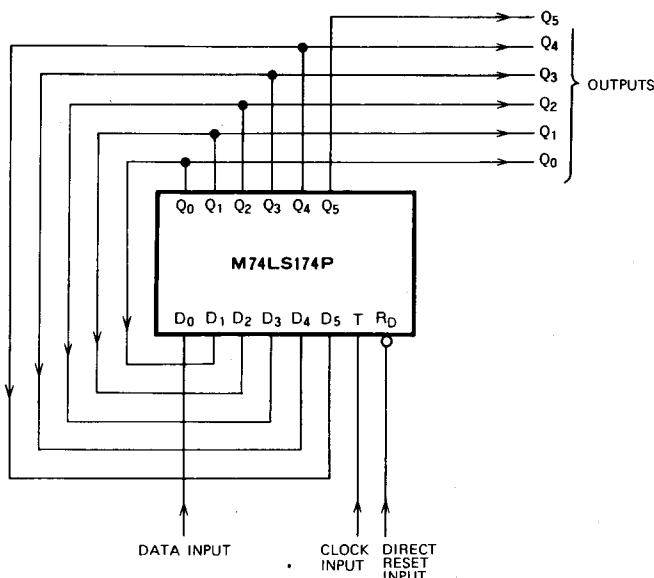
TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

6-bit shift register



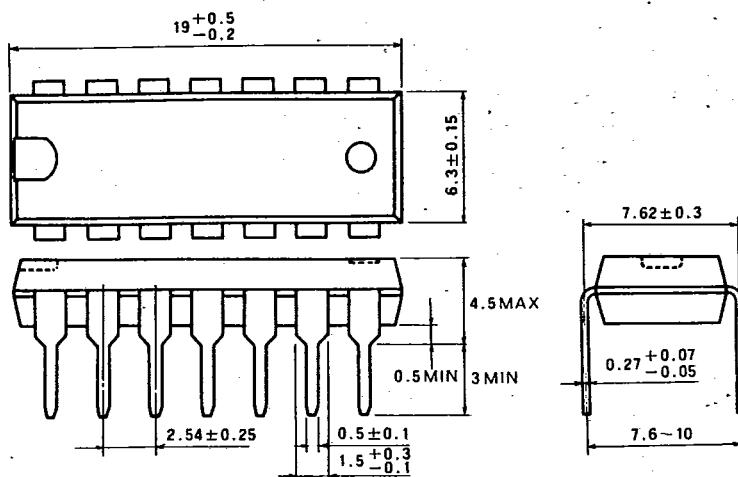
MITSUBISHI LSTTLs
PACKAGE OUTLINES

MITSUBISHI {DGTL LOGIC} 07E D | 6249827 0013561 3

T-90-20

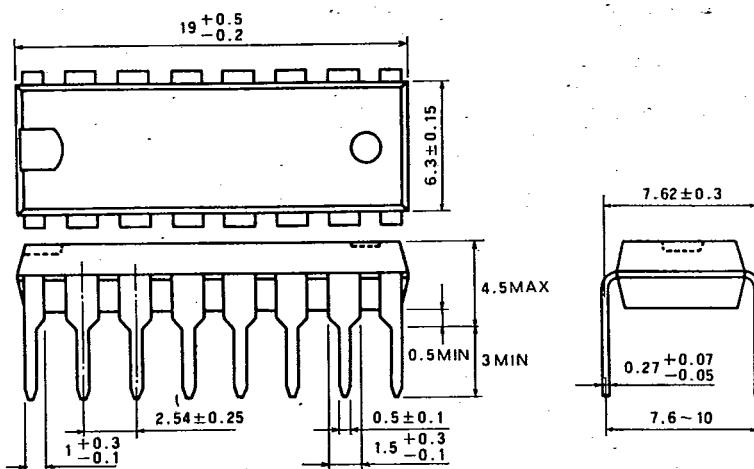
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

