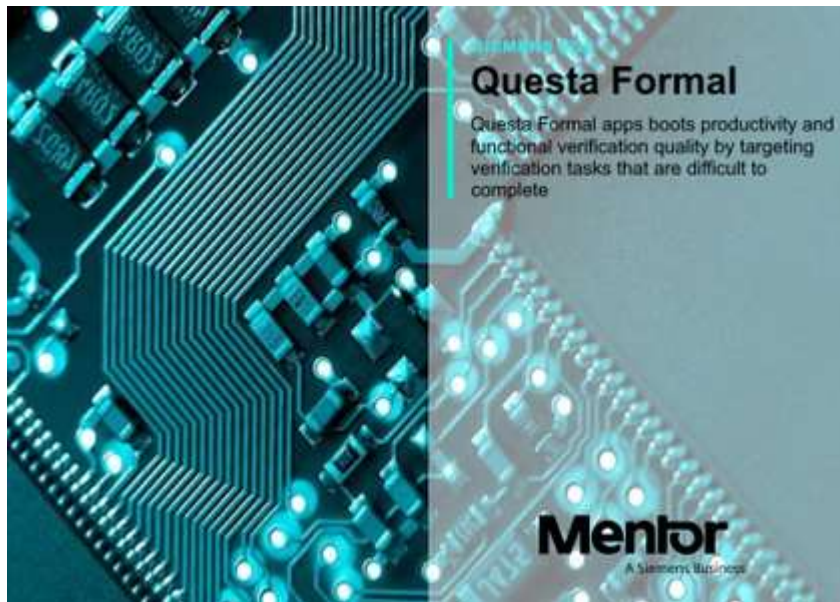


Mentor Questa Formal

Mentor Graphics Corporation, a Siemens business, is pleased to announce the availability of Questa Formal 2021.1. This solution finds obscure bugs, increasing design confidence through exhaustive analysis, before simulation test environments are available, and also boosts productivity and functional verification quality by targeting verification tasks that are difficult to complete.



2021.1 Release Notes

Major New Features in 2021.1

Version 2021.x releases have significant enhancements and changes compared with the 2020.x series of releases.

The Questa verification solution from Siemens EDA, a part of Siemens Digital Industries Software, continues to evolve in response to the growing complexity of SoC designs. Besides the sheer size of designs, the inclusion of multiple embedded processors and advanced interconnect systems, increasing software content and the configurability required by multi-platform based designs require a functional verification solution that unifies a broad arsenal of verification solutions.

Questa lets you apply CDC verification, formal verification, mixed-signal verification, portable stimulus, and other powerful technologies to maximize the effectiveness of your verification at

the block- and subsystem-level so your system-level verification can focus on system-level functionality, including software, without having to worry about lower-level bugs taking away from your productivity. No one wants to compromise product quality. However, time-to-market pressures dominate SoC projects. To deliver quality within schedule requires improving the time to achieve coverage and quality goals and improving debug productivity.

Questa Formal Apps statically analyze a design's behavior with respect to a given set of properties; then exhaustively explore all possible input sequences in a breadth-first search manner. This uncovers design errors that would otherwise be missed or are impractical to find with simulation-based methods.

Questa Formal Apps boost verification efficiency and design quality by exhaustively addressing verification tasks that are difficult to complete with traditional methods, and they don't require formal or assertion-based verification experience.

Properties are synthesized from a combination of automatic RTL design analysis and a high-level specification of design intent. The generated properties are then exhaustively verified with formal analysis engines.

The Questa Formal App suite includes applications to address tasks such as: static and conditional connectivity checking, secure path integrity checking, unreachable code identification, X-state propagation, state-space analysis, and register verification. Additionally, the Questa Sequential Logic Equivalence Checking (SLEC) App uses formal methods to perform exhaustive comparisons between inputs to reveal any behavioral discrepancies that could arise in clock gating, ECO integration, re-pipelining, or fault mitigation logic.

Mentor Graphics Corporation, a Siemens business, is a world leader in electronic hardware and software design solutions, providing products, consulting services, and award-winning support for the world's most successful electronic, semiconductor, and systems companies. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.

Questa® Formal Technology Installation Guide

For Linux and Windows Platforms

Software Version 2021.1
Document Revision 1

Supported Operating Systems and Simulators

Questa Design and Formal applications and the QVerify infrastructure only run on specific Hardware and OS platform configurations and they require minimum memory resources. Some applications share data with specified versions of industry standard simulators.

Supported Hardware/OS Platforms

Platform	OS	Binary	VCO name ¹	Memory capacity
EM64T	<ul style="list-style-type: none"> SUSE Linux² Enterprise Server 12 Red Hat Enterprise Linux 7 and 8 	32-bit	linux	3GB ³
		64-bit	linux_x86_64	terabytes
x86	Windows 10	32-bit	win32 ⁴	2GB
		64-bit	win64	terabytes
	<ul style="list-style-type: none"> SUSE Linux Enterprise Server 12 Red Hat Enterprise Linux 7 and 8 	32-bit	linux	3GB
		64-bit	linux_x86_64	terabytes
AMD64	<ul style="list-style-type: none"> SUSE Linux Enterprise Server 12 Red Hat Enterprise Linux 7 and 8 	32-bit	linux	3GB
		64-bit	linux_x86_64	terabytes
ARM64	<ul style="list-style-type: none"> Red Hat Enterprise Linux 7 	64-bit	linux_aarch64 ⁵	terabytes

- The VCO name refers to the platform directories that are created during installation.
- Linux[®] is a registered trademark of Linus Torvalds in the U.S. and other countries.
- Memory usage is limited to the maximum process size allowed by the Linux kernel.
- ModelSim 32-bit (win32) installs and runs on Windows 64-bit OS, though it only runs as a 32-bit binary.
- Early access support available. Contact Siemens EDA to enable support.

Application Support and Limitations

Questa Design and Formal applications are available on Linux, but only a subset of the complete suite is available for Windows.

Following table list the applications supported for Linux.

Table 1-1. Applications Support for Linux

Design Solutions	Formal Solutions
Questa AutoCheck	Questa AutoCheck
Questa CDC	Questa CoverCheck
Questa Lint	Questa PropCheck
Questa RDC	Questa SLEC
Questa Signoff CDC	Questa X-Check
Questa X-Check	

Following table list the applications supported for Windows along with their limitations.

Table 1-2. Applications Support for Windows

Application	Limitation
Questa AutoCheck	Does not offer any grid support

Available FPGA Libraries

Distribution software includes commonly-used vendor FPGA libraries. Latest versions are pre-compiled and ready to use. Other versions are available, but need to be locally compiled for use.

Available FPGA Libraries

Table 1-3 shows the supported FPGA libraries.

Table 1-3. Available FPGA Libraries

FPGA Library	Default	Compiled Versions	Available Versions
XILINX ISE	14.7	13.2, 13.4, 14.7	13.2, 13.4, 14.7
XILINX VIVADO	2020.1	2018.2, 2018.3, 2019.1, 2019.2, 2020.1	2013.1, 2013.2, 2013.3, 2013.4, 2014.1, 2014.2, 2014.3, 2014.4, 2015.1, 2015.2, 2015.3, 2015.4.2, 2016.1, 2016.2, 2016.3, 2016.4, 2017.1, 2017.2, 2017.3, 2017.4, 2018.1, 2018.2, 2018.3, 2019.1, 2019.2, 2020.1
INTEL/ALTERA QUARTUS	20.2_pro	19.3_pro, 19.4_pro, 20.1_pro, 20.2_pro	13.0, 13.0sp1, 13.1, 14.0, 15.0, 15.1, 16.0, 16.1, 17.0, 17.0_std, 17.1_pro, 17.1_std, 18.0_std, 18.0_pro, 18.1_pro, 18.1_std, 19.2_pro, 19.3_pro, 19.4_pro, 20.1_pro, 20.2_pro
MICROSEMI LIBEROS	12.4	11.7_sp1, 11.7_sp3, 11.8, 11.9, 12.0, 12.1, 12.2, 12.3, 12.4	9.2_SP3, 11.7_sp1, 11.7_sp3, 11.8, 11.9, 12.0, 12.1, 12.2, 12.3, 12.4

Product: Mentor Questa Formal

Version: 2021.1

Supported Architectures: x64

Website Home Page : eda.sw.siemens.com/

Languages Supported: english

System Requirements: PC *

Mentor Questa Formal 2021.1 | 1.4 Gb