SINO WEALTH

SH367309

Analog Front-End IC For 5-16 Serials Cell Lithium-Ion Pack

1. Features

- Hardware Protection
  - Overvoltage Protection
  - Undervoltage Protection
  - Charge Overtemperature Protection
  - Charge Undertemperature Protection
  - Discharge Overtemperature Protection
  - Discharge Undertemperature Protection
  - Charge and Discharge Overcurrent Protection
  - Short Circuit Protection
  - Secondary Overvoltage Protection
  - Broken-wire Protection
- Integrated Balance Switch
- Low Voltage Prohibition Charge
- Small Current Detection For Wake Up
- Support Out-of-order Power On and Down
- Integrated Watchdog
- Operating Mode
  - AFE(SH367309 with MCU Application)
  - Protect Mode (SH367309 Independently Application)
  - SHIP Mode
  - WRITE Mode
- 13-bit VADC for Cell Voltage, Temperature and Current Measurements
  - Measurement Frequency: 10Hz
  - 16 Channels for Cell Voltage Measurements
  - 1 Channel for Current Measurement
  - 3 Channels For Temperature Measurements
- 16-bit Σ-ΔCADC for Current Measurement
  - Measurement Frequency: 4Hz
- Integrated EEPROM
  - Program Times: 100 times(@Max)
- LDO
  - 3.3V(25mA@MAX)
- Integrated N-MOSFET Driver
- CTL pin: Priority Control Charge and Discharge MOSFET
- TWI Communication With CRC8
- Low Power Consumption:
  - IDLE: 40uA@Typ (50uA@Max)
  - SLEEP: 35uA@Typ (45uA@Max)
  - PowerDown: 3uA@Typ (5uA@Max)
- Package
  - TQFP48L

2. General Description

SH367309 is an analog front-end IC for lithium battery BMS. It is suitable for lithium battery packs with a total voltage of no higher than 70V.

In protect mode, SH367309 can protect lithium battery packs independently, provides overvoltage protection, undervoltage protection, temperature protection, charge and discharge overcurrent protection, short circuit protection, and secondary overvoltage protection. Integrated balance switch improve cell consistency.

In AFE mode, SH367309 can be used with the MCU to manage the lithium battery pack, supports all protection.

SH367309 has Integrated VADC for cell voltage measurements, temperature measurements and current measurement; Integrated CADC for current measurement, used to count the remaining capacity; Integrated EEPROM, used to save adjustable parameters, such as protection threshold and delay; Integrated TWI communication.

3. Block Diagram

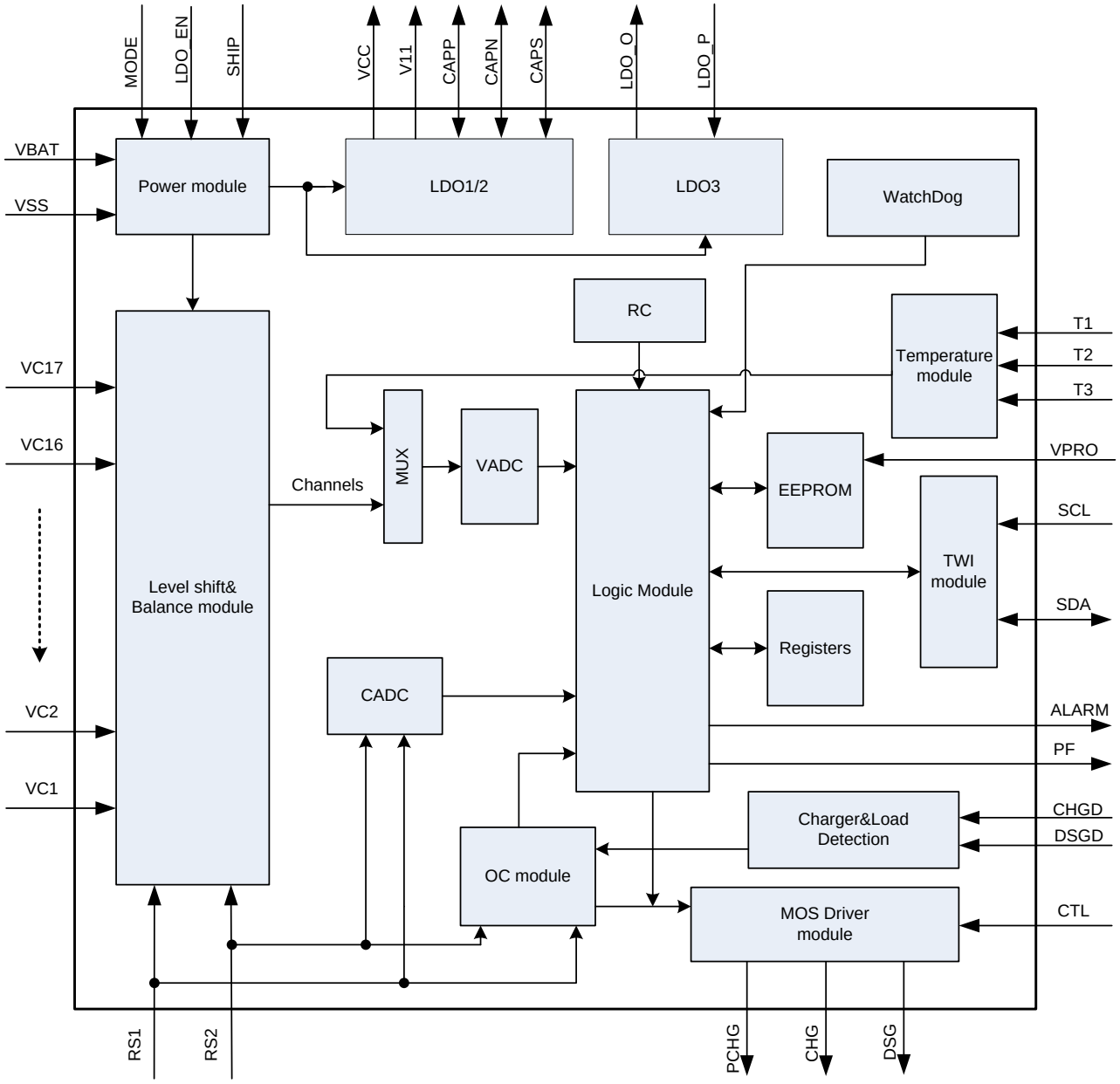


Fig 1. Block Diagram of SH367309

4. Pin Configuration

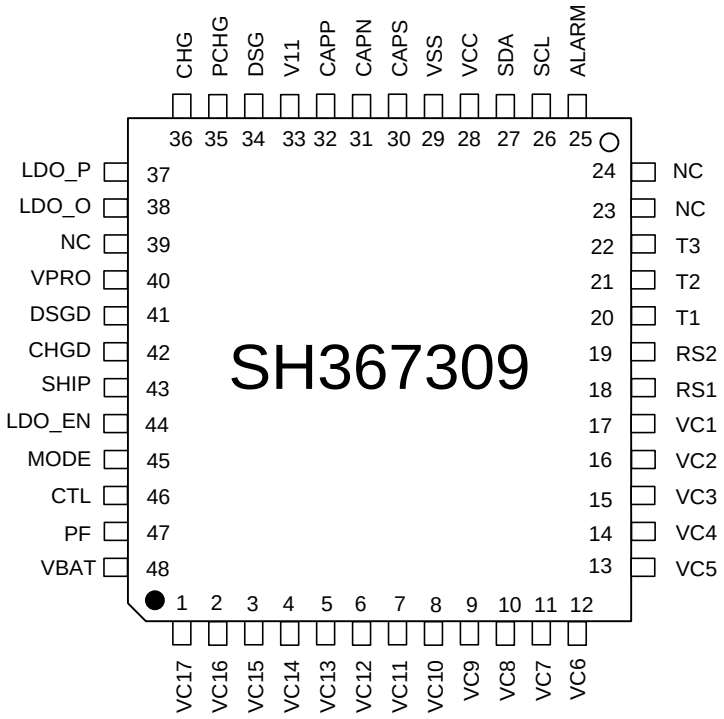


Fig 2. Pin Configuration of SH367309 (TQFP48L)

5. Pin Definition

Table1.Pin Definition

Pin No.	Pin Name	I/O	Function
1-17	VC17~VC1	I	Cell connect terminal(VC17 is the 16th cell positive terminal,VC1 is the 1th cell negative terminal
18	RS1	I	Negative current sense (nearest VSS)
19	RS2	I	Positive current sense
20~22	T1~T3	I	Thermistor #1/#2/#3 positive terminal
23	NC	-	No connect
24	NC	-	No connect
25	ALARM	O	Communication to the host controller, open drain output
26	SCL	I	TWI communication clock, open drain output
27	SDA	I/O	TWI communication data, open drain output
28	VCC	O	3.3V regulator
29	VSS	P	Chip ground
30	CAPS	I/O	DCDC converter
31	CAPN	I/O	DCDC converter
32	CAPP	I/O	DCDC converter
33	V11	O	11V regulator
34	DSG	O	Discharge MOSFET driver
35	PCHG	O	Pre-charge MOSFET driver
36	CHG	O	Charge MOSFET driver
37	LDO_P	P	LDO3 power supply
38	LDO_O	O	LDO3 regulator output
39	NC	-	No connect
40	VPRO	P	EEPROM power supply
41	DSGD	I	Load detection
42	CHGD	I	Charger detection
43	SHIP	I	Ship mode control pin
44	LDO_EN	I	LDO3 enable control pin
45	MODE	I	Mode control pin
46	CTL	I	MOSFET priority control pin
47	PF	O	Secondary overvoltage output
48	VBAT	P	Positive power supply

6 Typical Application

6.1 16S-Cell Two Terminals Application

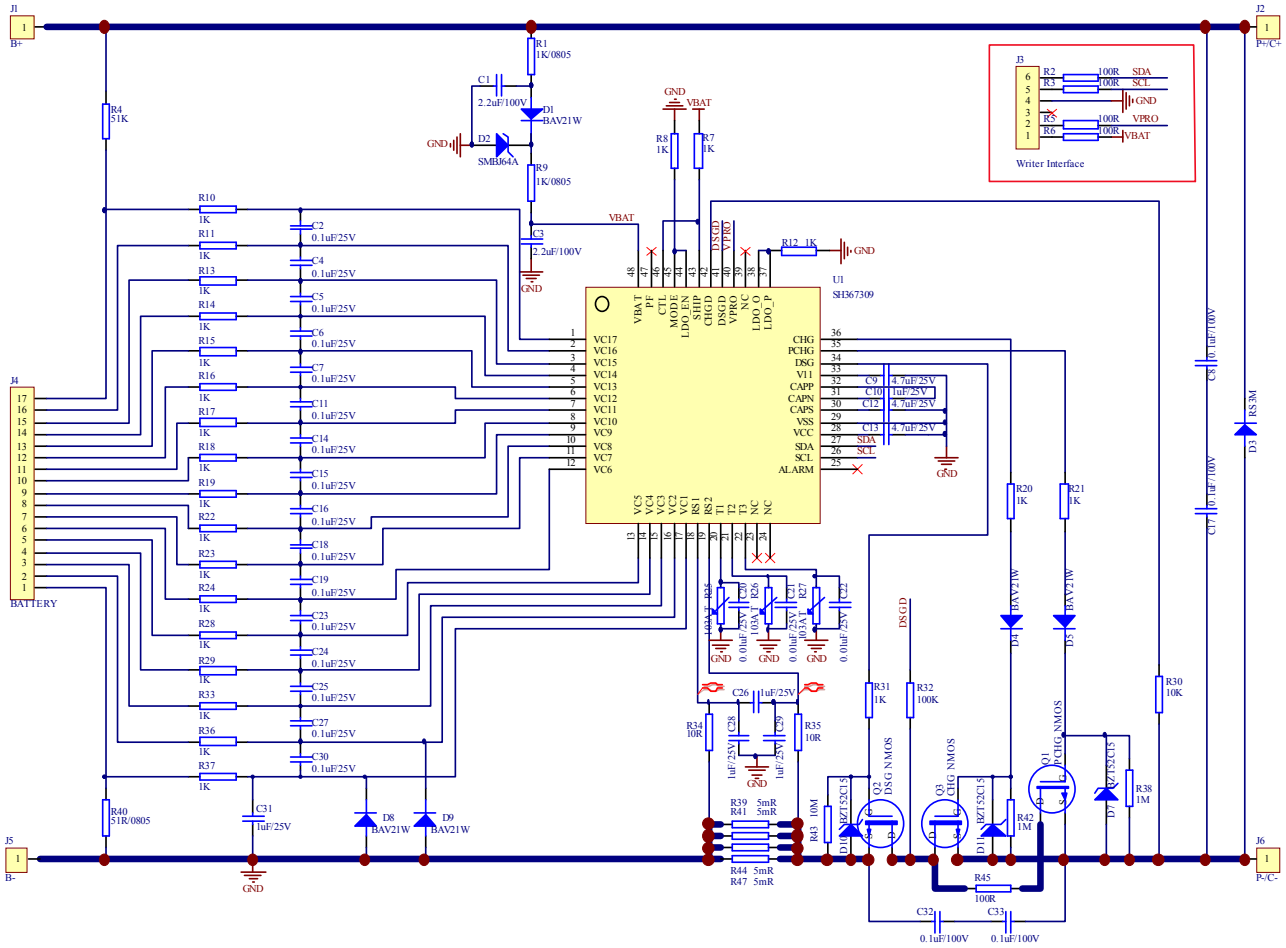


Fig 3. 16S-Cell two terminals application

6.2 16S-Cell Three Terminals Application With Balance

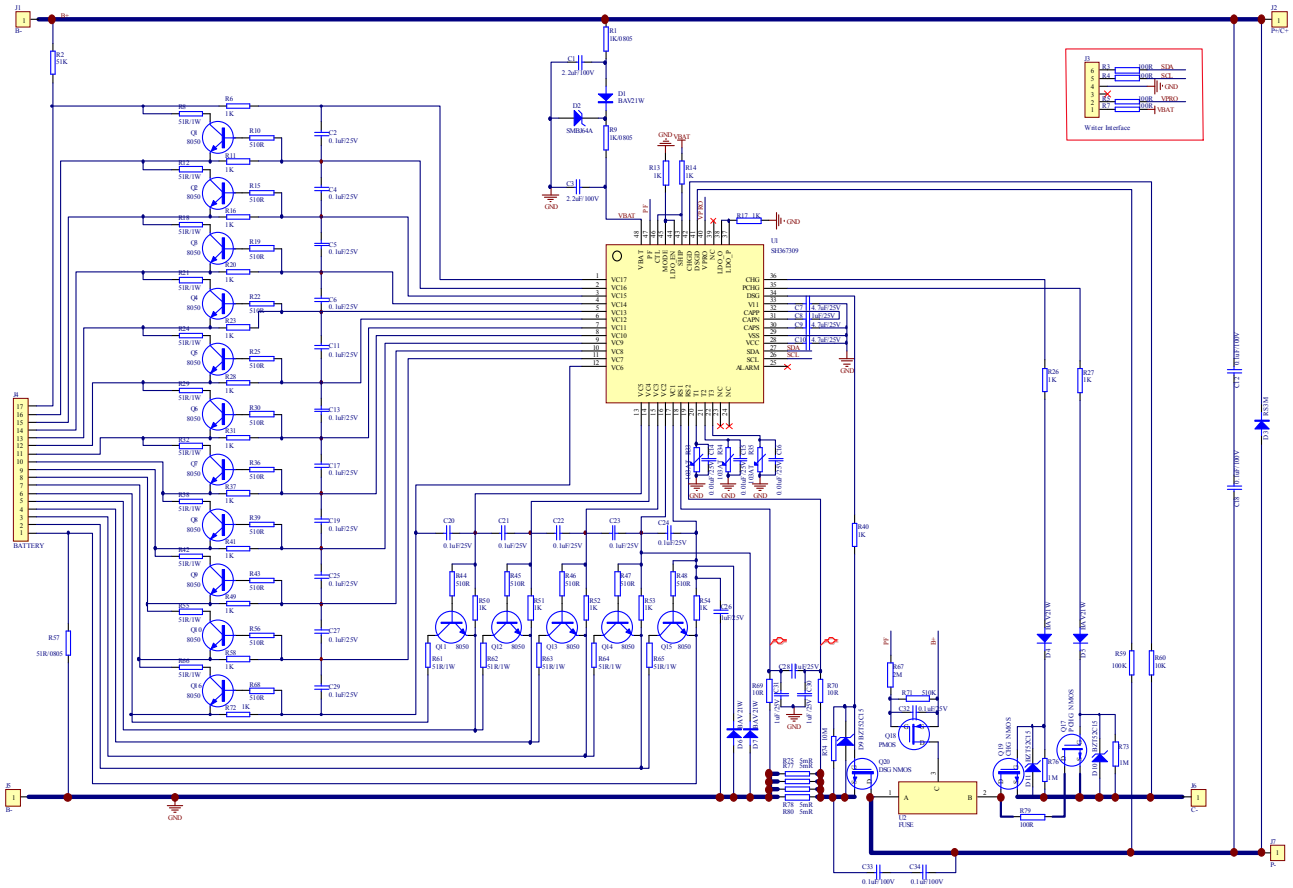


Fig 5. 16S-Cell three terminals application with balance

6.3 16S-Cell Three Terminals(full) Application

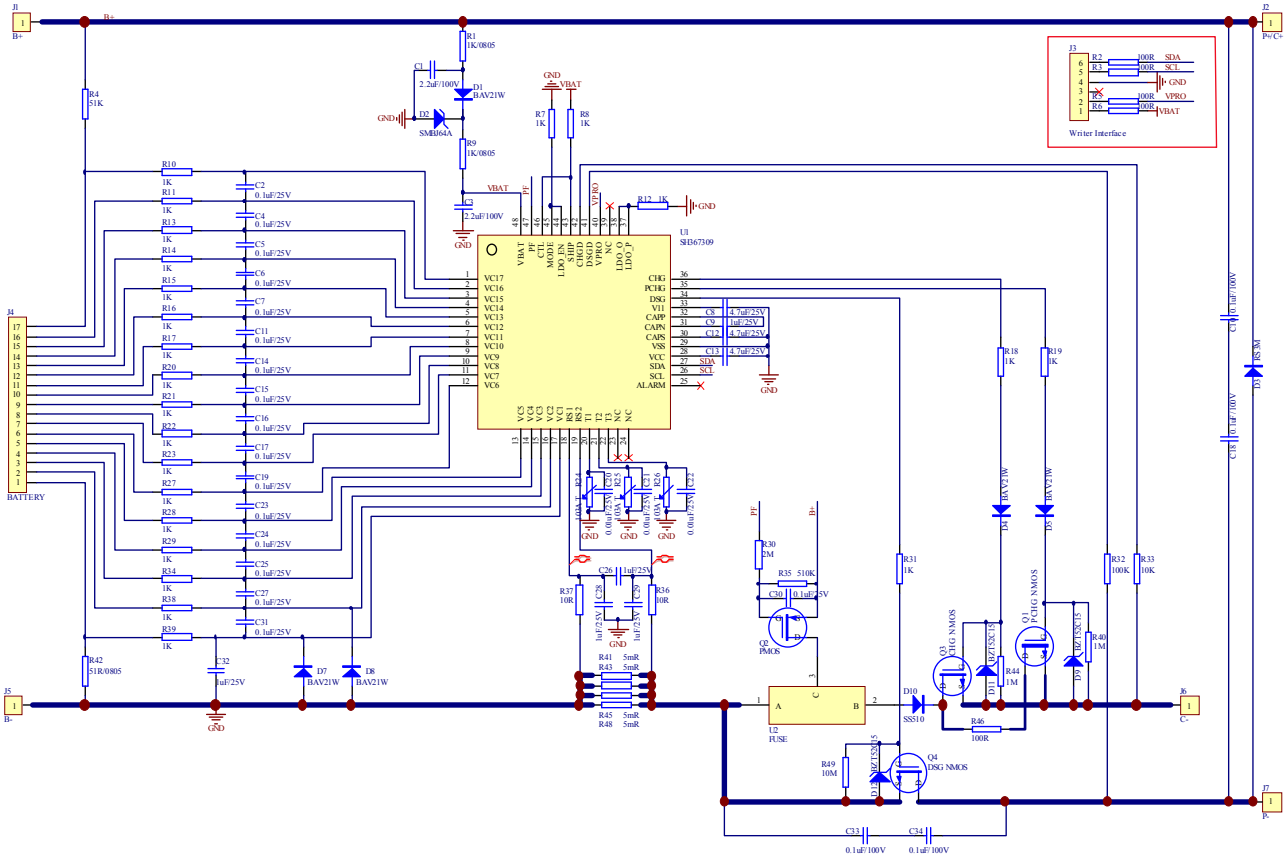


Fig 6. 16S-Cell three terminals (full) application

6.4 10S-Cell Three Terminals(Full) Application

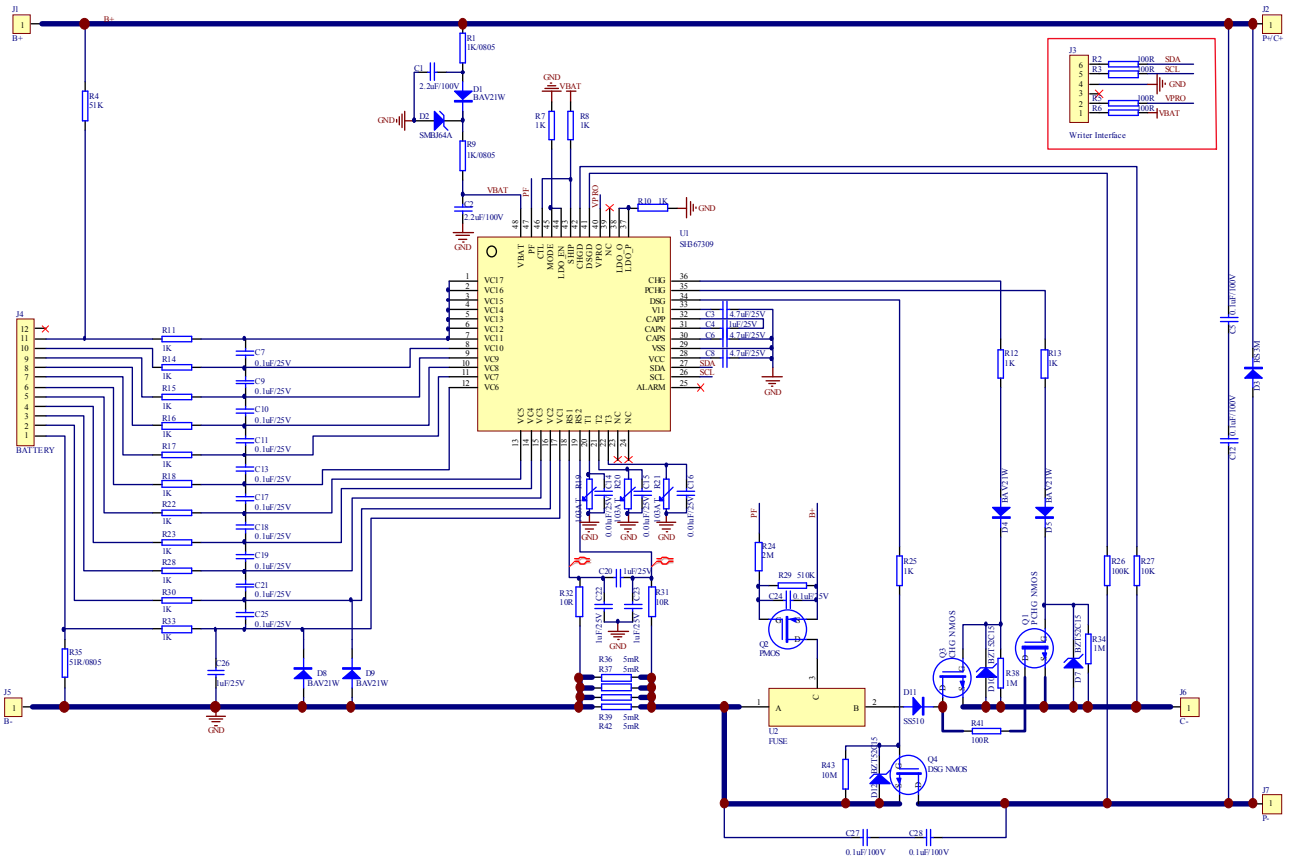


Fig 7. 10S-Cell three terminals (Full) application

6.5 AFE 16S-Cell Three Terminals Application

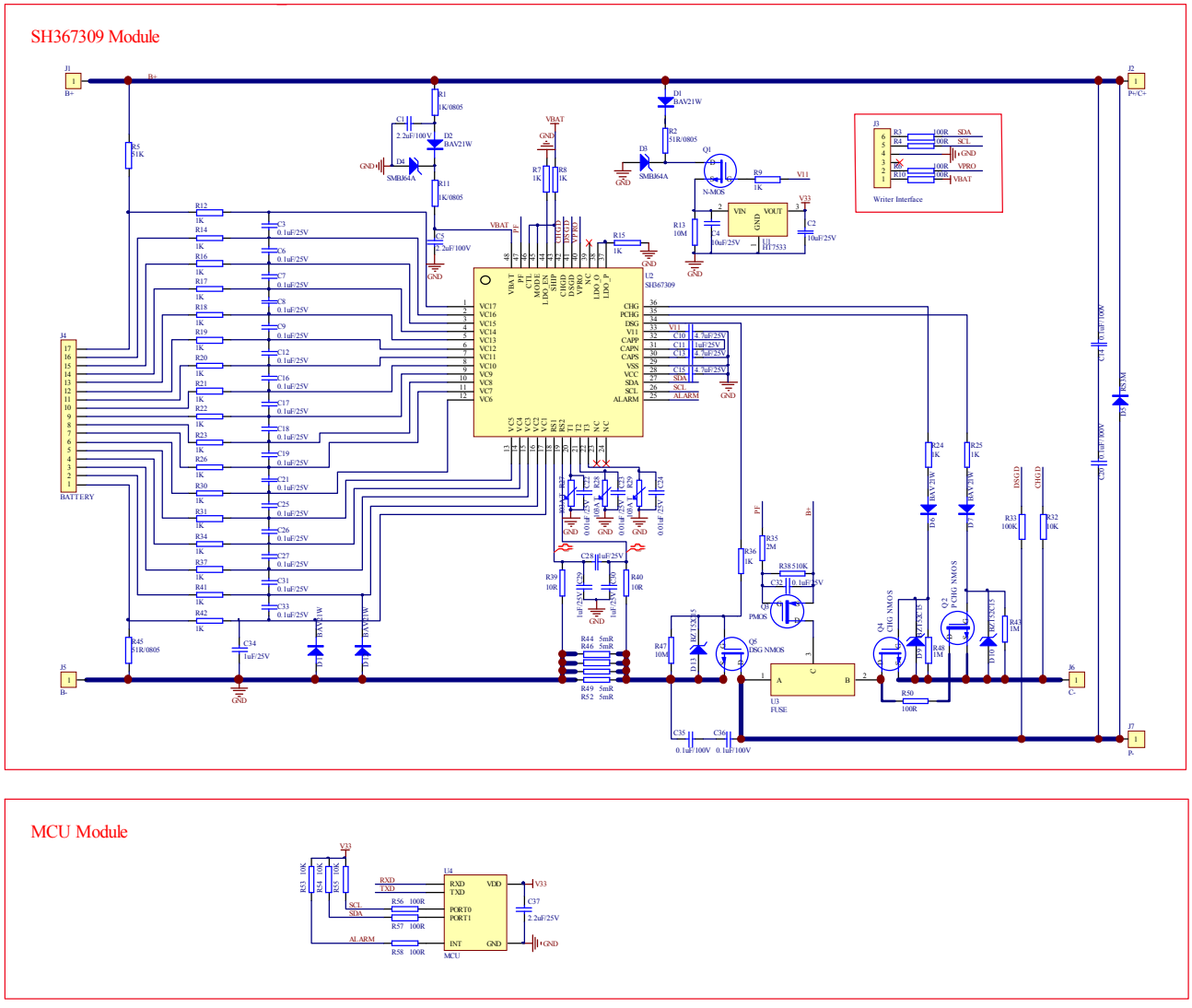


Fig 8. AFE 16S-Cell three terminals application

7. Operating Mode

7.1 Overview

SH367309 supports four operating modes: protect mode, AFE mode, SHIP mode, WRITE mode.

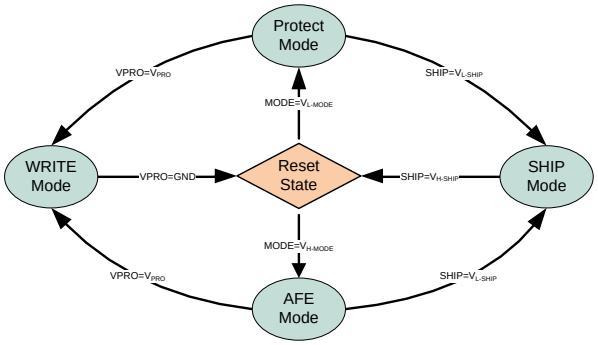


Fig 9. Operating Mode Convert

Table2. Function List

Function	Protect Mode		AFE Mode			SHIP Mode
	Normal State	Powerdown State	Normal State	IDLE State	SLEEP State	
Overvoltage/Undervoltage/Temperature protection	√	X	√	X	X	X
Overcurrent protection	√	X	√	√	X	X
Secondary overvoltage protection	√	X	√	X	X	X
Balance	√	X	√	X	X	X
VADC	√	X	√	X	X	X
CADC❶	X	X	√	X	X	X
TWI	X	X	√	X	X	X
Charger detection	√	√	√	√	√	X
STA detection❷	X	X	X	√	√	X
Small current detection❷	X	X	X	√	X	X
WDT❶	X	X	√	O	X	X
LDO1,LDO2	√	X	√	√	√	X
LDO3❸	X	X	√	√	√	X
Current(uA)	＜55	＜5	＜105	＜50	＜45	＜2

Note: Power consumption test conditions see AC/DC section.

Note: “√”Indicates that the function is on; “X” indicates that the function is off; “O” indicates that the function maintains the state before entering IDLE.

Note: ❶In the AFE mode, the CADC and WDT are turned off by default. MCU can turn on CADC and WDT by configuring the corresponding registers through the TWI.

❷STA detection is defined as the internal detection circuit. It is used in the AFE mode to wake up with low power consumption. The charge or discharge current detection voltage threshold is V_{CD}. If it is higher than V_{CD} and the delay is longer than t_{CD}, WAKE_FLG is set to 1 and an ALARM interrupt is generated.

❸LDO3 can be controlled by the LDO_EN pin. When LDO_EN=$V_{L\text{-}LDO\_EN}$, LDO3 is turned off. When LDO_EN=$V_{H\text{-}LDO\_EN}$, LDO3 is turned on.

7.2 Protect Mode

When MODE pin is low level $V_{L\text{-}MODE}$, SH367309 operate in protect mode.

7.2.1 Normal State

SH367309 turns on the integrated protection, turns on the balance, and turns off the watchdog and TWI communication.

7.2.2 Powerdown State

When the following conditions are satisfied, SH367309 enters the powerdown state and turns off the charge and discharge MOSFET:

(1) Any one cell voltage is lower than V_{PD}

(2) The status (1) duration is longer than T_{PD}

When the following conditions are satisfied, SH367309 exits the Powerdown state:

(1) Connect the charger (detect the CHGD pin voltage lower than V_{CHGD3})

Note: When the charger is connected, it cannot enter the powerdown state, after exiting the powerdown state, SH367309 generates a hardware reset.

7.3 AFE Mode

When MODE pin is high level $V_{H\text{-}MODE}$, SH367309 operate in AFE mode.

7.3.1 Normal State

SH367309 turns on integrated protection, turns on TWI communication. MCU can read and write SH367309 internal register through TWI communication.

7.3.2 IDLE State

When the following conditions are satisfied, SH367309 enters the IDLE state:

(1) No protection has occurred and no protection delay has occurred

(2) Detect that the sense resistor (RS2-RS1) voltage is higher than the charge current detection threshold V_{CD2} and (RS2-RS1) voltage is lower than the discharge current detection threshold V_{CD1}

(3) The IDLE bit in CONF register is set to 1

Note: Protection includes overvoltage, undervoltage, secondary overvoltage, short circuit, charge and discharge overcurrent, charge overtemperature and undertemperature, discharge overtemperature and undertemperature protection, pre-charge, low voltage prohibition charge, does not include watchdog overflow and CTL pin control.

After entering the IDLE state, SH367309 executes the following actions:

(1) Turn off VADC, CADC, TWI modules, and turn off voltage and temperature related protection

(2) Clear the BALANCEH and BALANCEL register

(3) Turn on STA detection

(4) Turn on charge and discharge current detection

When any one of the following conditions is satisfied, SH367309 exits the IDLE state:

(1) STA signal detected

(2) Detect that the sense resistor (RS2-RS1) voltage is lower than the charge current detection threshold V_{CD2} or the voltage is higher than the discharge current detection threshold V_{CD1}, and the delay is longer the charge-discharge current detection delay t_{CD}

When mode (2) exiting the IDLE state, SH367309 outputs a low level pulse to the MCU through the ALARM pin.

7.3.3 SLEEP State

When the following conditions are satisfied, SH367309 enters SLEEP state:

(1) The SLEEP bit in CONF register is set to 1

After entering the SLEEP state, SH367309 executes the following actions:

(1) Turn off the charge and discharge MOSFET, turn off the VADC, CADC, TWI, WDT, and turn off all protections

(2) Clear the BALANCEH and BALANCEL register

(3) Turn on STA detection

(4) Turn on charger detection

When any one of the following conditions is satisfied, SH367309 exits the SLEEP state:

(1) STA signal detected

(2) Connect the charger (detect the CHGD pin voltage is lower than V_{CHGD1} and the delay is longer than t_{D3})

When status (2) exiting the SLEEP state, SH367309 outputs a low level pulse to the MCU through the ALARM pin.

Note: When the charger is connected, the SLEEP bit in CONF register is set to 1, and SH367309 enters the SLEEP state before exiting.

7.4 SHIP Mode

When SHIP pin is low level V_{L-SHIP}, SH367309 operate in SHIP mode:

(1) Turn off the charge and discharge MOSFET, and turn off all modules

(2) Connect charger without any action

When SH367309 operate in SHIP mode, only the SHIP pin is connected to the high level V_{H-SHIP} to exit the SHIP mode, and generate a hardware reset.

7.5 WRITE Mode

When VPRO pin is EEPROM write voltage V_{PRO}, and the delay is longer than 10mS, SH367309 enters the WRITE mode, turn off the charge and discharge MOSFET and all protections. At this time, other devices can read/write the Integrated EEPROM register through the TWI communication.

7.6 Warm-up

7.6.1 Hardware Reset

Hardware reset includes power-on reset, LVR reset, exit SHIP mode, and exit the powerdown state.

After a power-on reset, exit the SHIP mode, and exit the powerdown state:

(1) LDO_EN pin is high level V_{H-LDO_EN}, SH367309 enter to be activated state, turn off charge and discharge MOSFET and TWI communication

(2) LDO_EN pin is low level V_{L-LDO_EN}, SH367309 enters warm-up state

When the system is in mode (1), the following conditions must be satisfied to exit be activated state, and enter the warm-up state:

(1) Connect charger (CHGD pin voltage is lower than V_{CHGD1})

(2) The status (1) duration is longer than t_{D3}

After the LVR reset occurs, SH367309 enters the warm-up state directly.

The warm-up state duration is T_{WARMUP}. The charge and discharge MOSFET are turned off during the warm-up state. TWI communication is disabled. After the warm-up is over, the system starts normal operation.

7.6.2 Software Reset

In AFE mode, When the TWI module receives a software reset command sent by the MCU; a software reset occurs and enters the warm-up state.

Note: After warm-up is over, broken-wire and secondary overvoltage protection are not detected within 8 minutes.

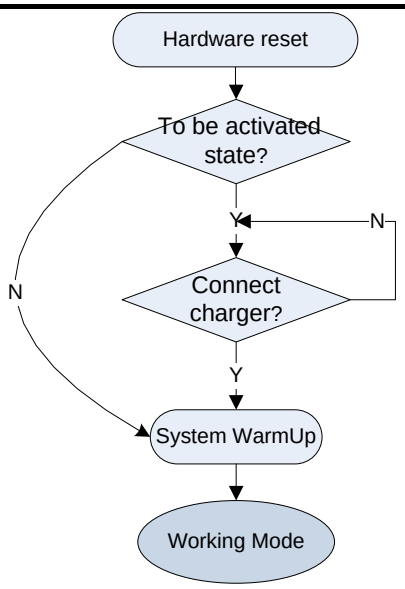


Fig 10. Warm-up Timing

8. Protect Function

8.1 Overview

In protect or AFE mode, SH367309 integrated all protection.

8.2 Overvoltage Protection

When the following conditions are satisfied, SH367309 enters overvoltage protection status:

(1) Any one cell voltage is higher than V_{OV}

(2) The status (1) duration is longer than t_{OV}

When SH367309 is in the overvoltage protection status, executes the following actions:

(1) Turn off the charge MOSFET

(2) The OV bit in the BSTATUS1 register is set to 1

(3) The OV_FLG bit in the BFLAG1 register is set to 1

When the following conditions are satisfied, SH367309 exits the overvoltage protection status:

(1) All cell voltages are lower than V_{OVR}

(2) The status (1) duration is longer than t_{OVR}

When SH367309 exits the overvoltage protection status, executes the following actions:

(1) Turn on charge MOSFET

(2) The OV bit in the BSTATUS1 register is clear

Note: V_{OV}, V_{OVR} and t_{OV} can be set in the corresponding EEPROM register.

Table 8.1 System Status Register1

43H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSTATUS1	WDT	PF	SC	OCC	OCD2	OCD1	UV	OV
R/W	R	R	R	R	R	R	R	R

Bit Number	Symbol	Description
0	**OV**	Overvoltage protection status 1: Protection occurring 0: Protection has not occurring

Table 8.2 System Flag Register1

70H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BFLAG1	WDT_FLG	PF_FLG	SC_FLG	OCC_FLG	LOAD_FLG	OCD_FLG	UV_FLG	OV_FLG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
0	**OV_FLG**	Overvoltage protection flag 1: Protection occurred 0: Protection has not occurred

Table 8.3 Overvoltage Threshold Register

02H,03H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OVH	OVT3	OVT2	OVT1	OVT0	LDRT1	LDRT0	OV.9	OV.8
OVL	OV.7	OV.6	OV.5	OV.4	OV.3	OV.2	OV.1	OV.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**OVT3~OVT0**	Overvoltage detection delay configuration OVT[3:0] = 0000: OV delay = 100mS OVT[3:0] = 0001: OV delay = 200mS OVT[3:0] = 0010: OV delay = 300mS OVT[3:0] = 0011: OV delay = 400mS OVT[3:0] = 0100: OV delay = 600mS OVT[3:0] = 0101: OV delay = 800mS OVT[3:0] = 0110: OV delay = 1S OVT[3:0] = 0111: OV delay = 2S OVT[3:0] = 1000: OV delay = 3S OVT[3:0] = 1001: OV delay = 4S OVT[3:0] = 1010: OV delay = 6S OVT[3:0] = 1011: OV delay = 8S OVT[3:0] = 1100: OV delay = 10S OVT[3:0] = 1101: OV delay = 20S OVT[3:0] = 1110: OV delay = 30S OVT[3:0] = 1111: OV delay = 40S
1:0 **7:0**	**OV.9~OV.0**	Overvoltage threshold, calculation formula: V_{OV} = register value * 5mV

Table 8.4 Overvoltage Recovery Threshold Register

04H,05H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OVRH	UVT3	UVT2	UVT1	UVT0	-	-	OVR.9	OVR.8
OVRL	OVR.7	OVR.6	OVR.5	OVR.4	OVR.3	OVR.2	OVR.1	OVR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
3:2	**-**	**Reserved**
1:0 **7:0**	**OVR.9~OVR.0**	Overvoltage recovery threshold, calculation formula: V_{OVR} = register value * 5mV

8.3 Under Voltage Protection

When the following conditions are satisfied, SH367309 enters undervoltage protection status:

(1) Any one cell voltage is lower than V_{UV}

(2) The status (1) duration is longer than t_{UV}

When SH367309 is in the undervoltage protection status, executes the following actions:

(1) Turn off the discharge MOSFET

(2) The UV bit in the BSTATUS1 register is set to 1

(3) The UV_FLG bit in the BFLAG1 register is set to 1

EUVR=0, When the following conditions are satisfied, SH367309 exits the undervoltage protection status:

(1) All cell voltages are higher than V_{UVR}

(2) The status (1) duration is longer than t_{UVR}

EUVR=1, When the following conditions are satisfied, SH367309 exits the undervoltage protection status:

(1) All cell voltages are higher than V_{UVR}

(2) The status (1) duration is longer than t_{UVR}

(3) Load disconnected (DSGD pin voltage is lower than V_{DSGD})

When SH367309 exits the undervoltage protection status, executes the following actions:

(1) Turn on discharge MOSFET

(2) The UV bit in the BSTATUS1 register is clear

When SH367309 enters undervoltage protection status, the charge MOSFET can be turned off by configuration UV_OP bit:

(1) UV_OP = 1, after undervoltage protection, turn off the charge and discharge MOSFET, then connect the charger (CHGD pin voltage is lower than V_{CHGD1}), delay 100mS to turn on the charge MOSFET

(2) UV_OP = 0, turn off discharge MOSFET after undervoltage protection

Note: V_{UV}, V_{UVR} and t_{UV} can be set in the corresponding EEPROM register.

Table 8.5 System Configuration Register2

01H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF2	E0VB	-	UV_OP	DIS_PF	CTLC1	CTLC0	OCRA	EUVR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
5	**UV_OP**	Charge MOSFET control after undervoltage 0: Undervoltage only turn off discharge MOSFET 1: Undervoltage Turn off charge and discharge MOSFET
0	**EUVR**	Undervoltage recovery control 0: Undervoltage recovery no need to disconnect the load 1: Undervoltage recovery need to disconnect the load

Table 8.6 System Status Register1

43H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSTATUS1	WDT	PF	SC	OCC	OCD2	OCD1	UV	OV
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
1	**UV**	Undervoltage protection status 1: Protection occurring 0: Protection has not occurring

Table 8.7 System Flag Register1

70H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BFLAG1	WDT_FLG	PF_FLG	SC_FLG	OCC_FLG	LOAD_FLG	OCD_FLG	UV_FLG	OV_FLG
R/W	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
1	**UV_FLG**	Undervoltage protection flag 1: Protection occurred 0: Protection has not occurred

Table 8.8 Undervoltage Detection Delay Register

04H,05H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OVRH	UVT3	UVT2	UVT1	UVT0	-	-	OVR.9	OVR.8
OVRL	OVR.7	OVR.6	OVR.5	OVR.4	OVR.3	OVR.2	OVR.1	OVR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:4	**UVT3~UVT0**	Undervoltage detection delay configuration UVT[3:0] = 0000: UV delay = 100mS UVT[3:0] = 0001: UV delay = 200mS UVT[3:0] = 0010: UV delay = 300mS UVT[3:0] = 0011: UV delay = 400mS UVT[3:0] = 0100: UV delay = 600mS UVT[3:0] = 0101: UV delay = 800mS UVT[3:0] = 0110: UV delay = 1S UVT[3:0] = 0111: UV delay = 2S UVT[3:0] = 1000: UV delay = 3S UVT[3:0] = 1001: UV delay = 4S UVT[3:0] = 1010: UV delay = 6S UVT[3:0] = 1011: UV delay = 8S UVT[3:0] = 1100: UV delay = 10S UVT[3:0] = 1101: UV delay = 20S UVT[3:0] = 1110: UV delay = 30S UVT[3:0] = 1111: UV delay = 40S

Table 8.9 Undervoltage Threshold Register

06H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UV	UV.7	UV.6	UV.5	UV.4	UV.3	UV.2	UV.1	UV.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	UV.7~ UV.0	Undervoltage threshold, calculation formula: V_{UV} = register value * 20mV

Table 8.10 Undervoltage Recovery Threshold Register

07H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UVR	UVR.7	UVR.6	UVR.5	UVR.4	UVR.3	UVR.2	UVR.1	UVR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	UVR.7~UVR.0	Undervoltage recovery threshold, calculation formula: V_{UVR} = register value * 20mV

8.4 Overcurrent Protection

SH367309 Integrated three levels discharge overcurrent protection and a charge overcurrent protection. The operation method of the discharge overcurrent level-1 and the discharge overcurrent level-2 is the same, so the discharge overcurrent protection level-1 is taken as an example.

8.4.1 Discharge Overcurrent Level-1 Protection

When the following conditions are satisfied, SH367309 enters the discharge overcurrent level-1 protection status:

(1) The RS2-RS1 voltage is higher than V_{DOC1}

(2) The status (1) duration is longer than t_{DOC1}

When SH367309 is in the discharge overcurrent level-1 protection status, executes the following actions:

(1) Turn off the discharge MOSFET

(2) The OCD1 bit in BSTATUS1 register is set to 1

(3) The OCD_FLG bit in BFLAG1 register is set to 1

When the following conditions are satisfied, SH367309 exits the discharge overcurrent level-1 protection status:

(1) The load is disconnected (DSGD pin voltage is lower than V_{DSGD})

(2) The status (1) duration is longer than t_{D1}

8.4.2 Short Circuit Protection

When the following conditions are satisfied, SH367309 enters the short circuit protection status:

(1) The RS2-RS1 voltage is higher than V_{DOC3}

(2) The status (1) duration is longer than t_{DOC3}

When SH367309 is in the short circuit protection status, executes the following actions:

(1) Turn off the discharge MOSFET

(2) The SC bit in BSTATUS1 register is set to 1

(3) The SC_FLG bit in BFLAG1 register is set to 1

When the following conditions are satisfied, SH367309 exits the short circuit protection status:

(1) The load is disconnected (DSGD pin voltage is lower than V_{DSGD})

(2) The status (1) duration is longer than t_{D1}

8.4.3 Charge Overcurrent Protection

When the following conditions are satisfied, SH367309 enters the charge overcurrent protection status:

(1) The RS2-RS1 voltage is lower than V_{COC}

(2) The status (1) duration is longer than t_{COC}

When SH367309 is in the charge overcurrent protection status, executes the following actions:

(1) Turn off the charge MOSFET

(2) The OCC bit in BSTATUS1 register is set to 1

(3) The OCC_FLG bit in BFLAG1 register is set to 1

When the following conditions are satisfied, SH367309 exits the charge overcurrent protection status:

(1) The charger is disconnected (CHGD pin voltage is higher than V_{CHGD2})

(2) The status (1) duration is longer than t_{D2}

Note: V_{DOC1}、t_{DOC1}、V_{DOC2}、t_{DOC2}、V_{DOC3}、t_{DOC3}、V_{COC} and t_{COC} can be set in the corresponding EEPROM register.

Table 8.11 System Status Register1

43H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSTATUS1	WDT	PF	SC	OCC	OCD2	OCD1	UV	OV
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

1)

Bit Number	Symbol	Description
5	**SC**	Short circuit protection status 1: Protection occurring 0: Protection has not occurring
4	**OCC**	Charge Overcurrent protection status 1: Protection occurring 0: Protection has not occurring
3	**OCD2**	Discharge Overcurrent level-1 protection status 1: Protection occurring 0: Protection has not occurring
2	**OCD1**	Discharge Overcurrent level-2 protection status 1: Protection occurring 0: Protection has not occurring

Table 8.12 System Flag Register1

70H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BFLAG1	WDT_FLG	PF_FLG	SC_FLG	OCC_FLG	LOAD_FLG	OCD_FLG	UV_FLG	OV_FLG
R/W	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
5	**SC_FLG**	Short circuit protection flag 1: Protection occurred 0: Protection has not occurred
4	**OCC_FLG**	Charge Overcurrent protection flag 1: Protection occurred 0: Protection has not occurred
2	**OCD_FLG**	Discharge Overcurrent protection flag 1: Protection occurred 0: Protection has not occurred

Table 8.13 Discharge Overcurrent level-1 Threshold and Detection Delay Register

0CH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCD1V/OCD1T	OCD1V3	OCD1V2	OCD1V1	OCD1V0	OCD1T3	OCD1T.2	OCD1T.1	OCD1T.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**OCD1V3~ OCD1V0**	Discharge overcurrent level-1 threshold configuration OCD1V[3:0] = 0000: OCD1 threshold = 20mV OCD1V[3:0] = 0001: OCD1 threshold = 30mV OCD1V[3:0] = 0010: OCD1 threshold = 40mV OCD1V[3:0] = 0011: OCD1 threshold = 50mV OCD1V[3:0] = 0100: OCD1 threshold = 60mV OCD1V[3:0] = 0101: OCD1 threshold = 70mV OCD1V[3:0] = 0110: OCD1 threshold = 80mV OCD1V[3:0] = 0111: OCD1 threshold = 90mV OCD1V[3:0] = 1000: OCD1 threshold = 100mV OCD1V[3:0] = 1001: OCD1 threshold = 110mV OCD1V[3:0] = 1010: OCD1 threshold = 120mV OCD1V[3:0] = 1011: OCD1 threshold = 130mV OCD1V[3:0] = 1100: OCD1 threshold = 140mV OCD1V[3:0] = 1101: OCD1 threshold = 160mV OCD1V[3:0] = 1110: OCD1 threshold = 180mV OCD1V[3:0] = 1111: OCD1 threshold = 200mV
3:0	**OCD1T3~ OCD1T0**	Discharge overcurrent level-1 detection delay configuration OCD1T[3:0] = 0000: OCD1 delay = 50mS OCD1T[3:0] = 0001: OCD1 delay = 100mS OCD1T[3:0] = 0010: OCD1 delay = 200mS OCD1T[3:0] = 0011: OCD1 delay = 400mS OCD1T[3:0] = 0100: OCD1 delay = 600mS OCD1T[3:0] = 0101: OCD1 delay = 800mS OCD1T[3:0] = 0110: OCD1 delay = 1S OCD1T[3:0] = 0111: OCD1 delay = 2S OCD1T[3:0] = 1000: OCD1 delay = 4S OCD1T[3:0] = 1001: OCD1 delay = 6S OCD1T[3:0] = 1010: OCD1 delay = 8S OCD1T[3:0] = 1011: OCD1 delay = 10S OCD1T[3:0] = 1100: OCD1 delay = 15S OCD1T[3:0] = 1101: OCD1 delay = 20S OCD1T[3:0] = 1110: OCD1 delay = 30S OCD1T[3:0] = 1111: OCD1 delay = 40S

Note: Discharge overcurrent level-1 threshold is voltage of VRS2-VRS1.

Table 8.14 Discharge Overcurrent level-2 Threshold and Detection Delay Register

0DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCD2V/OCD2T	OCD2V3	OCD2V2	OCD2V1	OCD2V0	OCD2T3	OCD2T2	OCD2T1	OCD2T0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**OCD2V3~ OCD2V0**	Discharge overcurrent level-2 threshold configuration OCD2V[3:0] = 0000: OCD2 threshold = 30mV OCD2V[3:0] = 0001: OCD2 threshold = 40mV OCD2V[3:0] = 0010: OCD2 threshold = 50mV OCD2V[3:0] = 0011: OCD2 threshold = 60mV OCD2V[3:0] = 0100: OCD2 threshold = 70mV OCD2V[3:0] = 0101: OCD2 threshold = 80mV OCD2V[3:0] = 0110: OCD2 threshold = 90mV OCD2V[3:0] = 0111: OCD2 threshold = 100mV OCD2V[3:0] = 1000: OCD2 threshold = 120mV OCD2V[3:0] = 1001: OCD2 threshold = 140mV OCD2V[3:0] = 1010: OCD2 threshold = 160mV OCD2V[3:0] = 1011: OCD2 threshold = 180mV OCD2V[3:0] = 1100: OCD2 threshold = 200mV OCD2V[3:0] = 1101: OCD2 threshold = 300mV OCD2V[3:0] = 1110: OCD2 threshold = 400mV OCD2V[3:0] = 1111: OCD2 threshold = 500mV
3:0	**OCD2T3~ OCD2T0**	Discharge overcurrent level-2 detection delay configuration OCD2T[3:0] = 0000: OCD2 delay = 10mS OCD2T[3:0] = 0001: OCD2 delay = 20mS OCD2T[3:0] = 0010: OCD2 delay = 40mS OCD2T[3:0] = 0011: OCD2 delay = 60mS OCD2T[3:0] = 0100: OCD2 delay = 80mS OCD2T[3:0] = 0101: OCD2 delay = 100mS OCD2T[3:0] = 0110: OCD2 delay = 200mS OCD2T[3:0] = 0111: OCD2 delay = 400mS OCD2T[3:0] = 1000: OCD2 delay = 600mS OCD2T[3:0] = 1001: OCD2 delay = 800mS OCD2T[3:0] = 1010: OCD2 delay = 1S OCD2T[3:0] = 1011: OCD2 delay = 2S OCD2T[3:0] = 1100: OCD2 delay = 4S OCD2T[3:0] = 1101: OCD2 delay = 8S OCD2T[3:0] = 1110: OCD2 delay = 10S OCD2T[3:0] = 1111: OCD2 delay = 20S

Note: Discharge overcurrent level-2 threshold is voltage of VRS2-VRS1

Table 8.15 Short Circuit Threshold and Detection Delay Register

0EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCV/SCT	SCV3	SCV2	SCV1	SCV0	SCT3	SCT2	SCT1	SCT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**SCV3~ SCV0**	Short circuit threshold configuration SCV[3:0] = 0000: SC threshold = 50mV SCV[3:0] = 0001: SC threshold = 80mV SCV[3:0] = 0010: SC threshold = 110mV SCV[3:0] = 0011: SC threshold = 140mV SCV[3:0] = 0100: SC threshold = 170mV SCV[3:0] = 0101: SC threshold = 200mV SCV[3:0] = 0110: SC threshold = 230mV SCV[3:0] = 0111: SC threshold = 260mV SCV[3:0] = 1000: SC threshold = 290mV SCV[3:0] = 1001: SC threshold = 320mV SCV[3:0] = 1010: SC threshold = 350mV SCV[3:0] = 1011: SC threshold = 400mV SCV[3:0] = 1100: SC threshold = 500mV SCV[3:0] = 1101: SC threshold = 600mV SCV[3:0] = 1110: SC threshold = 800mV SCV[3:0] = 1111: SC threshold = 1000mV
3:0	**SCT3~ SCT0**	Short circuit detection delay configuration SCT[3:0] = 0000: SC delay = 0uS SCT[3:0] = 0001: SC delay = 64uS SCT[3:0] = 0010: SC delay = 128uS SCT[3:0] = 0011: SC delay = 192uS SCT[3:0] = 0100: SC delay = 256uS SCT[3:0] = 0101: SC delay = 320uS SCT[3:0] = 0110: SC delay = 384uS SCT[3:0] = 0111: SC delay = 448uS SCT[3:0] = 1000: SC delay = 512uS SCT[3:0] = 1001: SC delay = 576uS SCT[3:0] = 1010: SC delay = 640uS SCT[3:0] = 1011: SC delay = 704uS SCT[3:0] = 1100: SC delay = 768uS SCT[3:0] = 1101: SC delay = 832uS SCT[3:0] = 1110: SC delay = 896uS SCT[3:0] = 1111: SC delay = 960uS

Note: The short circuit protection threshold is voltage of VRS2-VRS1.

Note: The short circuit protection delay refers only to the delay of the internal circuit detection. If there is an RC filter at both terminals of the sense resistor, it will introduce a certain delay (＜50uS).

Table 8.16 Charge Overcurrent Threshold and Detection Delay Register

0FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCCV/OCCT	OCCV3	OCCV2	OCCV1	OCCV0	OCCT3	OCCT2	OCCT1	OCCT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**OCCV3~ OCCV0**	Charge overcurrent threshold configuration OCCV[3:0] = 0000: OCC threshold = 20mV OCCV[3:0] = 0001: OCC threshold = 30mV OCCV[3:0] = 0010: OCC threshold = 40mV OCCV[3:0] = 0011: OCC threshold = 50mV OCCV[3:0] = 0100: OCC threshold = 60mV OCCV[3:0] = 0101: OCC threshold = 70mV OCCV[3:0] = 0110: OCC threshold = 80mV OCCV[3:0] = 0111: OCC threshold = 90mV OCCV[3:0] = 1000: OCC threshold = 100mV OCCV[3:0] = 1001: OCC threshold = 110mV OCCV[3:0] = 1010: OCC threshold = 120mV OCCV[3:0] = 1011: OCC threshold = 130mV OCCV[3:0] = 1100: OCC threshold = 140mV OCCV[3:0] = 1101: OCC threshold = 160mV OCCV[3:0] = 1110: OCC threshold = 180mV OCCV[3:0] = 1111: OCC threshold = 200mV
3:0	**OCCT3~ OCCT0**	Charge overcurrent detection delay configuration OCCT[3:0] = 0000: OCC delay = 10mS OCCT[3:0] = 0001: OCC delay = 20mS OCCT[3:0] = 0010: OCC delay = 40mS OCCT[3:0] = 0011: OCC delay = 60mS OCCT[3:0] = 0100: OCC delay = 80mS OCCT[3:0] = 0101: OCC delay = 100mS OCCT[3:0] = 0110: OCC delay = 200mS OCCT[3:0] = 0111: OCC delay = 400mS OCCT[3:0] = 1000: OCC delay = 600mS OCCT[3:0] = 1001: OCC delay = 800mS OCCT[3:0] = 1010: OCC delay = 1S OCCT[3:0] = 1011: OCC delay = 2S OCCT[3:0] = 1100: OCC delay = 4S OCCT[3:0] = 1101: OCC delay = 8S OCCT[3:0] = 1110: OCC delay = 10S OCCT[3:0] = 1111: OCC delay = 20S

Note: The charge overcurrent protection threshold is voltage of VRS1-VRS2.

8.4.4 Overcurrent Protection Special Configuration

8.4.4.1 Overcurrent Protection Self-recovery Configuration

The OCRA bit in SCONF2 register is used to enable overcurrent protection self-recovery.

Table 8.17 System Configuration Register

01H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF2	E0VB	-	UV_OP	DIS_PF	CTLC1	CTLC0	OCRA	EUVR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
1	**OCRA**	Overcurrent protection self-recovery enable control 0: Disable 1: Enable

If the OCRA bit in SCONF2 register is set to 1, when any one of the following conditions is satisfied, SH367309 exits the overcurrent protection status:

(1) The load is disconnected and the duration is longer than t_{D1} (for discharge overcurrent)

(2) The charger is disconnected and the duration is longer than t_{D2} (for charge overcurrent)

(3) The duration after overcurrent protection is longer than the self-recovery delay t_{AUTO}

Table 8.18 Overcurrent Self-recovery Delay Register

10H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MOST/OCRT/PFT	CHS1	CHS0	MOST1	MOST0	OCRT1	OCRT0	PFT1	PFT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1)

Bit Number	Symbol	Description
3:2	**OCRT1~OCRT0**	Overcurrent self-recovery delay configuration OCRT[1:0] = 00: delay = 8S OCRT[1:0] = 01: delay = 16S OCRT[1:0] = 10: delay = 32S OCRT[1:0] = 11: delay = 64S

8.4.4.2 Overcurrent Protection Software Recovery Configuration

In AFE mode, the MCU can recovery overcurrent by writing the OCRC bit in CONF register, turn on the MOSFET:

(1) Write the OCRC bit consecutively according to the "0-1-0" timing

Table 8.19 System Configuration Register

40H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONF	OCRC	PCHMOS	DSGMOS	CHGMOS	CADCON	ENWDT	SLEEP	IDLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default (POR/WDT/LVR/PIN)	0	1	1	1	0	0	0	0

Bit Number	Symbol	Description
7	**OCRC**	Overcurrent protection software recovery control, write the OCRC bit consecutively according to the "0-1-0" timing

8.4.4.3 Overcurrent Protection Action Configuration

The OCPM bit in the SCONF register sets whether the charge and discharge MOSFET is turned off after overcurrent protection occurs.

Table 8.20 System Configuration Register1

00H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF1	ENPCH	ENMOS	OCPM	BAL	CN3	CN2	CN1	CN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
5	**OCPM**	Overcurrent MOSFET control 0: Charge overcurrent only turns off charge MOSFET discharge overcurrent and short circuit only turns off discharge MOSFET 1: Overcurrent protection turns off charge and discharge MOSFET

8.5 Temperature Protection

Temperature protection includes charge overtemperature and undertemperature, discharge overtemperature and undertemperature.

8.5.1 Charge Overtemperature Protection

When the following conditions are satisfied, SH367309 enters charge overtemperature protection status:

(1) Any one temperature is higher than T_{OTC}

(2) The status (1) duration is longer than t_T

When SH367309 is in the charge overtemperature protection status, executes the following actions:

(1) Turn off the charge MOSFET

(2) The OTC bit in the BSTATUS2 register is set to 1

(3) The OTC_FLG bit in the BFLAG2 register is set to 1

When the following conditions are satisfied, SH367309 exits the charge overtemperature protection status:

(1) All temperatures are lower than T_{OTCR}

(2) The status (1) duration is longer than t_T

When SH367309 exits the charge overtemperature protection status, executes the following actions:

(1) Turn on charge MOSFET

(2) The OTC bit in the BSTATUS2 register is clear

8.5.2 Charge Undertemperature Protection

When the following conditions are satisfied, SH367309 enters charge undertemperature protection status:

(1) Any one temperature is lower than T_{UTC}

(2) The status (1) duration is longer than t_T

When SH367309 is in the charge undertemperature protection status, executes the following actions:

(1) Turn off the charge MOSFET

(2) The UTC bit in the BSTATUS2 register is set to 1

(3) The UTC_FLG bit in the BFLAG2 register is set to 1

When the following conditions are satisfied, SH367309 exits the charge undertemperature protection status:

(1) All temperatures are higher than T_{UTCR}

(2) The status (1) duration is longer than t_T

When SH367309 exits the charge undertemperature protection status, executes the following actions:

(1) Turn on charge MOSFET

(2) The UTC bit in the BSTATUS2 register is clear

8.5.3 Discharge Overtemperature Protection

When the following conditions are satisfied, SH367309 enters discharge overtemperature protection status:

(1) Any one temperature is higher than T_{OTD}

(2) The status (1) duration is longer than t_T

When SH367309 is in the discharge overtemperature protection status, executes the following actions:

(1) Turn off the discharge MOSFET

(2) The OTD bit in the BSTATUS2 register is set to 1

(3) The OTD_FLG bit in the BFLAG2 register is set to 1

When the following conditions are satisfied, SH367309 exits the discharge overtemperature protection status:

(1) All temperatures are lower than T_{OTDR}

(2) The status (1) duration is longer than t_T

When SH367309 exits the discharge overtemperature protection status, executes the following actions:

(1) Turn on discharge MOSFET

(2) The OTD bit in the BSTATUS2 register is clear

8.5.4 Discharge Undertemperature Protection

When the following conditions are satisfied, SH367309 enters discharge undertemperature protection status:

(1) Any one temperature is lower than T_{UTD}

(2) The status (1) duration is longer than t_T

When SH367309 is in the discharge undertemperature protection status, executes the following actions:

(1) Turn off the discharge MOSFET

(2) The UTD bit in the BSTATUS2 register is set to 1

(3) The UTD_FLG bit in the BFLAG2 register is set to 1

When the following conditions are satisfied, SH367309 exits the discharge undertemperature protection status:

(1) All temperatures are higher than T_{UTDR}

(2) The status (1) duration is longer than t_T

When SH367309 exits the discharge undertemperature protection status, executes the following actions:

(1) Turn on discharge MOSFET

(2) The UTD bit in the BSTATUS2 register is clear

Note: T_{OTC}、T_{OTCR}、T_{UTC}、T_{UTCR}、T_{OTD}、T_{OTDR}、T_{UTD}、T_{UTDR} can be set in the corresponding EEPROM register.

Table 8.21 System Status Register2

44H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSTATUS2	-	-	-	-	OTD	UTD	OTC	UTC
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

1)

Bit Number	Symbol	Description
7:4	**-**	Reserved
3	**OTD**	Discharge overtemperature protection status 1: Protection occurring 0: Protection has not occurring
2	**UTD**	Discharge undertemperature protection status 1: Protection occurring 0: Protection has not occurring
1	**OTC**	Charge overtemperature protection status 1: Protection occurring 0: Protection has not occurring
0	**UTC**	Charge undertemperature protection status 1: Protection occurring 0: Protection has not occurring

Table 8.22 System Flag Register2

71H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BFLAG2	RST_FLG	WAKE_FLG	CADC_FLG	VADC_FLG	OTD_FLG	UTD_FLG	OTC_FLG	UTC_FLG
R/W	R/W“0”	R/W“0”	R	R	R/W“0”	R/W“0”	R/W“0”	R/W”0”
Default	1	0	0	0	0	0	0	0

2)

Bit Number	Symbol	Description
3	**OTD_FLG**	Discharge overtemperature protection flag 1: Protection occurred 0: Protection has not occurred
2	**UTD_FLG**	Discharge undertemperature protection flag 1: Protection occurred 0: Protection has not occurred
1	**OTC_FLG**	Charge overtemperature protection flag 1: Protection occurred 0: Protection has not occurred
0	**UTC_FLG**	Charge undertemperature protection flag 1: Protection occurred 0: Protection has not occurred

Table 8.23 Charge Overtemperature Threshold Register

11H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTC	OTC7	OTC6	OTC5	OTC4	OTC3	OTC2	OTC1	OTC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0	**OTC7~OTC0**	Charge overtemperature threshold configuration

Table 8.24 Charge Overtemperature Recovery Threshold Register

12H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTCR	OTCR7	OTCR6	OTCR5	OTCR4	OTCR3	OTCR2	OTCR1	OTCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**OTCR7~OTCR0**	Charge overtemperature recovery threshold configuration

Table 8.25 Charge Undertemperature Threshold Register

13H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UTC	UTC7	UTC6	UTC5	UTC4	UTC3	UTC2	UTC1	UTC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**UTC7~UTC0**	Charge undertemperature threshold configuration

Table 8.26 Charge Undertemperature Recovery Threshold Register

14H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UTCR	UTCR7	UTCR6	UTCR5	UTCR4	UTCR3	UTCR2	UTCR1	UTCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**UTCR7~UTCR0**	Charge undertemperature recovery threshold configuration

Table 8.27 Discharge Overtemperature Threshold Register

15H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTD	OTD7	OTD6	OTD5	OTD4	OTD3	OTD2	OTD1	OTD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**OTD7~OTD0**	Discharge overtemperature threshold configuration

Table 8.28 Discharge Overtemperature Recovery Threshold Register

16H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTDR	OTDR7	OTDR6	OTDR5	OTDR4	OTDR3	OTDR2	OTDR1	OTDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**OTDR7~OTDR0**	Discharge overtemperature recovery threshold configuration

Table 8.29 Discharge Undertemperature Threshold Register

17H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UTD	UTD7	UTD6	UTD5	UTD4	UTD3	UTD2	UTD1	UTD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**UTD7~UTD0**	Discharge undertemperature threshold configuration

Table 8.30 Discharge Undertemperature Recovery Threshold Register

18H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UTDR	UTDR7	UTDR6	UTDR5	UTDR4	UTDR3	UTDR2	UTDR1	UTDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**UTDR7~UTDR0**	Discharge undertemperature recovery threshold configuration

8.5.5 Temperature Protection Threshold Calculation

(1) Overtemperature and recovery threshold calculation formula:

$$\text{Threshold (OTC, OTCR, OTD, OTDR)} = \frac{R_{T1}}{R_{REF} + R_{T1}} \times 512$$

(2) Undertemperature and recovery threshold calculation formula:

$$\text{Threshold (UTC, UTCR, UTD, UTDR)} = \left(\frac{R_{T1}}{R_{REF}+R_{T1}}-0.5\right)\times 512$$

R_{T1} is the thermistor resistance corresponding to the temperature protection threshold (unit is KΩ), R_{REF} is the internal reference resistance (unit is KΩ).

The R_{REF} is calculated as:

$$R_{REF}=6.8+0.05*TR[6:0]$$

Table 8.31 Internal Reference Resistance Coefficient Register

19H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TR	-	TR6	TR5	TR4	TR3	TR2	TR1	TR0
R	-	R	R	R	R	R	R	R

Bit Number	Symbol	Description
7	**-**	Reserved
6:0	**TR6~ TR0**	Internal reference resistance coefficient

8.6 Secondary Overvoltage Protection

If the DIS_PF bit in the SCONF2 register is clear, when the following conditions are satisfied, SH367309 enters secondary overvoltage protection status:

(1) Any one cell voltage is higher than V_{P2N}

(2) The status (1) duration is longer than t_{P2N}

When SH367309 is in the secondary overvoltage protection status, not allowed to enter powerdown state and SLEEP state, and executes the following actions:

(1) Turn off the charge and discharge MOSFET

(2) Turn off the VADC and CADC modules (data before the VADC and CADC related register values are held)

(3) PF pin output VSS

(4) The PF bit in the BSTATUS1 register is set to 1

(5) The PF_FLG bit in the BFLAG1 register is set to 1

When any one of the following conditions is satisfied, SH367309 exits the secondary overvoltage protection status:

(1) System is powered on again

(2) Software reset

(3) Enter SHIP mode and exit SHIP mode

Note: V_{P2N} and t_{P2N} can be set in the corresponding EEPROM register.

Table 8.32 System Configuration Register2

01H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF2	E0VB	-	UV_OP	DIS_PF	CTLC1	CTLC0	OCRA	EUVR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
4	**DIS_PF**	Secondary overvoltage protection enable control 0: Enable 1: Disable

Table 8.33 System Status Register1

43H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSTATUS1	WDT	PF	SC	OCC	OCD2	OCD1	UV	OV
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
6	**PF**	Secondary overvoltage protection status 1: Protection occurring 0: Protection has not occurring

Table 8.34 System Flag Register1

70H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BFLAG1	WDT_FLG	PF_FLG	SC_FLG	OCC_FLG	LOAD_FLG	OCD_FLG	UV_FLG	OV_FLG
R/W	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
6	**PF_FLG**	Secondary overvoltage protection flag 1: Protection occurred 0: Protection has not occurred

Table 8.35 Secondary Overvoltage Threshold Register

0BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PFV	PFV.7	PFV.6	PFV.5	PFV.4	PFV.3	PFV.2	PFV.1	PFV.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	PFV.7~ PFV.0	Secondary overvoltage threshold, calculation formula: V_{P2N} = register value * 20mV

Table 8.36 Secondary Overvoltage Detection Delay Register

10H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MOST/OCRT/PFT	CHS1	CHS0	MOST1	MOST0	OCRT1	OCRT0	PFT1	PFT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
1:0	**PFT1~PFT0**	Secondary overvoltage detection delay configuration PFT[1:0] = 00: PF delay = 8S PFT[1:0] = 01: PF delay = 16S PFT[1:0] = 10: PF delay = 32S PFT[1:0] = 11: PF delay = 64S

8.7 Broken-wire Protection

If the DIS_PF bit in the SCONF2 register is clear, enable broken-wire protection function.When SH367309 is in broken-wire protection status, not allowed to enter powerdown state and SLEEP state, and executes the following actions:

(1) Turn off the charge and discharge MOSFET

(2) Turn off the VADC and CADC modules (data before the VADC and CADC related register values are held)

(3) PF pin output VSS

(4) The PF bit in the BSTATUS1 register is set to 1

(5) The PF_FLG bit in the BFLAG1 register is set to 1

When any one of the following conditions is satisfied, SH367309 exits the broken-wire protection status:

(1) System is powered on again

(2) Software reset

(3) Enter SHIP mode and exit SHIP mode

Note: V_{P2N} and t_{P2N} can be set in the corresponding EEPROM register.

8.8 Low Voltage Prohibition Charge

The E0VB bit in SCONF2 register is used to enable low voltage prohibition charge.

Table 8.37 System Configuration Register2

01H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF2	E0VB	-	UV_OP	DIS_PF	CTLC1	CTLC0	OCRA	EUVR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7	**E0VB**	Low voltage prohibition charge enable control 0: Allow low voltage charge 1: Prohibit low voltage charge

When low voltage prohibition charge is enables, the following conditions are satisfied, SH367309 turns off the charge MOSFET:

(1) Any one cell voltage is lower than V_{L0V}

(2) The status (1) duration is longer than 10* t_{cycle}

Note: V_{L0V} can be set in the corresponding EEPROM register.

Table 8.38 Low Voltage Prohibition Charge Threshold Register

0AH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
L0V	-	L0V.6	L0V.5	L0V.4	L0V.3	L0V.2	L0V.1	L0V.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	L0V.6~ L0V.0	Low voltage prohibition charge threshold, calculation formula: V_{L0V} = register value * 20mV

8.9 Balance

SH367309 integrated balance switch, the BAL bit in SCONF1 register can set the operating mode.

Table 8.39 System Configuration Register1

00H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF1	ENPCH	ENMOS	OCPM	BAL	CN3	CN2	CN1	CN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
4	**BAL**	Balance control 0: Balance switch is controlled by SH367309 internal logic 1:Balance switch is controlled by MCU, balance timing is controlled by SH367309 internal logic

If the balance switch is controlled by SH367309, when the following conditions are satisfied, the balance of CELLn is turned on:

(1) No temperature protection occurred

(2) No secondary overvoltage protection occurred

(3) CELLn voltage is higher than V_{BAL}

(4) The status (1) ~ (3) duration is longer than $t_{balanceT}$

When any one of the following conditions is satisfied, SH367309 turned off CELLn balance:

(1) CELLn voltage is lower than V_{BAL}

(2) Temperature protection occurs

(3) Secondary overvoltage protection occurs

Note: V_{BAL} can be set in the corresponding EEPROM register.

SH367309 internal balance to take odd and even balance timing, as shown below:

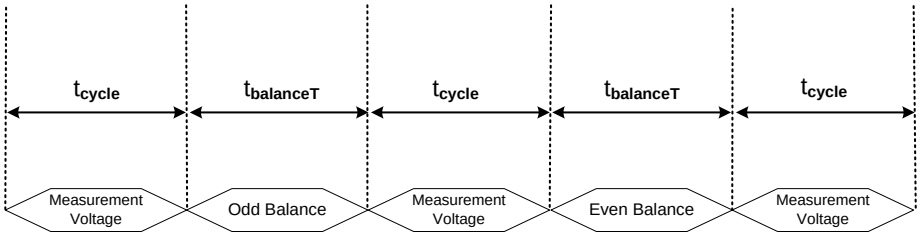


Fig 11. Odd and even balance timing

Table 8.40 Balance Threshold Register

08H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BALV	BALV.7	BALV.6	BALV.5	BALV.4	BALV.3	BALV.2	BALV.1	BALV.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	BALV.7~ BALV.0	Balance threshold, calculation formula: VBAL= register value * 20mV

9. AFE Mode

In AFE Mode, SH367309 enable the TWI module. ADC and TWI module introduced in chapter 12.

9.1 Balance Control Function

In AFE Mode, when the BAL bit in the SCONF1 register is set to 1, MCU can control the balance module.

Table 9.1 System Configuration Register 1

00H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF1	ENPCH	ENMOS	OCPM	BAL	CN3	CN2	CN1	CN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
4	**BAL**	Balance control 0: Balance switch is controlled by SH367309 internal logic 1:Balance switch is controlled by MCU, balance timing is controlled by SH367309 internal logic

When the balance is controlled by MCU, any bit is set to 1, SH367309 balance module is turned on: the balanced path corresponding to the set control bit in the BALANCE register is turned on. When the balance lasts for 1 minute, the balance is automatically stopped and all the bits in the BALANCE register are cleared. If the balance needs to be continued, the MCU needs to reconfigure the BALANCE register.

Note: During the balancing process, any bit in the BALANCE register is set to 1 and it will restart for 1 minute.

Table 9.2 Balance Register

41H,42H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BALANCEH	CB16	CB15	CB14	CB13	CB12	CB11	CB10	CB9
BALANCEL	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
15:0	CBn	Balance control 1: Turn on CELLn balance 0: Turn off CELLn balance

9.2 Charging and Discharging Status

When the following conditions are satisfied, SH367309 determines that the system is in the charging status:

(1) (RS2-RS1) voltage ≤ $-V_{CH}$

(2) The status (1) duration is longer than 2* t_{cycle}

In the charging status, the CHGING bit in the BSTATUS3 register is set to 1.

When the following conditions are satisfied, SH367309 determines that the system is in the discharging status:

(1) (RS2-RS1) voltage ≥ V_{CH}

(2) The status (1) duration is longer than 2* t_{cycle}

In the discharging status, the DSGING bit in the BSTATUS3 register is set to 1.

When the CHGING and DSGING bit in the BSTATUS3 register are cleared, SH367309 determines that the system is in a static status.

Table 9.3 System Status Register3

45H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSTATUS3	CHGING	DSGING	-	-	L0V	PCHG_FET	CHG_FET	DSG_FET
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7	**CHGING**	Charging status 1: Charging 0: Non-charging
6	**DSGING**	Discharging status 1: Discharging 0: Non-Discharging

9.3 Watchdog (WDT)

The SH367309 built in watchdog, but the watchdog is enabled only in the AFE mode. The watchdog timer is a down counter. The valid TWI communication resets the watchdog counter and starts counting again.

When the watchdog timer overflows, SH367309 executes the following actions:

(1) Turn off charge and discharge MOSFET

(2) Clear balance control registers BALANCEH and BALANCEL

When any one of the following conditions is satisfied, SH367309 release the watchdog overflow status:

(1) The valid TWI communication

(2) SH367309 Reset

The entry and exit (except reset) of watchdog overflow, does not clear any protection status.

The RSTSTAT register can set the watchdog timeout, and the ENWDT bit in the CONF register is used to enable the watchdog module.

Table 9.4 Watchdog Register

72H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	-	-	-	-	-	-	WDT.1	WDT.0
R/W	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
1:0	**WDT.1~ WDT.0**	Watchdog overflow time configuration WDT[1:0]=00: watchdog overflow time is 32S WDT[1:0]=01: watchdog overflow time is 16S WDT[1:0]=10: watchdog overflow time is 8S WDT[1:0]=11: watchdog overflow time is 4S

Table 9.5 System Configuration Register

40H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONF	OCRC	PCHMOS	DSGMOS	CHGMOS	CADCON	ENWDT	SLEEP	IDLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default (POR/WDT/LVR/PIN)	0	1	1	1	0	0	0	0

Bit Number	Symbol	Description
2	**ENWDT**	Watchdog enable control 0: Disable 1: Enable

10. MOSFET driver

SH367309 integrated N-MOSFET driver, include discharge, charge and precharge N-MOSFET driver.

Table3. MOSFET Drive

Pin	Description	High level	Low level
DSG	Discharge MOSFET Driver Pin	V_{DSGH}	V_{DSGL}
CHG	Charge MOSFET Driver Pin	V_{CHGH}	High impedance
PCHG	Precharge MOSFET Driver Pin	V_{PCHGH}	High impedance

The status of the MOSFET can be viewed in the BSTATUS3 register.

Table 10.1 System Status Register3

45H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSTATUS3	CHGING	DSGING	-	-	L0V	PCHG_FET	CHG_FET	DSG_FET
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
2	**PCHG_FET**	Precharge MOSFET status 1: On 0: Off
1	**CHG_FET**	Charge MOSFET status 1: On 0: Off
0	**DSG_FET**	Discharge MOSFET status 1: On 0: Off

Table 10.2 System Configuration Register

The MCU can control the MOSFET drive to turn off or on by configuring the corresponding bits of the CONF register, when these PCHMOS/DSGMOS/CHGMOS bits of the CONF register are 1, the MOSFET switch is controlled by the SH367309 internal logic.

40H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONF	OCRC	PCHMOS	DSGMOS	CHGMOS	CADCON	ENWDT	SLEEP	IDLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default (POR/WDT/LVR/PIN)	0	1	1	1	0	0	0	0

Bit Number	Symbol	Description
6	**PCHMOS**	Precharge MOSFET control 0: Off 1: Precharge MOSFET is cotroled by hardware protection
5	**DSGMOS**	Discharge MOSFET control 0: Off 1: Discharge MOSFET is controlled by hardware protection
4	**CHGMOS**	Charge MOSFET control 0: Off 1: Charge MOSFET is controlled by hardware protection

10.1 Precharge MOSFET

The ENPCH bit in SOCNF1 register is used to enable precharge.

Table 10.3 System Configuration Register1

00H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF1	ENPCH	ENMOS	OCPM	BAL	CN3	CN2	CN1	CN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7	**ENPCH**	Precharge enable control 0: Disable 1: Enable

When ENPCH = 1, turn on the precharge MOSFET when the following conditions are satisfied:

(1) In the undervoltage status, any cell voltage is lower than the V_{PCH} and the duration is longer than the t_{PCHG}

(2) No overvoltage protection, charge overtemperature and undertemperature protection, charge overcurrent protection, discharge overcurrent (OCPM = 1), secondary overvoltage protection

(3) CTL pin uncontrolled precharge MOSFET

(4) Watchdog does not overflow (this condition is invalid in the protection mode)

(5) The PCHMOS bit in the CONF register is set to 1(this condition is invalid in the protection mode)

(6) Turn off the low voltage prohibition charge, or the low voltage prohibition charge is valid, but all cell voltages are higher than the V_{L0V}

SH367309 turns off the charge MOSFET when the precharge MOSFET is on. In the precharging process, the balance is effective.

When any one of the following conditions is satisfied, turn off the precharge MOSFET:

(1) Any one cell is higher than V_{PCH} and the duration is longer than 2* t_{cycle}

(2) Overvoltage protection, charge overtemperature and undertemperature protection, charge overcurrent protection, discharge overcurrent protection (OCPM = 1), and secondary overvoltage protection

(3) CTL pin control precharge MOSFET off

(4) Watchdog register overflow (this condition is invalid in the protection mode)

(5) The PCHMOS control bit in the CONF register is set to 0 (this condition is invalid in the protection mode)

(6) The low voltage prohibition charge is valid, and at this time, the cell voltage is lower than V_{L0V}

Note: V_{PCH} and the precharge enabled can be set in the corresponding EEPROM register.

Table 10.4 Precharge Voltage Threshold Register

09H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PREV	PREV.7	PREV.6	PREV.5	PREV.4	PREV.3	PREV.2	PREV.1	PREV.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	PREV.7~ PREV.0	Precharge threshold, calculation formula: V_{PCH} = register value * 20mV

10.2 Force Turn On Charge MOSFET

The ENMOS bit in the SCONF1 register can be set SH367309 forced turn on charge MOSFET.

Table 10.5 System Configuration Register1

00H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF1	ENPCH	ENMOS	OCPM	BAL	CN3	CN2	CN1	CN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
6	**ENMOS**	Charge MOSFET recovery control 0: Disable 1: Enable When the charge overtemperature and undertemperature protection turns off the charge MOSFET, if the discharge overcurrent1 or discharging status is detected, the charge MOSFET is turned on

ENMOS=1, SH367309 turns on the charge MOSFET when any one of the following conditions is satisfied

(1) Discharge current exceeds the discharge overcurrent1 and the duration is longer than t_{MOSFET}

(2) The discharging status is detected

If the above conditions are not satisfied, the corresponding protection status is not released and the charge MOSFET is turned on, turn off the charge MOSFET after delay of 10mS.

11. Pin function

11.1 CTL Pin

The charge and discharge MOSFET can be controlled by the CTL pin of SH367309. The CTL pin can be configured by CTLC[1:0] of the SCONF2 register.

Table 11.1 System Configuration Register2

01H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF2	E0VB	-	UV_OP	DIS_PF	CTLC1	CTLC0	OCRA	EUVR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
3:2	**CTLC1~0**	CTL pin configuration control CTLC[1:0] = 00: Do not control any MOSFET, CTL pin input is invalid CTLC[1:0] = 01: Control the charge and precharge MOSFET CTLC[1:0] = 10: Control the discharge MOSFET CTLC[1:0] = 11: Control charge and discharge and pre-charge MOSFET

CTL pin input and control is shown in the following table:

Table4. CTL Pin Function

CTL pin input	MOSFET status
High level ($V_{H\text{-}CTL}$)	Depend on SH367309 internal logic
Low level ($V_{L\text{-}CTL}$)	Turn off the corresponding MOSFET

11.2 LDO_EN Pin

LDO_EN pin enable SH367309 LDO3:

Table5. LDO_EN Pin Function

LDO_EN pin input	LDO3
High level ($V_{H\text{-}LDO\_EN}$)	Enable
Low level ($V_{L\text{-}LDO\_EN}$)	Disable

11.3 MODE Pin

MODE pin configuration SH367309 works in AFE or protect mode:

Table6. MODE Pin Function

MODE pin input	SH367309 operating mode
High level ($V_{H\text{-}MODE}$)	AFE
Low level ($V_{L\text{-}MODE}$)	Protect

11.4 ALARM pin

In protect mode, ALARM pin is in high impedance status.

In AFE mode, ALARM pin can communicate with external, the ALARM pin outputs normal high. The system status in the following table appears and the ALARM pin outputs a low level pulse.

Table7. ALARM pin function

System status (status bit from 0→1)	ALARM pin output
VADC measurement completed(period: 100mS)	Low pulse
CADC measurement completed (period: 250mS)	Low pulse
Overvoltage/Undervoltage protection occurs	Low pulse
Charge overcurrent / Discharge overcurrent / Short circuit protection occurs	Low pulse
Temperature protection occurs	Low pulse
Secondary overvoltage protection occurs	Low pulse
Watchdog overflow	Low pulse
External LDO3 overcurrent protection occurs	Low pulse
Current wakes up IDLE status	Low pulse
Charger connection wake up SLEEP status	Low pulse

The ALARM pin low level pulse timing diagram is as follows:

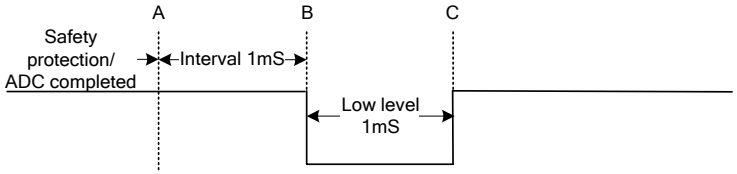


Fig 12. External communication of ALARM pin

11.5 STA Detection

In AFE mode, SH367309 is in IDLE status or SLEEP status, the system will turn on STA detection. When SH367309 receives the start signal of the TWI communication, SH367309 pulls down the SCL pin, exits the IDLE or SLEEP status, and simultaneously releases the SCL pin. At the same time, the WAKE_FLG bit in the BFLAG2 register is set to 1.

12. Function Module

12.1 VADC for Cell Voltage and Temperature Measurements

12.1.1 Features

- 13-bit Σ-Δ analog-to-digital converter
- 10Hz measurement frequency
- 20-channel measurements

12.1.2 Measurement Range and Result Registers

SH367309 Built-in VADC has 20 measurement channels: 16 channels for cell voltage, 1 channel for current and 3 channels for temperature.

Cell voltage measurements range: 0~5V;

Current measurement range: -0.2~0.2V;

Temperature measurements range: 0~3.0V.

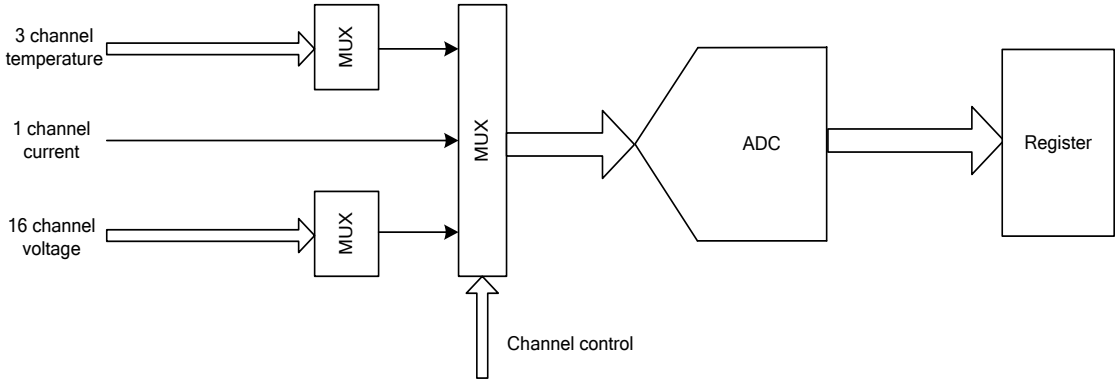


Fig 13. VADC channel diagram

The cell voltage measurement results of VADC are stored in the register in the form of cell voltage value, and the result is a signed 16-bit data. CELL1 is the cell near VSS, CELL16 is the cell near VBAT; the temperature measurement results are the ratio of temperature resistance to voltage divider, the result is a signed 16-bit data; the current is stored in the register in the form of a measurement resistor voltage, and the result is a signed 16-bit data.

All VADC measurement results are stored in dedicated registers, as follows:

Table 12.1 Cell1 Voltage Measurement Register

4EH,4FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL1H	CELL1.15	CELL1.14	CELL1.13	CELL1.12	CELL1.11	CELL1.10	CELL1.9	CELL1.8
CELL1L	CELL1.7	CELL1.6	CELL1.5	CELL1.4	CELL1.3	CELL1.2	CELL1.1	CELL1.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL1.15- CELL1.0	When the measurement is completed, the data is updated to the value of the Cell1

Table 12.2 Cell2 Voltage Measurement Register

50H,51H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL2H	CELL2.15	CELL2.14	CELL2.13	CELL2.12	CELL2.11	CELL2.10	CELL2.9	CELL2.8
CELL2L	CELL2.7	CELL2.6	CELL2.5	CELL2.4	CELL2.3	CELL2.2	CELL2.1	CELL2.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL2.15- CELL2.0	When the measurement is completed, the data is updated to the value of the Cell2

Table 12.3 Cell3 Voltage Measurement Register

52H,53H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL3H	CELL3.15	CELL3.14	CELL3.13	CELL3.12	CELL3.11	CELL3.10	CELL3.9	CELL3.8
CELL3L	CELL3.7	CELL3.6	CELL3.5	CELL3.4	CELL3.3	CELL3.2	CELL3.1	CELL3.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL3.15- CELL3.0	When the measurement is completed, the data is updated to the value of the Cell3

Table 12.4 Cell4 Voltage Measurement Register

54H,55H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL4H	CELL4.15	CELL4.14	CELL4.13	CELL4.12	CELL4.11	CELL4.10	CELL4.9	CELL4.8
CELL4L	CELL4.7	CELL4.6	CELL4.5	CELL4.4	CELL4.3	CELL4.2	CELL4.1	CELL4.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL4.15- CELL4.0	When the measurement is completed, the data is updated to the value of the Cell4

Table 12.5 Cell5 Voltage Measurement Register

56H,57H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL5H	CELL5.15	CELL5.14	CELL5.13	CELL5.12	CELL5.11	CELL5.10	CELL5.9	CELL5.8
CELL5L	CELL5.7	CELL5.6	CELL5.5	CELL5.4	CELL5.3	CELL5.2	CELL5.1	CELL5.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL5.15- CELL5.0	When the measurement is completed, the data is updated to the value of the Cell5

Table 12.6 Cell6 Voltage Measurement Register

58H,59H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL6H	CELL6.15	CELL6.14	CELL6.13	CELL6.12	CELL6.11	CELL6.10	CELL6.9	CELL6.8
CELL6L	CELL6.7	CELL6.6	CELL6.5	CELL6.4	CELL6.3	CELL6.2	CELL6.1	CELL6.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL6.15- CELL6.0	When the measurement is completed, the data is updated to the value of the Cell6

Table 12.7 Cell7 Voltage Measurement Register

5AH,5BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL7H	CELL7.15	CELL7.14	CELL7.13	CELL7.12	CELL7.11	CELL7.10	CELL7.9	CELL7.8
CELL7L	CELL7.7	CELL7.6	CELL7.5	CELL7.4	CELL7.3	CELL7.2	CELL7.1	CELL7.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL7.15- CELL7.0	When the measurement is completed, the data is updated to the value of the Cell7

Table 12.8 Cell8 Voltage Measurement Register

5CH,5DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL8H	CELL8.15	CELL8.14	CELL8.13	CELL8.12	CELL8.11	CELL8.10	CELL8.9	CELL8.8
CELL8L	CELL8.7	CELL8.6	CELL8.5	CELL8.4	CELL8.3	CELL8.2	CELL8.1	CELL8.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL8.15- CELL8.0	When the measurement is completed, the data is updated to the value of the Cell8

Table 12.9 Cell9 Voltage Measurement Register

5EH,5FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL9H	CELL9.15	CELL9.14	CELL9.13	CELL9.12	CELL9.11	CELL9.10	CELL9.9	CELL9.8
CELL9L	CELL9.7	CELL9.6	CELL9.5	CELL9.4	CELL9.3	CELL9.2	CELL9.1	CELL9.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL9.15- CELL9.0	When the measurement is completed, the data is updated to the value of the Cell9

Table 12.10 Cell10 Voltage Measurement Register

60H,61H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL10H	CELL10.15	CELL10.14	CELL10.13	CELL10.12	CELL10.11	CELL10.10	CELL10.9	CELL10.8
CELL10L	CELL10.7	CELL10.6	CELL10.5	CELL10.4	CELL10.3	CELL10.2	CELL10.1	CELL10.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL10.15- CELL10.0	When the measurement is completed, the data is updated to the value of the Cell10

Table 12.11 Cell11 Voltage Measurement Register

62H,63H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL11H	CELL11.15	CELL11.14	CELL11.13	CELL11.12	CELL11.11	CELL11.10	CELL11.9	CELL11.8
CELL11L	CELL11.7	CELL11.6	CELL11.5	CELL11.4	CELL11.3	CELL11.2	CELL11.1	CELL11.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL11.15- CELL11.0	When the measurement is completed, the data is updated to the value of the Cell11

Table 12.12 Cell12 Voltage Measurement Register

64H,65H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL12H	CELL12.15	CELL12.14	CELL12.13	CELL12.12	CELL12.11	CELL12.10	CELL12.9	CELL12.8
CELL12L	CELL12.7	CELL12.6	CELL12.5	CELL12.4	CELL12.3	CELL12.2	CELL12.1	CELL12.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL12.15- CELL12.0	When the measurement is completed, the data is updated to the value of the Cell12

Table 12.13 Cell13 Voltage Measurement Register

66H,67H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL13H	CELL13.15	CELL13.14	CELL13.13	CELL13.12	CELL13.11	CELL13.10	CELL13.9	CELL13.8
CELL13L	CELL13.7	CELL13.6	CELL13.5	CELL13.4	CELL13.3	CELL13.2	CELL13.1	CELL13.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL13.15- CELL13.0	When the measurement is completed, the data is updated to the value of the Cell13

Table 12.14 Cell14 Voltage Measurement Register

68H,69H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL14H	CELL14.15	CELL14.14	CELL14.13	CELL14.12	CELL14.11	CELL14.10	CELL14.9	CELL14.8
CELL14L	CELL14.7	CELL14.6	CELL14.5	CELL14.4	CELL14.3	CELL14.2	CELL14.1	CELL14.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL14.15- CELL14.0	When the measurement is completed, the data is updated to the value of the Cell14

Table 12.15 Cell15 Voltage Measurement Register

6AH,6BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL15H	CELL15.15	CELL15.14	CELL15.13	CELL15.12	CELL15.11	CELL15.10	CELL15.9	CELL15.8
CELL15L	CELL15.7	CELL15.6	CELL15.5	CELL15.4	CELL15.3	CELL15.2	CELL15.1	CELL15.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL15.15- CELL15.0	When the measurement is completed, the data is updated to the value of the Cell15

Table 12.16 Cell16 Voltage Measurement Register

6CH,6DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CELL16H	CELL16.15	CELL16.14	CELL16.13	CELL16.12	CELL16.11	CELL16.10	CELL16.9	CELL16.8
CELL16L	CELL16.7	CELL16.6	CELL16.5	CELL16.4	CELL16.3	CELL16.2	CELL16.1	CELL16.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CELL16.15- CELL16.0	When the measurement is completed, the data is updated to the value of the Cell16

Table 12.17 T1 Temperature Measurement Register

46H,47H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TEMP1H	TEMP1.15	TEMP1.14	TEMP1.13	TEMP1.12	TEMP1.11	TEMP1.10	TEMP1.9	TEMP1.8
TEMP1L	TEMP1.7	TEMP1.6	TEMP1.5	TEMP1.4	TEMP1.3	TEMP1.2	TEMP1.1	TEMP1.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	TEMP1.15- TEMP1.0	When the measurement is completed, the data is updated to the temperature resistance 1 voltage divider ratio

Table 12.18 T2 Temperature Measurement Register

48H,49H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TEMP2H	TEMP2.15	TEMP2.14	TEMP2.13	TEMP2.12	TEMP2.11	TEMP2.10	TEMP2.9	TEMP2.8
TEMP2L	TEMP2.7	TEMP2.6	TEMP2.5	TEMP2.4	TEMP2.3	TEMP2.2	TEMP2.1	TEMP2.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	TEMP2.15- TEMP2.0	When the measurement is completed, the data is updated to the temperature resistance 2 voltage divider ratio

Table 12.19 T3 Temperature Measurement Register

4AH,4BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TEMP3H	TEMP3.15	TEMP3.14	TEMP3.13	TEMP3.12	TEMP3.11	TEMP3.10	TEMP3.9	TEMP3.8
TEMP3L	TEMP3.7	TEMP3.6	TEMP3.5	TEMP3.4	TEMP3.3	TEMP3.2	TEMP3.1	TEMP3.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	TEMP3.15- TEMP3.0	When the measurement is completed, the data is updated to the temperature resistance 3 voltage divider ratio

Table 12.20 Current Measurement Register

4CH,4DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CURH	CUR.15	CUR.14	CUR.13	CUR.12	CUR.11	CUR.10	CUR.9	CUR.8
CURL	CUR.7	CUR.6	CUR.5	CUR.4	CUR.3	CUR.2	CUR.1	CUR.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CUR.15- CUR.0	CUR15 is a sign bit, "1" indicates discharge; "0" indicates charge. When the measurement is completed, the data is updated to the value corresponding to the voltage across the sense resistor

12.1.3 Voltage/Temperature/Current Calculation Formula

According to the VADC measurement result, the cell voltage, temperature value and current value can be calculated.

(1) Cell voltage calculation formula, using CELL1 as an example (Unit: mV, CELL1 is the CELL1 register value):

$$V_{CELL1}=CELL1\times\frac{5}{32}$$

(2) Temperature calculation formula, using TEMP1 as an example (Unit: KΩ, R_{T1} is the external thermistor resistance, R_{REF} is the internal reference resistance, TEMP1 is the TEMP1 register value, which can be based on the resistance between the external thermistor resistance RT1 and the temperature relationship to obtain true temperature value):

$$R_{T1}=\frac{TEMP1}{32768\text{-}TEMP1}\times R_{REF}$$

The internal reference resistor R_{REF} is calculated (Unit: KΩ, TR[6:0] is the lower 7 bits of register TR):

$$R_{REF}=6.8+0.05*TR[6:0]$$

(3) Current is calculated (Unit: mA, CUR is the CUR register value and R_{SENSE} is the sense resistor (Unit: Ω)):

$$Current = \frac{200 \times CUR}{26837 \times R_{SENSE}}$$

12.1.4 VADC Measurement Timing

The VADC measurement frequency is 10Hz. The VADC measures cell voltage and temperature and current at a fixed timing.

(1) The VADC measurement 16 channels of voltage and 1 channel of current at a fixed timing during each t_{cycle}

(2) The VADC measurement 3 channels of temperature at a fixed timing during one second period

After each t_{cycle} is completed, the VADC_FLG bit is set to 1 and the ALARM pin will output a low pulse. The VADC_FLG flag is automatically cleared when the BFLAG2 register is read. The number of cell and temperature do not change VADC measurement timing.

Table 12.21 System Flag Register2

71H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BFLAG2	RST_FLG	WAKE_FLG	CADC_FLG	VADC_FLG	OTD_FLG	UTD_FLG	OTC_FLG	UTC_FLG
R/W	R/W“0”	R/W“0”	R	R	R/W“0”	R/W“0”	R/W“0”	R/W”0”
Default	1	0	0	0	0	0	0	0

Bit Number	Symbol	Description
4	**VADC_FLG**	VADC measurement completed flag 1: VADC measurement completed 0: VADC measurement not completed After the register is read, this bit will be automatically cleared

If the balance occurs, the VADC sample timing is adjusted: the VADC sample cycle and balance will be performed at intervals, as shown in the following figure.

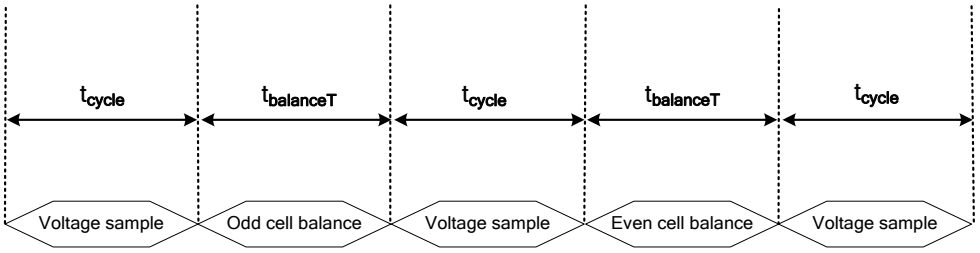


Fig 14. Odd and Even Balanced Timing

If the balance is turned on, the corresponding protection detection and status of the SH367309 will change:

(1) When detecting the following status, the protection delay may produce the maximum $t_{balanceT}$ deviation: overvoltage, overvoltage recovery, undervoltage, undervoltage recovery, secondary overvoltage, powerdown state, precharge, low voltage prohibition charge.

(2) Temperature measurements and protection are not affected

(3) Current measurement and protection are not affected

12.2 CADC for Current Measurement

12.2.1 Feature

- ◆ 16 bit Σ-Δ analog-to-digital measurement
- ◆ 4Hz measurement frequency
- ◆ 1 channel differential input

12.2.2 Measurement Range and Result

CADC only has 1 channel: current sample channel.

Current channel measurement range:-0.20~0.20V.

CADC measurement result is stored in the CADCD register.

Table 12.22 CADC Current Measurement Register

6EH,6FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CADCDH	CDATA.15	CDATA.14	CDATA.13	CDATA.12	CDATA.11	CDATA.10	CDATA.9	CDATA.8
CADCDL	CDATA.7	CDATA.6	CDATA.5	CDATA.4	CDATA.3	CDATA.2	CDATA.1	CDATA.0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:0 **7:0**	CDATA.15- CDATA.0	CDATA.15 is a sign bit, "1" indicates discharging; "0" indicates charging. When the measurement is completed, the data is updated to the value corresponding to the voltage across the sense resistor

12.2.3 Current Calculation Formula

According to the CADC measurement result can calculate the current value (unit: mA, CADCD is CADCD register value, R_{SENSE} is sense resistance, unit: Ω):

$$Current = \frac{200 \times CADCD}{21470 \times R_{SENSE}}$$

12.2.4 CADC Work Configuration

The CADCON bit in the CONF register can be used to enable the CADC module. After each measurement is completed, the CADC_FLG bit in BFLAG2 register is set to 1, and the ALARM pin outputs a low pulse. The CADC _FLG flag is automatically cleared when the BFLAG2 register is read.

Table 12.23 System Configuration Register

40H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONF	OCRC	PCHMOS	DSGMOS	CHGMOS	CADCON	ENWDT	SLEEP	IDLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default (POR/WDT/LVR/PIN)	0	1	1	1	0	0	0	0

Bit Number	Symbol	Description
3	**CADCON**	CADC enable control 0: Disable 1: Enable

Table 12.24 System Flag Register2

71H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BFLAG2	RST_FLG	WAKE_FLG	CADC_FLG	VADC_FLG	OTD_FLG	UTD_FLG	OTC_FLG	UTC_FLG
R/W	R/W“0”	R/W“0”	R	R	R/W“0”	R/W“0”	R/W“0”	R/W”0”
Default	1	0	0	0	0	0	0	0

Bit Number	Symbol	Description
5	**CADC_FLG**	CADC measurement completed flag 1: CADC measurement completed 0: CADC measurement not completed After the register is read, this bit will be automatically cleared

12.3 TWI Communication

12.3.1 Feature

- Two-line mode
- Slave is supported only, and the address is fixed at 0x1A
- Support Transmitter and Receiver
- Support low bus timeout
- Support CRC8
- Support communication wake-up system in IDLE and SLEEP status

12.3.2 Work Mode

SH367309 turns on the TWI module in AFE mode.TWI serial bus uses two wires (SDA and SCL) to transfer information between the bus and the device. SH367309 complies with the TWI bus specification, automatically processes bytes for transmission, and tracks serial communications.

12.3.3 Data Transmission Format

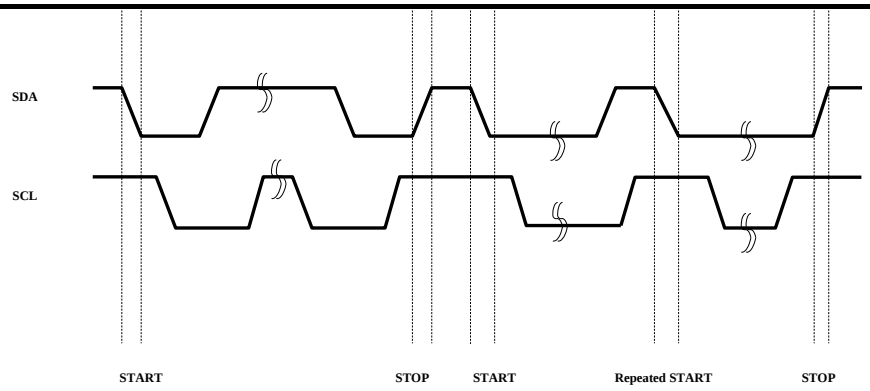
Transmission of each bit on the data line in data transmission requires one pulse on the clock line. The data line should remain stable when the clock is high. However, there is no need to follow this rule when sending start conditions and stop conditions.

TWI defines two special waveforms: start conditions and stop conditions. The falling edge of the data line is defined as the starting condition when the clock line is high; the rising edge of the data line is defined as the stopping condition when the clock line is high. Start and stop conditions are sent by the host.

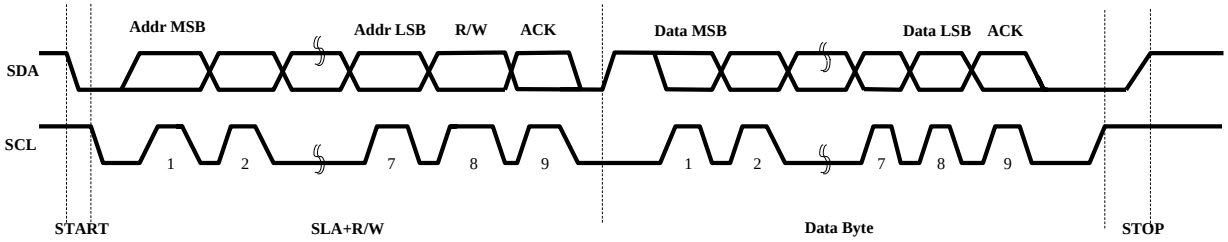
The host can start and end a transmission. A transmission starts when the host sends a start condition, and ends when it sends a stop condition. The bus is defined as "busy" between the start condition and the stop condition. Other hosts should not attempt to send transmissions. In the "Busy" state, if the host sends the start condition again, it is defined as "repeat start condition", indicating that the host wants to start a new transfer without giving up the bus. After the repeated start condition is transmitted, the bus is still in a "busy" state until the bus stops. In view of the fact that the repeated start conditions and the start conditions are completely consistent, unless otherwise stated, the start conditions will be used in place of both.

All data packets (including address packets) consist of 9 bits, including 1 byte and an acknowledgement bit. The host is responsible for issuing the clock and the start and stop conditions. The receiver is responsible for giving the reply signal. The receiver sends an "ACK" signal by pulling the data line low at the ninth clock pulse; or maintaining the high signal at the ninth pulse indicates a "NACK" signal. When the receiver receives the last byte, or for some reason cannot continue to receive data, it should respond to "NACK" signal. TWI uses high-to-low bit-by-bit transmission.

A transfer usually includes a start condition, address + R/W, one or more packets, and a stop condition. Only data formats containing start conditions and stop conditions are not compliant with the communication rules. It is worth noting that the "line and" structure provides convenience for handshake signals between the master and the slave. When the host is relatively fast or the slave needs to handle other transactions, the slave can pull down the clock line to lengthen the low time of the clock line, thereby reducing the communication frequency. Slave can stretch clock line low period but does not affect clock line high period.



When generating a response signal, the SH367309 pulls down the SDA signal line. When the SH367309 receives data, release the SCL signal line.



12.3.4 Transmission Mode

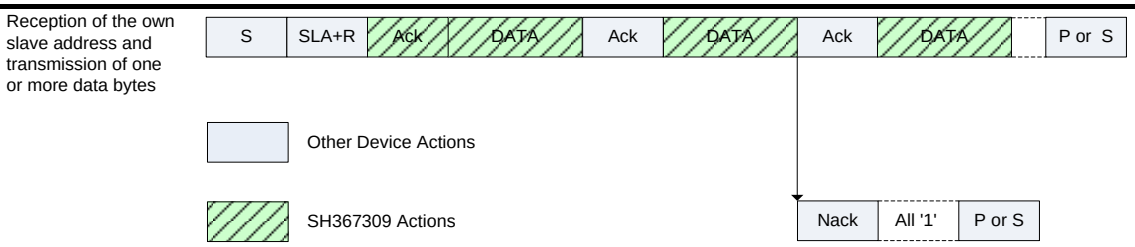
(1) Overview

The following describes the two modes of TWI as slave communication: slave transmission mode and slave reception mode. In the initial state, the SH367309 waits for the bus to respond to its own address. If the direction flag bit is "R", then TWI enters the slave transmission mode, otherwise it will enter the slave reception mode. Below are the following abbreviations:

S : Start condition
Rs : Repeat start condition
R : Read control bit
W : Write control bit
A : Response bit
Ā : No response bit
DATA : 8-bit data
P : Stop condition
SLA : Slave address

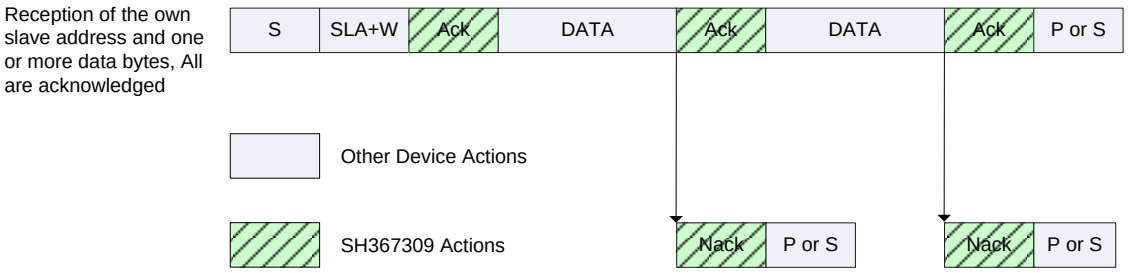
(2) Slave transmission mode

In the slave transmission mode, the slave sends a series of data to the host. After sending a byte, if the host responds with “response” message, the SH367309 is ready to send the next byte; if the host responds “no response”, it will not continue sending data (if the host is still reading data, it returns “1" data), waiting for the host to send a "stop condition" or "repeat start condition".



(3) Slave reception mode

In the slave reception mode, SH367309 receives a series of data from the host.



12.3.5 Communication protocol

12.3.5.1 Overview

The TWI communication protocol consists of two parts: read and write EEPROM and RAM registers.

TWI communication writes EEPROM registers when VPRO pin voltage is V_{PRO}.

In TWI communication, SH367309 acts as a slave and its fixed address is:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	1	1	0	1	0	R/W

12.3.5.2 EEPROM Register Read and Write Protocol

(1) Write Protocol

The EEPROM register can be written when the VPRO pin is connected to the voltage V_{PRO}. The EEPROM register 00H~18H can be written, and the length of data written is fixed to one byte.

It takes 35mS delay after writing a register to start writing a register.

Fig 15. TWI EEPROM Write Timing

(2) Read Protocol

The EEPROM register with address 00H~19H can be read. The data length to be read needs to be sent to SH367309 in units of Byte (this length does not include the read CRC byte). Returns "All 1" data if the register address read exceeds the definition.

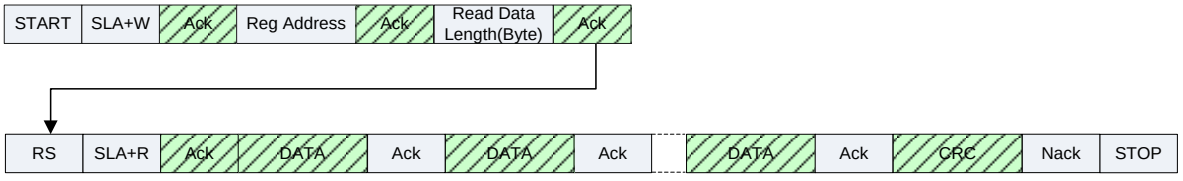


Fig 16. TWI EEPROM Read Timing

12.3.5.3 RAM Register Read and Write Protocol

(1) Write Protocol

The RAM registers with address 40H~42H, 70H~72H can be written, and the length of data written is fixed to one byte.

Fig 17. TWI RAM Write Timing

(2) Read Protocol

The RAM registers with address 40H to 72H can be read. The data length to be read needs to be sent to SH367309 in units of Byte (this length does not include the read CRC byte). Returns "All 1" data if the register address read exceeds the definition.

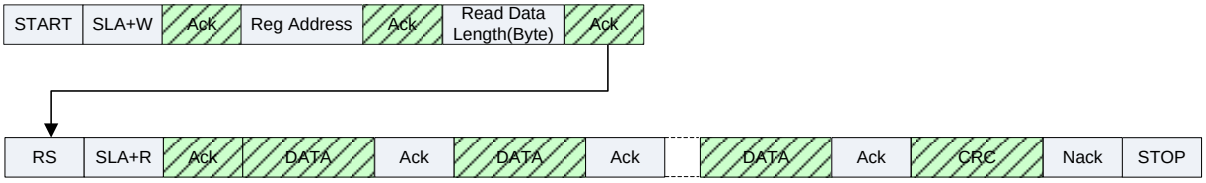


Fig 18. TWI RAM Read Timing

12.3.5.4 Software Reset Protocol

SH367309 will execute a software reset after receiving the following instruction protocol (the rewritten EEPROM register is valid after a software reset operation).

Fig 19. Software Reset Timing

12.3.5.5 CRC8 check

TWI write operation is fixed to write 1Byte, CRC8 will check from the data after the start bit, including the slave address (including R/W bit), register address, write data, the CRC8 generation formula = $X^8 + X^2 + X + 1$, if CRC check is correct, SH367309 will update the data to the specified register, and return ACK to the host, otherwise, it will not be updated, and returns NACK to the host.

The data length of the TWI read operation can be set by the host. The CRC8 will check the data after the start bit, including the slave address (including the R/W bit), the register address, the read data length N, and after the repetition start, the slave address (including R/W bit) and N bytes of data, the CRC8 generation formula = $X^8 + X^2 + X + 1$, SH367309 will send calculated CRC8 to the host.

Software reset instructions follow a fixed format. SH367309 will determine the subsequent data length and CRC8 based on the received 1st Byte "0xEA".

Note: The initial value of CRC8 is fixed at 0x00.

13. EEPROM and RAM Register Configuration

13.1 EEPROM and RAM Overview

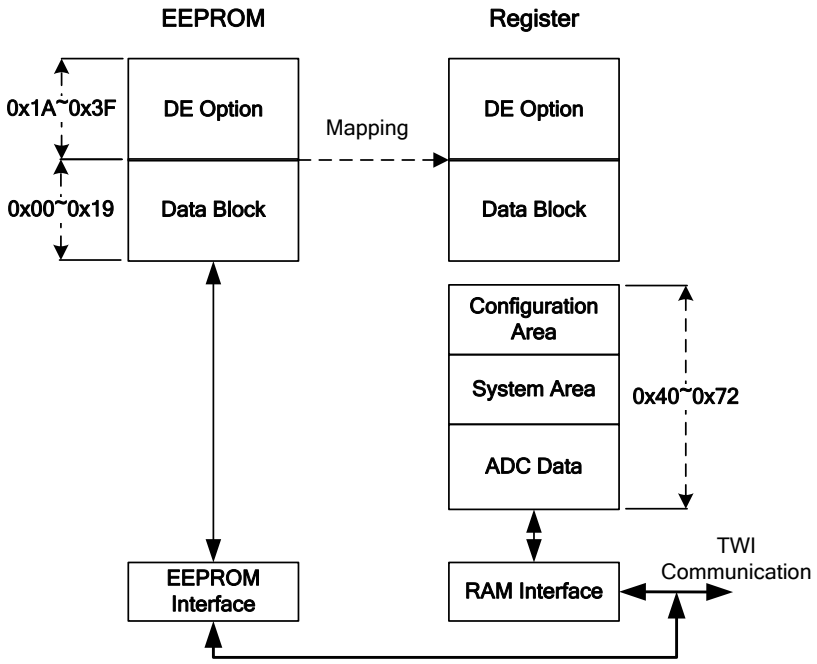


Fig 20. Register Configuration

13.2 EEPROM Register List and Details

Table8. EEPROM Register List

No.(Hex)	Name	Status bits							
		7	6	5	4	3	2	1	0
00H	**SCONF1**	ENPCH	ENMOS	OCPM	BAL	CN3	CN2	CN1	CN0
01H	**SCONF2**	E0VB	-	UV_OP	DIS_PF	CTLC1	CTLC0	OCRA	EUVR
02H	**OVT/LDRT /OVH**	OVT3	OVT2	OVT1	OVT0	LDRT1	LDRT0	OV.9	OV.8
03H	**OVL**	OV.7	OV.6	OV.5	OV.4	OV.3	OV.2	OV.1	OV.0
04H	**UVT/OVRH**	UVT3	UVT2	UVT1	UVT0	-	-	OVR.9	OVR.8
05H	**OVRL**	OVR.7	OVR.6	OVR.5	OVR.4	OVR.3	OVR.2	OVR.1	OVR.0
06H	**UV**	UV.7	UV.6	UV.5	UV.4	OV.3	UV.2	UV.1	UV.0
07H	**UVR**	UVR.7	UVR.6	UVR.5	UVR.4	UVR.3	UVR.2	UVR.1	UVR.0
08H	**BALV**	BALV.7	BALV.6	BALV.5	BALV.4	BALV.3	BALV.2	BALV.1	BALV.0
09H	**PREV**	PREV.7	PREV.6	PREV.5	PREV.4	PREV.3	PREV.2	PREV.1	PREV.0
0AH	**L0V**	-	L0V.6	L0V.5	L0V.4	L0V.3	L0V.2	L0V.1	L0V.0
0BH	**PFV**	PFV.7	PFV.6	PFV.5	PFV.4	PFV.3	PFV.2	PFV.1	PFV.0
0CH	**OCD1V/OCD1T**	OCD1V3	OCD1V2	OCD1V1	OCD1V0	OCD1T3	OCD1T2	OCD1T1	OCD1T0
0DH	**OCD2V/OCD2T**	OCD2V3	OCD2V2	OCD2V1	OCD2V0	OCD2T3	OCD2T2	OCD2T1	OCD2T0
0EH	**SCV/SCT**	SCV3	SCV2	SCV1	SCV0	SCT3	SCT2	SCT1	SCT0
0FH	**OCCV/OCCT**	OCCV3	OCCV2	OCCV1	OCCV0	OCCT3	OCCT2	OCCT1	OCCT0
10H	**MOST/OCRT/PFT**	CHS1	CHS0	MOST1	MOST0	OCRT1	OCRT0	PFT1	PFT0
11H	**OTC**	OTC7	OTC6	OTC5	OTC4	OTC3	OTC2	OTC1	OTC0
12H	**OTCR**	OTCR7	OTCR6	OTCR5	OTCR4	OTCR3	OTCR2	OTCR1	OTCR0
13H	**UTC**	UTC7	UTC6	UTC5	UTC4	UTC3	UTC2	UTC1	UTC0
14H	**UTCR**	UTCR7	UTCR6	UTCR5	UTCR4	UTCR3	UTCR2	UTCR1	UTCR0
15H	**OTD**	OTD7	OTD6	OTD5	OTD4	OTD3	OTD2	OTD1	OTD0
16H	**OTDR**	OTDR7	OTDR6	OTDR5	OTDR4	OTDR3	OTDR2	OTDR1	OTDR0
17H	**UTD**	UTD7	UTD6	UTD5	UTD4	UTD3	UTD2	UTD1	UTD0
18H	**UTDR**	UTDR7	UTDR6	UTDR5	UTDR4	UTDR3	UTDR2	UTDR1	UTDR0
19H	**TR**	-	TR6	TR5	TR4	TR3	TR2	TR1	TR0
1AH~1FH	**Reserved**	-	-	-	-	-	-	-	-

Table 13.1 System Configuration Register1

00H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF1	ENPCH	ENMOS	OCPM	BAL	CN3	CN2	CN1	CN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7	**ENPCH**	Precharge enable control 0: Disable 1: Enable
6	**ENMOS**	Charge MOSFET recovery control 0: Disable 1: Enable When the charge overtemperature and undertemperature protection turns off the charge MOSFET, if the discharge overcurrent1 or discharging status is detected, the charge MOSFET is turned on
5	**OCPM**	Overcurrent MOSFET control 0: charge Overcurrent only turns off charge MOSFET discharge Overcurrent/short circuit only turns off discharge MOSFET 1: Overcurrent protection turns off charge and discharge MOSFET
4	**BAL**	Balance control 0: Balance switch is controlled by SH367309 internal logic 1:Balance switch is controlled by MCU, balance timing is controlled by SH367309 internal logic
3:0	**CN3~CN0**	The Number of cells in series configuration CN[3:0] = 0101: 5 Cell CN[3:0] = 0110: 6 Cell CN[3:0] = 0111: 7 Cell CN[3:0] = 1000: 8 Cell CN[3:0] = 1001: 9 Cell CN[3:0] = 1010: 10 Cell CN[3:0] = 1011: 11 Cell CN[3:0] = 1100: 12 Cell CN[3:0] = 1101: 13 Cell CN[3:0] = 1110: 14 Cell CN[3:0] = 1111: 15 Cell CN[3:0] = other: 16 Cell Note: SH367309 is compatible with 5 to 16 series lithium-ion pack. When the number of series is less than 16, the unused input terminal (nearest VBAT) can be shorted to the positive terminal of the highest cell

Table 13.2 System Configuration Register2

01H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONF2	E0VB	-	UV_OP	DIS_PF	CTLC1	CTLC0	OCRA	EUVR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7	**E0VB**	Low voltage prohibition charge control 0: Allow low voltage charge 1: Prohibit low voltage charge
6	**-**	Reserved
5	**UV_OP**	Charge MOSFET control after undervoltage 0: Undervoltage only turn off discharge MOSFET 1: Undervoltage Turn off charge and discharge MOSFET
4	**DIS_PF**	Secondary Overvoltage control bit 0:Enable secondary overvoltage protection 1:Disable secondary overvoltage protection
3:2	**CTLC1~0**	CTL pin configuration control CTLC[1:0] = 00: Do not control any MOSFET, CTL pin input is invalid CTLC[1:0] = 01: Control the charge and precharge MOSFET CTLC[1:0] = 10: Control the discharge MOSFET CTLC[1:0] = 11: Control charge and discharge and pre-charge MOSFET
1	**OCRA**	overcurrent protection self-recovery control 0: Disable 1: Enable
0	**EUVR**	Undervoltage recovery control 0: Undervoltage recovery no need to disconnect the load 1: Undervoltage recovery need to disconnect the load

Table 13.3 Overvoltage Threshold and Delay Register / Load Release Delay Register

02H,03H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OVH	OVT3	OVT2	OVT1	OVT0	LDRT1	LDRT0	OV.9	OV.8
OVL	OV.7	OV.6	OV.5	OV.4	OV.3	OV.2	OV.1	OV.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**OVT3~OVT0**	Overvoltage detection delay configuration OVT[3:0] = 0000: OV delay = 100mS OVT[3:0] = 0001: OV delay = 200mS OVT[3:0] = 0010: OV delay = 300mS OVT[3:0] = 0011: OV delay = 400mS OVT[3:0] = 0100: OV delay = 600mS OVT[3:0] = 0101: OV delay = 800mS OVT[3:0] = 0110: OV delay = 1S OVT[3:0] = 0111: OV delay = 2S OVT[3:0] = 1000: OV delay = 3S OVT[3:0] = 1001: OV delay = 4S OVT[3:0] = 1010: OV delay = 6S OVT[3:0] = 1011: OV delay = 8S OVT[3:0] = 1100: OV delay = 10S OVT[3:0] = 1101: OV delay = 20S OVT[3:0] = 1110: OV delay = 30S OVT[3:0] = 1111: OV delay = 40S
3:2	**LDRT1~LDRT0**	Load release detection delay configuration LDRT[1:0] = 00: delay = 100mS LDRT[1:0] = 01: delay = 500mS LDRT[1:0] = 10: delay = 1000mS LDRT[1:0] = 11: delay = 2000mS
1:0 **7:0**	**OV.9~OV.0**	Overvoltage threshold, calculation formula: V_{OV} = register value * 5mV

Table 13.4 Overvoltage Recovery Threshold / Undervoltage Delay Register

04H,05H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OVRH	UVT3	UVT2	UVT1	UVT0	-	-	OVR.9	OVR.8
OVRL	OVR.7	OVR.6	OVR.5	OVR.4	OVR.3	OVR.2	OVR.1	OVR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**UVT3~UVT0**	Undervoltage detection delay configuration UVT[3:0] = 0000: UV delay = 100mS UVT[3:0] = 0001: UV delay = 200mS UVT[3:0] = 0010: UV delay = 300mS UVT[3:0] = 0011: UV delay = 400mS UVT[3:0] = 0100: UV delay = 600mS UVT[3:0] = 0101: UV delay = 800mS UVT[3:0] = 0110: UV delay = 1S UVT[3:0] = 0111: UV delay = 2S UVT[3:0] = 1000: UV delay = 3S UVT[3:0] = 1001: UV delay = 4S UVT[3:0] = 1010: UV delay = 6S UVT[3:0] = 1011: UV delay = 8S UVT[3:0] = 1100: UV delay = 10S UVT[3:0] = 1101: UV delay = 20S UVT[3:0] = 1110: UV delay = 30S UVT[3:0] = 1111: UV delay = 40S
3:2	**-**	Reserved
1:0 **7:0**	**OVR.9~OVR.0**	Overvoltage recovery threshold, calculation formula: V_{OVR} = register value * 5mV

Table 13.5 Undervoltage Threshold Register

06H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UV	UV.7	UV.6	UV.5	UV.4	UV.3	UV.2	UV.1	UV.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	UV.7~ UV.0	Undervoltage threshold, calculation formula: V_{UV} = register value * 20mV

Table 13.6 Undervoltage Recovery Threshold Register

07H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UVR	UVR.7	UVR.6	UVR.5	UVR.4	UVR.3	UVR.2	UVR.1	UVR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	UVR.7~UVR.0	Undervoltage recovery threshold, calculation formula: V_{UVR} = register value * 20mV

Table 13.7 Balance Threshold Register

08H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BALV	BALV.7	BALV.6	BALV.5	BALV.4	BALV.3	BALV.2	BALV.1	BALV.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	BALV.7~ BALV.0	Balance threshold, calculation formula: V_{BALV} = register value * 20mV

Table 13.8 Precharge Threshold Register

09H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PREV	PREV.7	PREV.6	PREV.5	PREV.4	PREV.3	PREV.2	PREV.1	PREV.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	PREV.7~ PREV.0	Precharge threshold, calculation formula: V_{PREV} = register value * 20mV

Table 13.9 Low Voltage Prohibition Charge Threshold Register

0AH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
L0V	-	L0V.6	L0V.5	L0V.4	L0V.3	L0V.2	L0V.1	L0V.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	L0V.6~ L0V.0	Low voltage prohibition charge threshold, calculation formula: V_{L0V} = register value * 20mV

Table 13.10 Secondary Overvoltage Threshold Register

0BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PFV	PFV.7	PFV.6	PFV.5	PFV.4	PFV.3	PFV.2	PFV.1	PFV.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	PFV.7~ PFV.0	Secondary overvoltage threshold, calculation formula: V_{PFV} = register value * 20mV

Table 13.11 Voltage Threshold Relationship

High → Low							
PFV	**OV**	**OVR**	**UVR**	**UV**	**V_{PD}**	**PREV**	**L0V**
Secondary overvoltage threshold	Overvoltage threshold	Overvoltage recovery threshold	Undervoltage recovery threshold	Undervoltage threshold	Powerdown threshold	Precharge threshold	Low voltage prohibition charge threshold

Table 13.12 Discharge Overcurrent Level-1 Configuration Register

0CH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCD1V/OCD1T	OCD1V3	OCD1V2	OCD1V1	OCD1V0	OCD1T3	OCD1T.2	OCD1T.1	OCD1T.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**OCD1V3~ OCD1V0**	Discharge overcurrent level-1 threshold configuration OCD1V[3:0] = 0000: OCD1 threshold = 20mV OCD1V[3:0] = 0001: OCD1 threshold = 30mV OCD1V[3:0] = 0010: OCD1 threshold = 40mV OCD1V[3:0] = 0011: OCD1 threshold = 50mV OCD1V[3:0] = 0100: OCD1 threshold = 60mV OCD1V[3:0] = 0101: OCD1 threshold = 70mV OCD1V[3:0] = 0110: OCD1 threshold = 80mV OCD1V[3:0] = 0111: OCD1 threshold = 90mV OCD1V[3:0] = 1000: OCD1 threshold = 100mV OCD1V[3:0] = 1001: OCD1 threshold = 110mV OCD1V[3:0] = 1010: OCD1 threshold = 120mV OCD1V[3:0] = 1011: OCD1 threshold = 130mV OCD1V[3:0] = 1100: OCD1 threshold = 140mV OCD1V[3:0] = 1101: OCD1 threshold = 160mV OCD1V[3:0] = 1110: OCD1 threshold = 180mV OCD1V[3:0] = 1111: OCD1 threshold = 200mV
3:0	**OCD1T3~ OCD1T0**	Discharge overcurrent level-1 detection delay configuration OCD1T[3:0] = 0000: OCD1 delay = 50mS OCD1T[3:0] = 0001: OCD1 delay = 100mS OCD1T[3:0] = 0010: OCD1 delay = 200mS OCD1T[3:0] = 0011: OCD1 delay = 400mS OCD1T[3:0] = 0100: OCD1 delay = 600mS OCD1T[3:0] = 0101: OCD1 delay = 800mS OCD1T[3:0] = 0110: OCD1 delay = 1S OCD1T[3:0] = 0111: OCD1 delay = 2S OCD1T[3:0] = 1000: OCD1 delay = 4S OCD1T[3:0] = 1001: OCD1 delay = 6S OCD1T[3:0] = 1010: OCD1 delay = 8S OCD1T[3:0] = 1011: OCD1 delay = 10S OCD1T[3:0] = 1100: OCD1 delay = 15S OCD1T[3:0] = 1101: OCD1 delay = 20S OCD1T[3:0] = 1110: OCD1 delay = 30S OCD1T[3:0] = 1111: OCD1 delay = 40S

Note: Discharge overcurrent level-1 threshold is voltage of VRS2-VRS1.

Table 13.13 Discharge Overcurrent Level-2 Configuration Register

0DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCD2V/OCD2T	OCD2V3	OCD2V2	OCD2V1	OCD2V0	OCD2T3	OCD2T2	OCD2T1	OCD2T0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**OCD2V3~ OCD2V0**	Discharge overcurrent level-2 threshold configuration OCD2V[3:0] = 0000: OCD2 threshold = 30mV OCD2V[3:0] = 0001: OCD2 threshold = 40mV OCD2V[3:0] = 0010: OCD2 threshold = 50mV OCD2V[3:0] = 0011: OCD2 threshold = 60mV OCD2V[3:0] = 0100: OCD2 threshold = 70mV OCD2V[3:0] = 0101: OCD2 threshold = 80mV OCD2V[3:0] = 0110: OCD2 threshold = 90mV OCD2V[3:0] = 0111: OCD2 threshold = 100mV OCD2V[3:0] = 1000: OCD2 threshold = 120mV OCD2V[3:0] = 1001: OCD2 threshold = 140mV OCD2V[3:0] = 1010: OCD2 threshold = 160mV OCD2V[3:0] = 1011: OCD2 threshold = 180mV OCD2V[3:0] = 1100: OCD2 threshold = 200mV OCD2V[3:0] = 1101: OCD2 threshold = 300mV OCD2V[3:0] = 1110: OCD2 threshold = 400mV OCD2V[3:0] = 1111: OCD2 threshold = 500mV
3:0	**OCD2T3~ OCD2T0**	Discharge overcurrent level-2 detection delay configuration OCD2T[3:0] = 0000: OCD2 delay = 10mS OCD2T[3:0] = 0001: OCD2 delay = 20mS OCD2T[3:0] = 0010: OCD2 delay = 40mS OCD2T[3:0] = 0011: OCD2 delay = 60mS OCD2T[3:0] = 0100: OCD2 delay = 80mS OCD2T[3:0] = 0101: OCD2 delay = 100mS OCD2T[3:0] = 0110: OCD2 delay = 200mS OCD2T[3:0] = 0111: OCD2 delay = 400mS OCD2T[3:0] = 1000: OCD2 delay = 600mS OCD2T[3:0] = 1001: OCD2 delay = 800mS OCD2T[3:0] = 1010: OCD2 delay = 1S OCD2T[3:0] = 1011: OCD2 delay = 2S OCD2T[3:0] = 1100: OCD2 delay = 4S OCD2T[3:0] = 1101: OCD2 delay = 8S OCD2T[3:0] = 1110: OCD2 delay = 10S OCD2T[3:0] = 1111: OCD2 delay = 20S

Note: Discharge overcurrent level-2 threshold is voltage of VRS2-VRS1.

Table 13.14 Discharge Short circuit Register

0EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCV/SCT	SCV3	SCV2	SCV1	SCV0	SCT3	SCT2	SCT1	SCT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**SCV3~ SCV0**	Discharge short circuit threshold configuration SCV[3:0] = 0000: SC threshold = 50mV SCV[3:0] = 0001: SC threshold = 80mV SCV[3:0] = 0010: SC threshold = 110mV SCV[3:0] = 0011: SC threshold = 140mV SCV[3:0] = 0100: SC threshold = 170mV SCV[3:0] = 0101: SC threshold = 200mV SCV[3:0] = 0110: SC threshold = 230mV SCV[3:0] = 0111: SC threshold = 260mV SCV[3:0] = 1000: SC threshold = 290mV SCV[3:0] = 1001: SC threshold = 320mV SCV[3:0] = 1010: SC threshold = 350mV SCV[3:0] = 1011: SC threshold = 400mV SCV[3:0] = 1100: SC threshold = 500mV SCV[3:0] = 1101: SC threshold = 600mV SCV[3:0] = 1110: SC threshold = 800mV SCV[3:0] = 1111: SC threshold = 1000mV
3:0	**SCT3~ SCT0**	Discharge short circuit detection delay configuration SCT[3:0] = 0000: SC delay = 0uS SCT[3:0] = 0001: SC delay = 64uS SCT[3:0] = 0010: SC delay = 128uS SCT[3:0] = 0011: SC delay = 192uS SCT[3:0] = 0100: SC delay = 256uS SCT[3:0] = 0101: SC delay = 320uS SCT[3:0] = 0110: SC delay = 384uS SCT[3:0] = 0111: SC delay = 448uS SCT[3:0] = 1000: SC delay = 512uS SCT[3:0] = 1001: SC delay = 576uS SCT[3:0] = 1010: SC delay = 640uS SCT[3:0] = 1011: SC delay = 704uS SCT[3:0] = 1100: SC delay = 768uS SCT[3:0] = 1101: SC delay = 832uS SCT[3:0] = 1110: SC delay = 896uS SCT[3:0] = 1111: SC delay = 960uS

Note: The short circuit protection threshold is voltage of VRS2-VRS1.

Note: The short circuit protection delay refers only to the delay of the internal circuit detection. If there is an RC filter at both ends of the sense resistor, it will introduce a certain delay (＜50uS).

Table 13.15 Charge Overcurrent Register

0FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCCV/OCCT	OCCV3	OCCV2	OCCV1	OCCV0	OCCT3	OCCT2	OCCT1	OCCT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:4	**OCCV3~ OCCV0**	Charge overcurrent threshold configuration OCCV[3:0] = 0000: OCC threshold = 20mV OCCV[3:0] = 0001: OCC threshold = 30mV OCCV[3:0] = 0010: OCC threshold = 40mV OCCV[3:0] = 0011: OCC threshold = 50mV OCCV[3:0] = 0100: OCC threshold = 60mV OCCV[3:0] = 0101: OCC threshold = 70mV OCCV[3:0] = 0110: OCC threshold = 80mV OCCV[3:0] = 0111: OCC threshold = 90mV OCCV[3:0] = 1000: OCC threshold = 100mV OCCV[3:0] = 1001: OCC threshold = 110mV OCCV[3:0] = 1010: OCC threshold = 120mV OCCV[3:0] = 1011: OCC threshold = 130mV OCCV[3:0] = 1100: OCC threshold = 140mV OCCV[3:0] = 1101: OCC threshold = 160mV OCCV[3:0] = 1110: OCC threshold = 180mV OCCV[3:0] = 1111: OCC threshold = 200mV
3:0	**OCCT3~ OCCT0**	Charge overcurrent detection delay configuration OCCT[3:0] = 0000: OCC delay = 10mS OCCT[3:0] = 0001: OCC delay = 20mS OCCT[3:0] = 0010: OCC delay = 40mS OCCT[3:0] = 0011: OCC delay = 60mS OCCT[3:0] = 0100: OCC delay = 80mS OCCT[3:0] = 0101: OCC delay = 100mS OCCT[3:0] = 0110: OCC delay = 200mS OCCT[3:0] = 0111: OCC delay = 400mS OCCT[3:0] = 1000: OCC delay = 600mS OCCT[3:0] = 1001: OCC delay = 800mS OCCT[3:0] = 1010: OCC delay = 1S OCCT[3:0] = 1011: OCC delay = 2S OCCT[3:0] = 1100: OCC delay = 4S OCCT[3:0] = 1101: OCC delay = 8S OCCT[3:0] = 1110: OCC delay = 10S OCCT[3:0] = 1111: OCC delay = 20S

Note: The charge overcurrent protection threshold is voltage of VRS1-VRS2.

Table 13.16 State Detection / MOSFET Delay / Overcurrent Self-recovery / Secondary Overvoltage Delay Register

10H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MOST/OCRT/PFT	CHS1	CHS0	MOST1	MOST0	OCRT1	OCRT0	PFT1	PFT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:6	**CHS1~ CHS0**	Charge and discharge state detection threshold configuration CHS [1:0] = 00: threshold = 200uV CHS [1:0] = 01: threshold = 500uV CHS [1:0] = 10: threshold = 1000uV CHS [1:0] = 11: threshold = 2000uV
5:4	**MOST1~MOST0**	Charge MOSFET turn on delay configuration MOST[1:0] = 00: delay = 64uS MOST[1:0] = 01: delay = 128uS MOST[1:0] = 10: delay = 256uS MOST[1:0] = 11: delay = 512uS
3:2	**OCRT1~OCRT0**	Overcurrent self-recovery delay configuration OCRT[1:0] = 00: delay = 8S OCRT[1:0] = 01: delay = 16S OCRT[1:0] = 10: delay = 32S OCRT[1:0] = 11: delay = 64S
1:0	**PFT1~PFT0**	Second overvoltage detection delay configuration PFT[1:0] = 00: PF delay = 8S PFT[1:0] = 01: PF delay = 16S PFT[1:0] = 10: PF delay = 32S PFT[1:0] = 11: PF delay = 64S

Table 13.17 Charge Overtemperature Threshold Register

11H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTC	OTC7	OTC6	OTC5	OTC4	OTC3	OTC2	OTC1	OTC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**OTC7~OTC0**	Charge overtemperature threshold

Table 13.18 Charge Overtemperature Recovery Threshold Register

12H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTCR	OTCR7	OTCR6	OTCR5	OTCR4	OTCR3	OTCR2	OTCR1	OTCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**OTCR7~OTCR0**	Charge overtemperature recovery threshold

Table 13.19 Charge Undertemperature Threshold Register

13H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UTC	UTC7	UTC6	UTC5	UTC4	UTC3	UTC2	UTC1	UTC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**UTC7~UTC0**	Charge undertemperature threshold

Table 13.20 Charge Undertemperature Recovery Threshold Register

14H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UTCR	UTCR7	UTCR6	UTCR5	UTCR4	UTCR3	UTCR2	UTCR1	UTCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**UTCR7~UTCR0**	Charge undertemperature recovery threshold

Table 13.21 Discharge Overtemperature Threshold Register

15H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTD	OTD7	OTD6	OTD5	OTD4	OTD3	OTD2	OTD1	OTD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**OTD7~OTD0**	Discharge overtemperature threshold

Table 13.22 Discharge Overtemperature Recovery Threshold Register

16H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTDR	OTDR7	OTDR6	OTDR5	OTDR4	OTDR3	OTDR2	OTDR1	OTDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**OTDR7~OTDR0**	Discharge Overtemperature protection release threshold

Table 13.23 Discharge Undertemperature Threshold Register

17H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UTD	UTD7	UTD6	UTD5	UTD4	UTD3	UTD2	UTD1	UTD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**UTD7~UTD0**	Discharge undertemperature threshold

Table 13.24 Discharge Undertemperature Recovery Threshold Register

18H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UTDR	UTDR7	UTDR6	UTDR5	UTDR4	UTDR3	UTDR2	UTDR1	UTDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Symbol	Description
7:0	**UTDR7~UTDR0**	Discharge Undertemperature protection release threshold

Table 13.25 Temperature Internal Reference Resistance Coefficient Register

19H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TR	-	TR6	TR5	TR4	TR3	TR2	TR1	TR0
R	-	R	R	R	R	R	R	R

Bit Number	Symbol	Description
7	**-**	**Reserved**
6:0	**TR6~ TR0**	Temperature internal reference resistance coefficient

13.3 EEROM&RAM Register List and Details

Table9. EEPROM Register List

No.(Hex)	Name	Status bits							
		7	6	5	4	3	2	1	0
00H	**SCONF1**	ENPCH	ENMOS	OCPM	BAL	CN3	CN2	CN1	CN0
01H	**SCONF2**	E0VB	-	UV_OP	DIS_PF	CTLC1	CTLC0	OCRA	EUVR
02H	**OVT/LDRT/OVH**	OVT3	OVT2	OVT1	OVT0	LDRT1	LDRT0	OV.9	OV.8
03H	**OVL**	OV.7	OV.6	OV.5	OV.4	OV.3	OV.2	OV.1	OV.0
04H	**UVT/OVRH**	UVT3	UVT2	UVT1	UVT0	-	-	OVR.9	OVR.8
05H	**OVRL**	OVR.7	OVR.6	OVR.5	OVR.4	OVR.3	OVR.2	OVR.1	OVR.0
06H	**UV**	UV.7	UV.6	UV.5	UV.4	UV.3	UV.2	UV.1	UV.0
07H	**UVR**	UVR.7	UVR.6	UVR.5	UVR.4	UVR.3	UVR.2	UVR.1	UVR.0
08H	**BALV**	BALV.7	BALV.6	BALV.5	BALV.4	BALV.3	BALV.2	BALV.1	BALV.0
09H	**PREV**	PREV.7	PREV.6	PREV.5	PREV.4	PREV.3	PREV.2	PREV.1	PREV.0
0AH	**L0V**	-	L0V.6	L0V.5	L0V.4	L0V.3	L0V.2	L0V.1	L0V.0
0BH	**PFV**	PFV.7	PFV.6	PFV.5	PFV.4	PFV.3	PFV.2	PFV.1	PFV.0
0CH	**OCD1V/OCD1T**	OCD1V3	OCD1V2	OCD1V1	OCD1V0	OCD1T3	OCD1T2	OCD1T1	OCD1T0
0DH	**OCD2V/OCD2T**	OCD2V3	OCD2V2	OCD2V1	OCD2V0	OCD2T3	OCD2T2	OCD2T1	OCD2T0
0EH	**SCV/SCT**	SCV3	SCV2	SCV1	SCV0	SCT3	SCT2	SCT1	SCT0
0FH	**OCCV/OCCT**	OCCV3	OCCV2	OCCV1	OCCV0	OCCT3	OCCT2	OCCT1	OCCT0
10H	**MOST/OCRT/PFT**	CHS1	CHS0	MOST1	MOST0	OCRT1	OCRT0	PFT1	PFT0
11H	**OTC**	OTC7	OTC6	OTC5	OTC4	OTC3	OTC2	OTC1	OTC0
12H	**OTCR**	OTCR7	OTCR6	OTCR5	OTCR4	OTCR3	OTCR2	OTCR1	OTCR0
13H	**UTC**	UTC7	UTC6	UTC5	UTC4	UTC3	UTC2	UTC1	UTC0
14H	**UTCR**	UTCR7	UTCR6	UTCR5	UTCR4	UTCR3	UTCR2	UTCR1	UTCR0
15H	**OTD**	OTD7	OTD6	OTD5	OTD4	OTD3	OTD2	OTD1	OTD0
16H	**OTDR**	OTDR7	OTDR6	OTDR5	OTDR4	OTDR3	OTDR2	OTDR1	OTDR0
17H	**UTD**	UTD7	UTD6	UTD5	UTD4	UTD3	UTD2	UTD1	UTD0
18H	**UTDR**	UTDR7	UTDR6	UTDR5	UTDR4	UTDR3	UTDR2	UTDR1	UTDR0
19H	**TR**	-	TR6	TR5	TR4	TR3	TR2	TR1	TR0
1AH~3FH	**Reserved**	-	-	-	-	-	-	-	-

Table10. RAM Register List

No. (Hex)	Name	Status bits							
		7	6	5	4	3	2	1	0
40H	**CONF**	OCRC	PCHMOS	DSGMOS	CHGMOS	CADCON	ENWDT	SLEEP	IDLE
41H	**BALANCEH**	CB16	CB15	CB14	CB13	CB12	CB11	CB10	CB9
42H	**BALANCEL**	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1
43H	**BSTATUS1**	WDT	PF	SC	OCC	OCD2	OCD1	UV	OV
44H	**BSTATUS2**	-	-	-	-	OTD	UTD	OTC	UTC
45H	**BSTATUS3**	CHGING	DSGING	-	-	L0V	PCHG_FET	CHG_FET	DSG_FET
46H	**TEMP1H**	TEMP1.15	TEMP1.14	TEMP1.13	TEMP1.12	TEMP1.11	TEMP1.10	TEMP1.9	TEMP1.8
47H	**TEMP1L**	TEMP1.7	TEMP1.6	TEMP1.5	TEMP1.4	TEMP1.3	TEMP1.2	TEMP1.1	TEMP1.0
48H	**TEMP2H**	TEMP2.15	TEMP2.14	TEMP2.13	TEMP2.12	TEMP2.11	TEMP2.10	TEMP2.9	TEMP2.8
49H	**TEMP2L**	TEMP2.7	TEMP2.6	TEMP2.5	TEMP2.4	TEMP2.3	TEMP2.2	TEMP2.1	TEMP2.0
4AH	**TEMP3H**	TEMP3.15	TEMP3.14	TEMP3.13	TEMP3.12	TEMP3.11	TEMP3.10	TEMP3.9	TEMP3.8
4BH	**TEMP3L**	TEMP3.7	TEMP3.6	TEMP3.5	TEMP3.4	TEMP3.3	TEMP3.2	TEMP3.1	TEMP3.0
4CH	**CURH**	CUR.15	CUR.14	CUR.13	CUR.12	CUR.11	CUR.10	CUR.9	CUR.8
4DH	**CURL**	CUR.7	CUR.6	CUR.5	CUR.4	CUR.3	CUR.2	CUR.1	CUR.0
4EH	**CELL1H**	CELL1.15	CELL1.14	CELL1.13	CELL1.12	CELL1.11	CELL1.10	CELL1.9	CELL1.8
4FH	**CELL1L**	CELL1.7	CELL1.6	CELL1.5	CELL1.4	CELL1.3	CELL1.2	CELL1.1	CELL1.0
50H	**CELL2H**	CELL2.15	CELL2.14	CELL2.13	CELL2.12	CELL2.11	CELL2.10	CELL2.9	CELL2.8
51H	**CELL2L**	CELL2.7	CELL2.6	CELL2.5	CELL2.4	CELL2.3	CELL2.2	CELL2.1	CELL2.0
52H	**CELL3H**	CELL3.15	CELL3.14	CELL3.13	CELL3.12	CELL3.11	CELL3.10	CELL3.9	CELL3.8
53H	**CELL3L**	CELL3.7	CELL3.6	CELL3.5	CELL3.4	CELL3.3	CELL3.2	CELL3.1	CELL3.0
54H	**CELL4H**	CELL4.15	CELL4.14	CELL4.13	CELL4.12	CELL4.11	CELL4.10	CELL4.9	CELL4.8
55H	**CELL4L**	CELL4.7	CELL4.6	CELL4.5	CELL4.4	CELL4.3	CELL4.2	CELL4.1	CELL4.0
56H	**CELL5H**	CELL5.15	CELL5.14	CELL5.13	CELL5.12	CELL5.11	CELL5.10	CELL5.9	CELL5.8
57H	**CELL5L**	CELL5.7	CELL5.6	CELL5.5	CELL5.4	CELL5.3	CELL5.2	CELL5.1	CELL5.0
58H	**CELL6H**	CELL6.15	CELL6.14	CELL6.13	CELL6.12	CELL6.11	CELL6.10	CELL6.9	CELL6.8
59H	**CELL6L**	CELL6.7	CELL6.6	CELL6.5	CELL6.4	CELL6.3	CELL6.2	CELL6.1	CELL6.0
5AH	**CELL7H**	CELL7.15	CELL7.14	CELL7.13	CELL7.12	CELL7.11	CELL7.10	CELL7.9	CELL7.8
5BH	**CELL7L**	CELL7.7	CELL7.6	CELL7.5	CELL7.4	CELL7.3	CELL7.2	CELL7.1	CELL7.0
5CH	**CELL8H**	CELL8.15	CELL8.14	CELL8.13	CELL8.12	CELL8.11	CELL8.10	CELL8.9	CELL8.8
5DH	**CELL8L**	CELL8.7	CELL8.6	CELL8.5	CELL8.4	CELL8.3	CELL8.2	CELL8.1	CELL8.0
5EH	**CELL9H**	CELL9.15	CELL9.14	CELL9.13	CELL9.12	CELL9.11	CELL9.10	CELL9.9	CELL9.8
5FH	**CELL9L**	CELL9.7	CELL9.6	CELL9.5	CELL9.4	CELL9.3	CELL9.2	CELL9.1	CELL9.0
60H	**CELL10H**	CELL10.15	CELL10.14	CELL10.13	CELL10.12	CELL10.11	CELL10.10	CELL10.9	CELL10.8

Table11. RAM Register List

No.(Hex)	Name	Status bits							
		7	6	5	4	3	2	1	0
61H	**CELL10L**	CELL10.7	CELL10.6	CELL10.5	CELL10.4	CELL10.3	CELL10.2	CELL10.1	CELL10.0
62H	**CELL11H**	CELL11.15	CELL11.14	CELL11.13	CELL11.12	CELL11.11	CELL11.10	CELL11.9	CELL11.8
63H	**CELL11L**	CELL11.7	CELL11.6	CELL11.5	CELL11.4	CELL11.3	CELL11.2	CELL11.1	CELL11.0
64H	**CELL12H**	CELL12.15	CELL12.14	CELL12.13	CELL12.12	CELL12.11	CELL12.10	CELL12.9	CELL12.8
65H	**CELL12L**	CELL12.7	CELL12.6	CELL12.5	CELL12.4	CELL12.3	CELL12.2	CELL12.1	CELL12.0
66H	**CELL13H**	CELL13.15	CELL13.14	CELL13.13	CELL13.12	CELL13.11	CELL13.10	CELL13.9	CELL13.8
67H	**CELL13L**	CELL13.7	CELL13.6	CELL13.5	CELL13.4	CELL13.3	CELL13.2	CELL13.1	CELL13.0
68H	**CELL14H**	CELL14.15	CELL14.14	CELL14.13	CELL14.12	CELL14.11	CELL14.10	CELL14.9	CELL14.8
69H	**CELL14L**	CELL14.7	CELL14.6	CELL14.5	CELL14.4	CELL14.3	CELL14.2	CELL14.1	CELL14.0
6AH	**CELL15H**	CELL15.15	CELL15.14	CELL15.13	CELL15.12	CELL15.11	CELL15.10	CELL15.9	CELL15.8
6BH	**CELL15L**	CELL15.7	CELL15.6	CELL15.5	CELL15.4	CELL15.3	CELL15.2	CELL15.1	CELL15.0
6CH	**CELL16H**	CELL16.15	CELL16.14	CELL16.13	CELL16.12	CELL16.11	CELL16.10	CELL16.9	CELL16.8
6DH	**CELL16L**	CELL16.7	CELL16.6	CELL16.5	CELL16.4	CELL16.3	CELL16.2	CELL16.1	CELL16.0
6EH	**CADCDH**	CDATA.15	CDATA.14	CDATA.13	CDATA.12	CDATA.11	CDATA.10	CDATA.9	CDATA.8
6FH	**CADCDL**	CDATA.7	CDATA.6	CDATA.5	CDATA.4	CDATA.3	CDATA.2	CDATA.0	CDATA.0
70H	**BFLAG1**	WDT_FLG	PF_FLG	SC_FLG	OCC_FLG	LOAD_FLG	OCD_FLG	UV_FLG	OV_FLG
71H	**BFLAG2**	RST_FLG	WAKE_FLG	CADC_FLG	VADC_FLG	OTD_FLG	UTD_FLG	OTC_FLG	UTC_FLG
72H	**RSTSTAT**	-	-	-	-	-	-	WDT1	WDT0

13.4 RAM Other Registers

Table 13.26 System Configuration Register

40H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONF	OCRC	PCHMOS	DSGMOS	CHGMOS	CADCON	ENWDT	SLEEP	IDLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default (POR/WDT/LVR/PIN)	0	1	1	1	0	0	0	0

Bit Number	Symbol	Description
7	**OCRC**	Overcurrent protection software recovery control, write the OCRC bit consecutively according to the "0-1-0" timing
6	**PCHMOS**	Precharge MOSFET control 0: Off 1: Precharge MOSFET is controlled by hardware protection
5	**DSGMOS**	Discharge MOSFET control 0: Off 1: Discharge MOSFET is controlled by hardware protection
4	**CHGMOS**	Charge MOSFET control 0: Off 1: Charge MOSFET is controlled by hardware protection
3	**CADCON**	CADC enable control 0: Disable 1: Enable
2	**ENWDT**	Watchdog enable control 0: Disable 1: Enable
1	**SLEEP**	SLEEP state configuration 0: Normal state 1: SH367309 enter the SLEEP state, the hardware will automatically clear after wakeup Note: When set to "1", if SH367309 is connected to the charger, the SLEEP state will not be entered and the hardware will automatically clear it
0	**IDLE**	IDLE state configuration 0: Normal state 1: SH367309 enter the IDLE state, the hardware will automatically clear after wakeup Note: When set to "1", if there is any protection on SH367309, the IDLE state will not be entered and the hardware will automatically clear it

Table 13.27 System Status Register1

43H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSTATUS1	WDT	PF	SC	OCC	OCD2	OCD1	UV	OV
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7	**WDT**	Watchdog status bit 1:Watchdog overflow 0:Watchdog does not overflow
6	**PF**	Secondary overvoltage protection status 1: Protection occurring 0: Protection has not occurring
5	**SC**	Short circuit protection status 1: Protection occurring 0: Protection has not occurring
4	**OCC**	Charge Overcurrent protection status 1: Protection occurring 0: Protection has not occurring
3	**OCD2**	Discharge Overcurrent level-1 protection status 1: Protection occurring 0: Protection has not occurring
2	**OCD1**	Discharge Overcurrent level-2 protection status 1: Protection occurring 0: Protection has not occurring
1	**UV**	Undervoltage protection status 1: Protection occurring 0: Protection has not occurring
0	**OV**	Overvoltage protection status 1: Protection occurring 0: Protection has not occurring

Table 13.28 System Status Register2

44H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSTATUS2	-	-	-	-	OTD	UTD	OTC	UTC
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7:4	**-**	Reserved
3	**OTD**	Discharge overtemperature protection status 1: Protection occurring 0: Protection has not occurring
2	**UTD**	Discharge undertemperature protection status 1: Protection occurring 0: Protection has not occurring
1	**OTC**	Charge overtemperature protection status 1: Protection occurring 0: Protection has not occurring
0	**UTC**	Charge undertemperature protection status 1: Protection occurring 0: Protection has not occurring

Table 13.29 System Status Register3

45H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSTATUS3	CHGING	DSGING	-	-	L0V	PCHG_FET	CHG_FET	DSG_FET
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7	**CHGING**	Charging status 1: Charging 0: Non-charging
6	**DSGING**	Discharging status 1: Discharging 0: Non-Discharging
5:4	**-**	Reserved
3	**L0V**	Low voltage prohibition charge status 1: Low voltage prohibition charge occurring 0: No Low voltage prohibition charge occurring
2	**PCHG_FET**	Precharge MOSFET status 1: On 0: Off
1	**CHG_FET**	Charge MOSFET status 1: On 0: Off
0	**DSG_FET**	Discharge MOSFET status 1: On 0: Off

Table 13.30 System Flag Register1

70H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BFLAG1	WDT_FLG	PF_FLG	SC_FLG	OCC_FLG	LOAD_FLG	OCD_FLG	UV_FLG	OV_FLG
R/W	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”	R/W“0”
Default	0	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7	**WDT_FLG**	Watchdog overflow flag 1: Watchdog overflow occurred 0: Watchdog overflow has not occurred
6	**PF_FLG**	Secondary overvoltage protection flag 1: Protection occurred 0: Protection has not occurred
5	**SC_FLG**	Short circuit protection flag 1: Protection occurred 0: Protection has not occurred
4	**OCC_FLG**	Charge Overcurrent protection flag 1: Protection occurred 0: Protection has not occurred
3	**LOAD_FLG**	LDO3 overcurrent flag 1: LDO3 overcurrent occurred 0: LDO3 overcurrent has not occurred
2	**OCD_FLG**	Discharge Overcurrent protection flag 1: Protection occurred 0: Protection has not occurred
1	**UV_FLG**	Undervoltage protection flag 1: Protection occurred 0: Protection has not occurred
0	**OV_FLG**	Overvoltage protection flag 1: Protection occurred 0: Protection has not occurred

Table 13.31 System Flag Register2

71H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BFLAG2	RST_FLG	WAKE_FLG	CADC_FLG	VADC_FLG	OTD_FLG	UTD_FLG	OTC_FLG	UTC_FLG
R/W	R/W“0”	R/W“0”	R	R	R/W“0”	R/W“0”	R/W“0”	R/W”0”
Default	1	0	0	0	0	0	0	0

Bit Number	Symbol	Description
7	**RST_FLG**	Reset flag 1: This bit is set to 1 after system reset, and the MCU can be cleared 0: Not reset
6	**WAKE_FLG**	Wakeup flag 1: Wake up from IDLE state (detected charge and discharge current) or SLEEP state (charger connection) 0: Not awakened
5	**CADC_FLG**	CADC interrupt flag 1: CADC interrupt occurred 0: CADC interrupt has not occurred After the register is read, this bit will be automatically cleared
4	**VADC_FLG**	VADC interrupt flag 1: VADC interrupt occurred 0: VADC interrupt has not occurred After the register is read, this bit will be automatically cleared
3	**OTD_FLG**	Discharge overtemperature protection flag 1: Protection occurred 0: Protection has not occurred
2	**UTD_FLG**	Discharge undertemperature protection flag 1: Protection occurred 0: Protection has not occurred
1	**OTC_FLG**	Charge overtemperature protection flag 1: Protection occurred 0: Protection has not occurred
0	**UTC_FLG**	Charge undertemperature protection flag 1: Protection occurred 0: Protection has not occurred

13.5 EEPROM Map Register

00H~3FH is the corresponding address mapping area of EEPROM. Refer to EEPROM register for related characteristics and functions of registers.

13.6 Other Register

The ADC related registers are described in detail in the specification and are not described here.

14. Absolute Maximum Ratings

The absolute maximum ratings are rated values which should not be exceeded. Only when SH367309 works under absolute maximum ratings, the functions can be guaranteed.

Table12. Absolute Maximum Ratings

Name	Type	Pin name	Maximum Range	unit
Power	Analog	VBAT	VSS -0.3 ~ 80	V
	Analog	LDO_P	VSS-0.3~13	V
Input	Analog	RS1	VSS-0.3 ~ VSS+0.3	V
	Analog	VC1	-0.3 ~ 5	V
	Analog	VC2	-0.3 ~ 13	V
	Analog	VC3~VC17	VSS -0.3 ~ 80	V
	Analog	RS2	VSS-1V ~ V_{CC}+0.3	V
	Analog	CHGD/DSGD	V_{BAT}-70 ~ V_{BAT}+0.3	V
	Analog	CTL/SHIP/ MODE/LDO_EN	VSS-0.3 ~ V_{BAT}+0.3	V
	Analog	T1~T3	VSS-0.3 ~ V_{CC}+0.3	V
	Digital	SCL/SDA	VSS-0.3 ~ 5.5	V
	Analog	VPRO	VSS-0.3 ~ V_{PRO}+0.3	V
Output	Analog	CHG/PCHG	V_{BAT}-70 ~ V_{11}+0.3	V
	Analog	DSG	VSS-0.3 ~ V_{11}+0.3	V
	Analog	PF	VSS-0.3 ~ V_{BAT}+0.3	V
	Analog	V11/ CAPP/	VSS-0.3 ~ V_{11}+0.3	V
	Analog	CAPS/CAPN	VSS-0.3 ~ 5.5	V
	Digital	VCC/ALARM	VSS-0.3 ~ 5.5	V
	Analog	LDO_O	VSS-0.3~5.5	V
Operating Ambient Temperature			-40 to 85	℃
Storage Temperature			-40 to 125	℃

15. Electrical Characteristics

15.1 Electrical characteristic(TA=25℃, unless otherwise specified)

Operating Parameter						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{BAT}	Operating Voltage	8.5	-	70	V	No protection occurs, LDO1 and LDO2 no load
I_{OP1}	AFE Mode	-	70	105	μA	VBAT=60V, AFE mode/Protect Mode current consumption test: No protection occurs, no balance on, LDO1 and LDO2 no load, CHG/DSG floating, measured at chip VSS
I_{OP2}	Protect Mode	-	40	55	μA	
I_{OP3}	Ship Mode	-	1.5	2	μA	
I_{OP4}	IDLE State	-	40	50	μA	
I_{OP5}	Powerdown State	-	3	5	μA	
I_{OP6}	SLEEP State	-	35	45	μA	
I_{VCN-1}	Current Consumption of VCn	-	-	1	μA	VCn-VCn-1=3.8V, for VC1~VC16
I_{VCN-2}	Current Consumption of VCn	-	-	1.5	μA	VCn-VCn-1=3.8V, for VC17

System Configuration						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{H-CTL}	CTL High Level	V_{CC}-0.3	-	V_{BAT}	V	
V_{L-CTL}	CTL Low Level	-	-	0.3	V	
V_{H-MODE}	MODE High Level	V_{BAT}-0.3	-	V_{BAT}	V	
V_{L-MODE}	MODE Low Level	-	-	0.3	V	
V_{H-LDO_EN}	LDO_EN High Level	V_{BAT}-0.3	-	V_{BAT}	V	
V_{L-LDO_EN}	LDO_EN Low Level	-	-	0.3	V	
V_{H-SHIP}	SHIP High Level	V_{BAT}-0.3	-	V_{BAT}	V	
V_{L-SHIP}	SHIP Low Level	-	-	0.3	V	
$T_{L-ALARM}$	ALARM Low Pulse Time	0.8	1	1.2	mS	
$T_{I-ALARM}$	ALARM Low Pulse Interval	0.8	1	1.2	mS	
t_{MOSFET}	Charge MOSFET Turn On Delay	64		512	uS	Can be set in EEPROM register
	Charge MOSFET Turn On Delay Accuracy			64	uS	
t_{cycle}	VADC Measurement Voltage and Current Cycle	95	100	105	mS	Temperature measurements are taken every 1 second

Powerdown State						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{PD}	Powerdown Voltage	V_{UV}-150	V_{UV}-200	V_{UV}-250	mV	
T_{PD}	Powerdown Delay	-	10	-	S	Detect powerdown after undervoltage occurs
T_{WARMUP}	Poweron Warm-up Time	-	-	250	mS	

Digital/Analog Port Level						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Logic Threshold	2	-	5	V	SDA/SCL
V_{IL}	Input Low Logic Threshold	-	-	0.6	V	SDA/SCL
V_{OL}	Output Low Logic Drive	-	-	0.4	V	SDA/SCL, I_{OL}=3mA
		-	-	0.4	V	PF, I_{OL}=100uA
		-	-	0.4	V	ALARM, I_{OL}=1mA
V_{PRO}	Write EEPROM Voltage	7.7	8	8.3	V	

LDO1 Regulator						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{CC}	Regulator Output Drive	3.1	3.3	3.5	V	13≤VBAT≤70V,I_{load}≤10mA
		3.1	3.3	3.5	V	8.5≤VBAT＜13V,I_{load}≤2mA

LDO2 Regulator						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{11}	Regulator Output Drive	8.5	11	13	V	VBAT≥13V, I_{LOAD}=5mA
		8	-	-	V	VBAT=10V, I_{LOAD}=5mA

LDO3 Regulator						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{OUT}	Regulator Output Drive	3.1	3.3	3.5	V	
REG_{LINE}	Voltage Linearity	-	10	50	mV	12≤VBAT≤70V, I_{load}=25mA
REG_{LOAD}	Load Linearity	-	30	100	mV	VBAT=50V, 0.1mA≤I_{load}≤25mA
I_{LOAD}	Overcurrent Threshold	50	75	100	mA	
t_{OVER}	Overcurrent Delay	-	2	-	mS	

Note: When the load current exceeds the overcurrent threshold I_{LOAD}, the system will lock to the maximum current, and the output voltage cannot be guaranteed at this time.

Voltage Measurement						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{IN1}	Measurement Range	0	-	5	V	
T_{IN1}	Measurement Cycle	-	5	-	mS	
V_{ACC}	Absolute Accuracy	-5	-	5	mV	

Temperature Measurement						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{IN2}	Measurement Range	0	-	3	V	
T_{IN2}	Measurement Cycle	-	5	-	mS	
T_{ACC}	Absolute Accuracy	-2	-	2	℃	

Current Measurement						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{IN3}	Measurement Range	-200	-	200	mV	
T_{IN3}	Measurement Cycle	-	5	-	mS	
I_{ACC}	Absolute Accuracy	-150	-	150	uV	

CADC						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{IN4}	Measurement Range	-200	-	200	mV	
T_{IN4}	Measurement Cycle	237.5	250	262.5	mS	4Hz measurement frequency
INL	Integral nonlinearity error	-	±1	±3	LSB	

MOSFET Driver						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{CHGH}/V_{DSGH}/ V_{PCHGH}	CHG/DSG/PCHG High Level Drive	8	11	13	V	VBAT≥13V, External 1MΩ resistor to ground
		6.5	-	-	V	VBAT=8.5V(LDO1、LDO2 no load), External 1MΩ resistor to ground
V_{DSGL}	DSG Low Level Drive	-	-	1	V	I_{OL}=0.5mA
t_{CH}	CHG Rise Time	-	100	200	uS	C_{LOAD} = 50nF, V_{CHG} rised from 10% to 90%
t_{PCH}	PCHG Rise Time	-	500	1000	uS	C_{LOAD} = 4700pF, V_{PCHG} rised from 10% to 90%
t_{DL}	DSG Fall Time	-	150	400	uS	C_{LOAD} = 50nF, External resistance is 1kΩ,V_{DSG} falled from 90% to 10%
t_{DH}	DSG Rise Time	-	200	600	uS	C_{LOAD} = 50nF, External resistance is 1kΩ, V_{DSG} rised from 10% to 90%

Charge and Discharge State Detection						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{CH}	Charge and Discharge State Detection Voltage	50	200	350	uV	CHS[1:0]=00
		350	500	650	uV	CHS[1:0]=01
		850	1000	1150	uV	CHS[1:0]=10
		1850	2000	2150	uV	CHS[1:0]=11

Overvoltage Protection						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{OV}	Overvoltage Detection Threshold	3.6	-	4.5	V	Can be set in EEPROM register
V_{OVR}	Overvoltage Recovery Detection Threshold	3.3	-	4.5	V	Can be set in EEPROM register
V_{OVA}	Detection Accuracy	-25	-	25	mV	
t_{OV}	Overvoltage Detection Delay	0.1	-	40	S	Can be set in EEPROM register
	Detection Accuracy	100mS -t_{OV}*5%		200mS +t_{OV}*5%		
t_{OVR}	Overvoltage Recovery Detection Delay	-	2*t_{cycle}	-	mS	t_{cycle}=100mS

Undervoltage Protection						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{UV}	Undervoltage Detection Threshold	2.0	-	3.1	V	Can be set in EEPROM register
V_{UVR}	Undervoltage Recovery Detection Threshold	2.0	-	3.6	V	Can be set in EEPROM register
V_{UVA}	Detection Accuracy	-25	-	25	mV	
T_{UV}	Undervoltage Detection Delay	0.1	-	40	S	Can be set in EEPROM register
	Detection Accuracy	100mS $-t_{UV}$*5%		200mS $+t_{UV}$*5%		
T_{UVR}	Undervoltage protection recovery delay	-	$2*t_{cycle}$	-	mS	t_{cycle}=100mS

Balance						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{BAL}	Balance Detection Threshold	3.3	-	4.5	V	Can be set in EEPROM register
V_{BALA}	Detection Accuracy	-25	-	25	mV	
R_{BL}	Internal Resistance for Balance	120	260	400	Ω	Cell voltage is equal to V_{BAL}+100mV
$t_{balanceT}$	Balance Detection Delay	-	400	-	mS	

Load / Charger / Current detection						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{CHGD1}	Charger Detection Level 1	-0.25	-	-	V	Enter/exit SLEEP state, charger detection mode: CHGD level is less than V_{CHGD1}, judged as charger connection
V_{CHGD2}	Charger Detection Level 2	-	-	-0.05	V	Charge overcurren release, charger detection mode: CHGD level greater than V_{CHGD2}, judged as charger release
V_{CHGD3}	Charger Detection Level 3	1.0	-	-	V	Enter/Exit Powerdown state, charger detection mode: CHGD level is less than V_{CHGD3}, judged as charger connection
V_{DSGD}	Load Detection Threshold	1.0	-	-	V	
R_{DSGD}	DSGD Internal Pull-down Resistor	500	900	1400	KΩ	VBAT=50V,DSGD external 3V supply
V_{CD1}	Discharging Current Detection Threshold	0.5	1.4	2.6	mV	
V_{CD2}	Charging Current Detection Threshold	-2.6	-1.4	-0.5	mV	
t_{CD}	Charging and Discharging Current Detection Delay	10	15	20	mS	This interval is awaken from IDLE to ALARM output low pulse

Precharge						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{PCH}	Precharge Detection Threshold	1.0	-	3.0	V	Can be set in EEPROM register
V_{PCHA}	Detection Accuracy	-25	-	25	mV	
t_{PCHG}	Precharge Detection Delay	950	1000	1250	mS	

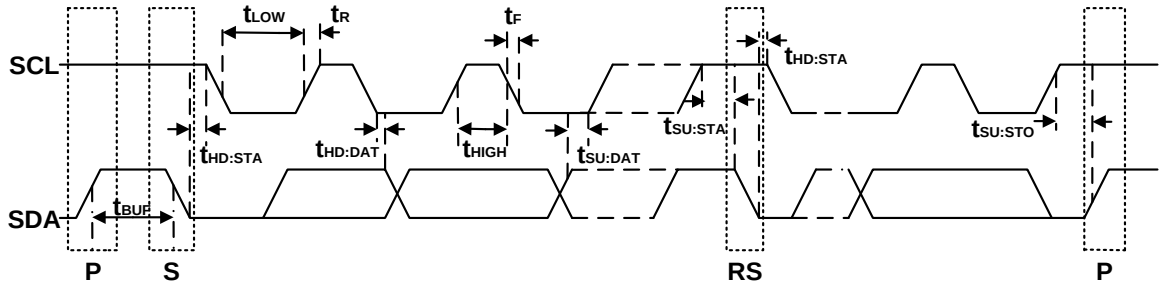
Secondary Overvoltage Protection						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{P2N}	Secondary Overvoltage Detection Threshold	3.8	-	5	V	Can be set in EEPROM register
V_{P2NA}	Detection Accuracy	-25	-	25	mV	
t_{P2N}	Secondary Overvoltage Detection Delay	8	-	64	S	Can be set in EEPROM register
	Detection Accuracy	100mS $-t_{P2N}$*5%		200mS $+t_{P2N}$*5%		

Low Voltage Prohibition Charge						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{L0V}	Low Voltage Prohibition Charge Detection Threshold	0.5	-	2	V	Can be set in EEPROM register
V_{L0VA}	Detection Accuracy	-25	-	25	mV	

Overcurrent						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{DOC1}	Discharge Overcurrent1 Detection Threshold	20	-	200	mV	Can be set in EEPROM register
V_{DOCA1}	Detection Accuracy	-10	-	10	mV	V_{DOC1} < 100mV
		-10%		10%	V_{DOC1}	V_{DOC1} ⩾ 100mV
t_{DOC1}	Discharge Overcurrent1 Detection Delay	0.05	-	40	S	Can be set in EEPROM register
	Detection Accuracy	$-t_{DOC1}$*5%		t_{DOC1}*5%		
V_{DOC2}	Discharge Overcurrent2 Detection Threshold	30	-	500	mV	Can be set in EEPROM register
V_{DOCA2}	Detection Accuracy	-10	-	10	mV	V_{DOC2} < 100mV
		-10%		10%	V_{DOC2}	V_{DOC2} ⩾ 100mV
t_{DOC2}	Discharge Overcurrent2 Detection Delay	0.01	-	20	S	Can be set in EEPROM register
	Detection Accuracy	$-t_{DOC2}$*5%		t_{DOC2}*5%		
V_{DOC3}	Discharge Short Circuit Detection Threshold	50	-	1000	mV	Can be set in EEPROM register
V_{DOCA3}	Detection Accuracy	-10	-	10	mV	V_{DOC3} < 100mV
		-10%		10%	V_{DOC3}	V_{DOC3} ⩾ 100mV
t_{DOC3}	Discharge Short Circuit Detection Delay	0	-	960	μS	During test, short circuit protection input voltage ≥ 500mV+100mV
	Detection Accuracy	0		64	uS	
V_{COC}	Charge Overcurrent Detection Threshold	-200	-	-20	mV	Can be set in EEPROM register
V_{COCA}	Detection Accuracy	-10	-	10	mV	V_{COC} < 100mV
		-10%	-	10%	V_{COC}	V_{COC} ⩾ 100mV
t_{COC}	Charge Overcurrent Detection Delay	0.01	-	20	S	Can be set in EEPROM register
	Detection Accuracy	$-t_{COC}$*5%		t_{COC}*5%		
t_{D1}	Discharge Overcurrent Detection Load Release Delay	100	-	2000	mS	Can be set in EEPROM register
	Detection Accuracy	$-t_{D1}$*5%		t_{D1}*5%		
t_{D2}	Charger Release Delay	400	500	600	mS	Exit charge overcurren
t_{D3}	Charger Connection Detection Delay	400	500	600	mS	Exit the SLEEP state or "Power on to be activated"
t_{AUTO}	Overcurrent Recovery Delay	8	-	64	S	Can be set in EEPROM register
	Detection Accuracy	$-t_{AUTO}$*5%		t_{AUTO}*5%		

Temperature Protection						
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
T_{OTC}	Charge Overtemperature Detection Threshold	45	-	70	℃	Can be set in EEPROM register, one step is 1℃
T_{UTC}	Charge Undertemperature Detection Threshold	-20	-	10	℃	Can be set in EEPROM register, one step is 1℃
T_{OTD}	Discharge Overtemperature Detection Threshold	45	-	80	℃	Can be set in EEPROM register, one step is 1℃
T_{UTD}	Discharge Undertemperature Detection Threshold	-40	-	10	℃	Can be set in EEPROM register, one step is 1℃
T_{OTCR}	Charge Overtemperature Recovery Detection Threshold	40	-	70	℃	Can be set in EEPROM register, one step is 1℃
T_{UTCR}	Charge Undertemperature Recovery Detection Threshold	-20	-	15	℃	Can be set in EEPROM register, one step is 1℃
T_{OTDR}	Discharge Overtemperature Recovery Detection Threshold	40	-	80	℃	Can be set in EEPROM register, one step is 1℃
T_{UTDR}	Discharge Undertemperature Recovery Detection Threshold	-40	-	15	℃	Can be set in EEPROM register, one step is 1℃
t_T	Temperature Potection Detection Delay	-	2	-	S	
T_{OA}	Detection Accuracy	-	±2	±4	℃	

TWI Timing						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	Conditions
TWI Clock Frequency	f_{TWI}	10	-	100	kHz	
Time the bus must be free before new transmission can start	t_{BUF}	4.7	-	-	μs	
SCL Pulse Width Low	t_{LOW}	4.7	-	-	μs	
SCL Pulse Width High	t_{HIGH}	4.0	-	50	μs	
Data Out Hold Time After Clock Low	$t_{HD:DAT}$	300	-	-	ns	
Data Setup Time	$t_{SU:DAT}$	250	-	-	ns	
START condition hold time after which first clock pulse is generated	$t_{HD:STA}$	4.0	-	-	μs	
Setup time for START condition	$t_{SU:STA}$	4.7	-	-	μs	
Setup time for STOP condition	$t_{SU:STO}$	4.0	-	-	μs	
Rise time	t_R	-	-	1000	ns	$(V_{ILMAX} – 0.15V)$ to $(V_{IHMIN}+ 0.15V)$
Fall Time	t_F	-	-	300	ns	$(V_{IHMIN}+ 0.15V)$ to $(V_{ILMAX} – 0.15)$
Timeout	$t_{TIMEOUT}$	-	25	-	ms	
RC Frequency Accuracy	f_E	-	-	±10	%	T_A=-40℃~85 ℃



15.2 Electrical characteristic(TA=-40℃~85℃unless otherwise specified)

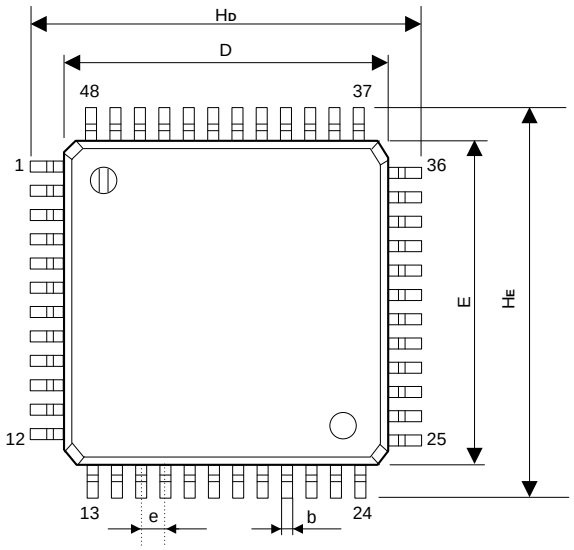
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
T_A	Operating Ambient Temperature	-40	-	85	℃	
I_{OP1}	AFE Mode	-	70	105	μA	VBAT=60V,AFE mode/Protect Mode current consumption test: No protection appears, no balance on, LDO1, LDO2 no load, CHG/DSG floating, measured at chip VSS
I_{OP2}	Protect Mode	-	40	55	μA	
I_{OP3}	Ship Mode	-	1.5	2	μA	
I_{OP4}	IDLE state	-	40	50	μA	
I_{OP5}	Powerdown State	-	3	6	μA	
I_{OP6}	SLEEP State	-	35	45	μA	
I_{VCN-1}	Current Consumption of VCn	-	-	1	μA	VCn-VCn-1=3.8V, for VC1~VC16
I_{VCN-2}	Current Consumption of VCn	-	-	2	μA	VCn-VCn-1=3.8V, for VC17
t_{CH}	CHG Rise Time	-	100	200	uS	C_{LOAD} = 50nF,V_{CHG} rised from 10% to 90%
t_{PCH}	PCHG Rise Time	-	500	1000	uS	C_{LOAD} = 4700pF,V_{PCHG} rised from 10% to 90%
t_{DL}	DSG Fall Time	-	150	400	uS	C_{LOAD} = 50nF,External resistance is 1kΩ,V_{DSG} falled from 90% to 10%
t_{DH}	DSG Rise Time	-	200	600	uS	C_{LOAD} = 50nF,External resistance is 1kΩ,V_{DSG} rised from 10% to 90%
V_{CH}	Charge and Discharge state Detection Voltage	50	200	350	uV	CHS[1:0]=00
		350	500	650	uV	CHS[1:0]=01
		850	1000	1150	uV	CHS[1:0]=10
		1850	2000	2150	uV	CHS[1:0]=11
R_{BL}	Internal Resistance for Balance	75	300	500	Ω	Cell voltage is equal to V_{BAL}+100mV
V_{OVA}	Overvoltage/Recovery Detection Accuracy	-50	-	50	mV	
V_{UVA}	Undervoltage/Recovery Detection Accuracy	-50	-	50	mV	
V_{BALA}	Balance Detection Accuracy	-50	-	50	mV	
V_{PCHA}	Precharge Detection Accuracy	-50	-	50	mV	
V_{P2NA}	Secondary Overvoltage Detection Accuracy	-50	-	50	mV	
V_{L0VA}	Low Voltage Prohibition Charge Detection Accuracy	-50	-	50	mV	
V_{CHGD1}	Charger Detection Level 1	-0.25	-	-	V	Enter/exit SLEEP state, charger detection mode: CHGD level is less than V_{CHGD1}, judged as charger connection
V_{CHGD2}	Charger Detection Level 2	-	-	-0.05	V	Charge overcurren release, charger detection mode: CHGD level greater than V_{CHGD2}, judged as charger release
V_{CHGD3}	Charger Detection Level 3	1.0	-	-	V	Enter/Exit Powerdown state, charger detection mode: CHGD level is less than V_{CHGD3}, judged as charger connection
V_{DSGD}	Load Detection Threshold	1.0	-	-	V	Detect load release

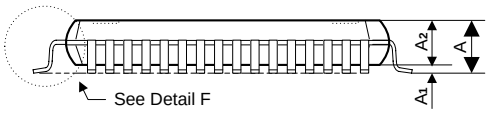
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
R_{DSGD}	DSGD Internal Pull-down Resistor	500	900	1400	KΩ	VBAT=50V,DSGD external 3V supply
V_{CD1}	Discharge current Detection Threshold	0.5	1.4	2.6	mV	
V_{CD2}	Charge current Detection Threshold	-2.6	-1.4	-0.5	mV	
V_{DOCA1}	Discharge Overcurrent1 Detection Accuracy	-10	-	10	mV	V_{DOC1} < 100mV
		-10%	-	10%	V_{DOC1}	V_{DOC1} ≥ 100mV

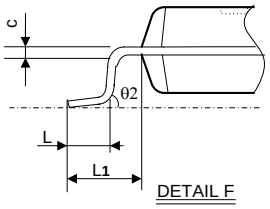
Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
V_{DOCA2}	Discharge Overcurrent2 Detection Accuracy	-10	-	10	mV	V_{DOC2} < 100mV
		-10%	-	10%	V_{DOC2}	V_{DOC2} ≥ 100mV
V_{DOCA3}	Discharge Short circuit Detection Accuracy	-10	-	10	mV	V_{DOC3} < 100mV
		-10%	-	10%	V_{DOC3}	V_{DOC3} ≥ 100mV
V_{COCA}	Charge Overcurrent Detection Accuracy	-10	-	10	mV	V_{COC} < 100mV
		-10%	-	10%	V_{COC}	V_{COC} ≥ 100mV
T_{OA}	Temperature Detection Accuracy	-	±2	±4	℃	

16. Package Information

TQFP 48L **unit: inches/mm**







Symbol	Dimensions in inches		Dimensions in mm	
	MIN	MAX	MIN	MAX
A	---	0.047	---	1.2
A1	0.002	0.006	0.05	0.15
A2	0.035	0.041	0.9	1.05
D	0.270	0.281	6.85	7.15
E	0.270	0.281	6.85	7.15
H_D	0.346	0.362	8.8	9.2
H_E	0.346	0.362	8.8	9.2
b	0.005	0.011	0.15	0.27
e	0.020 TYP		0.500 TYP	
c	0.004	0.008	0.090	0.200
L	0.018	0.030	0.45	0.75
L1	0.033	0.045	0.85	1.15
θ2	0°	10°	0°	10°

Note:

(1) Dimension D does not include mold Flash, protrusions or gate burrs

(2) Unless otherwise specified, Dimensional deviation does not exceed ±0.1mm

(3) Coplanarity: 0.1 mm

(4) Controlling dimension is millimeter, converted unit inch is unrestricted

17. Ordering Information

Product Name	Package	Case	Minimum order quantity
SH367309U/048UR	TQFP48L	Tray	2.5K

18. Specification Change Record

Version	Record	Date
1.2	1. Adjust the maximum operating voltage of the chip 2. Insert "important notice" on last page of SPEC	May 2020
1.1	Update the reference schematic of the CHGD port	August 2019
1.0	Original version	June 2019

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