55/75450A • 55/75451A • 55/75452A
55/75453A • 55/75454A
DUAL PERIPHERAL DRIVERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55/75450A, 55/75451A, 55/75452A, 55/75453A and 55/75454A are Dual High Speed General Purpose Interface Drivers that convert TTL and DTL logic levels to high current drive capability. The 55450A and 75450A feature two TTL NAND gates and two uncommitted transistors. The 55/75451A, 55/75452A, 55/75453A and 55/75454A feature two standard series 74 TTL gates in AND, NAND, OR and NOR configurations respectively, driving the base of two high voltage, high current, uncommitted collector output transistors.

The 55/75450A series offers flexibility in designing high speed logic buffers, power drivers, lamp drivers, line drivers, MOS drivers, clock drivers and memory drivers.

- **NO LATCH-UP AT 20 V**
- **HIGH OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

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TEST TABLE 1 – Operating Temperature Range and Supply Voltage Range

	55450A Series	75450A Series
Temperature, T_A	−55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

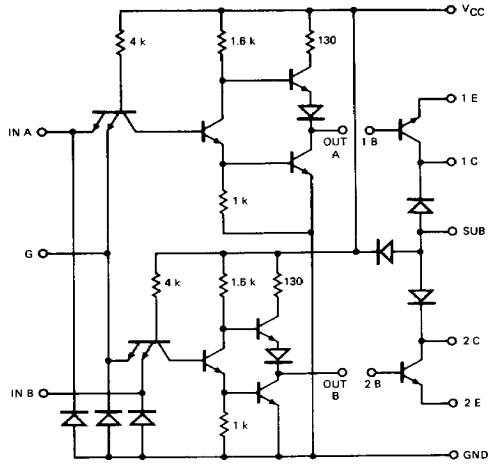
ABSOLUTE MAXIMUM RATINGS

	55450A	75450A	55451A 55452A 55453A 55454A	75451A 75452A 75453A 75454A
Supply Voltage, V_{CC} (See Note 1)	7 V	7 V	7 V	7 V
Input Voltage (See Note 1)	5.5 V	5.5 V	5.5 V	5.5 V
Interemitter Voltage(See Note 2)	5.5 V	5.5 V	5.5 V	5.5 V
V_{CC} to Substrate Voltage (See Note 6)	35 V	35 V		
Collector to Substrate Voltage (See Note 6)	35 V	35 V		
Collector to Base Voltage	35 V	35 V		
Collector to Emitter Voltage (See Note 3)	30 V	30 V		
Emitter to Base Voltage	5 V	5 V		
Output Voltage (See Notes 1 and 4)			30 V	30 V
Continuous Collector Current (See Note 5)	300 mA	300 mA		
Continuous Output Current (See Note 5)			300 mA	300 mA
Continuous Total Power Dissipation (See Note 7)	800 mW	800 mW	800 mW	800 mW
Operating Ambient Temperature Range	−55°C to +125°C	0°C to 70°C	−55°C to +125°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Pin Temperature				
Molded DIP (Soldering, 10 s)		260°C	260°C	260°C
Hermetic DIP (Soldering, 60 s)	300°C	300°C	300°C	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.
6. For the 55450A and 75450A only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation.
7. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C for Hermetic DIP and Molded DIP. For the Molded Mini DIP and Ceramic Mini DIP, derate at 6.7 mW/°C above 30°C.

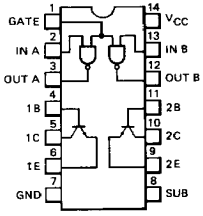
55450A/75450A
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



All resistor values in ohms.

CONNECTION DIAGRAM
14-PIN
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



LOGIC FUNCTION

Positive Logic: $Z = \overline{XY}$ (gate only)
$Z = XY$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
55450A	55450ADM
75450A	75450ADC
75450A	75450APC

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

TTL Gates

SYMBOL	CHARACTERISTICS		TEST FIGURE	CONDITIONS		MIN	TYP (Note 8)	MAX	UNIT
V_{IH}	Input HIGH Voltage		1			2			V
V_{IL}	Input LOW Voltage		2					0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = MIN, V_{IL} = 0.8 V I_{OH} = −400 μA		2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = MIN, V_{IH} = 2 V	55450A		0.22	0.5	V
				I_{OL} = 16 mA	75450A		0.22	0.4	
I_I	Input Current at Maximum Input Voltage	Input A	4	V_{CC} = MAX, V_I = 5.5 V				1	mA
		Input G						2	
I_{IH}	Input HIGH Current	Input A	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Input G						80	
I_{IL}	Input LOW Current	Input A	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Input G						−3.2	
I_{OS}	Short Circuit Output Current (Note 9)		5	V_{CC} = MAX		−18		−55	mA
I_{CCH}	Supply Current, Output HIGH		6	V_{CC} = MAX, V_I = 0 V			2	4	mA
I_{CCL}	Supply Current, Output LOW			V_{CC} = MAX, V_I = 5 V			6	11	

NOTES:
8. All typical values at V_{CC} = 5 V, T_A = 25°C.
9. Not more than one output should be shorted at a time.

55450A/75450A

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

Output Transistors

SYMBOL	CHARACTERISTICS	CONDITIONS		MIN	TYP (Note 10)	MAX	UNITS
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0		35			V
$V_{(BR)CER}$	Collector to Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		30			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 11)	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C		25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA	55450A	10			
			75450A	20			
		V_{CE} = 3 V, I_C = 300 mA	55450A	15			
			75450A	25			
$V_{BE(sat)}$	Base to Emitter Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55450A		0.85	1.2	V
			75450A		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA	55450A		1.05	1.4	V
			75450A		1.05	1.2	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55450A		0.25	0.5	V
			75450A		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA	55450A		0.5	0.8	V
			75450A		0.5	0.7	V

NOTES:
10. All typical values are at V_{CC} = 5 V, T_A = 25°C.
11. These parameters must be measured using the pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C.

TTL Gates

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		12		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8		ns

Output Transistors

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS (Note 12)	MIN	TYP	MAX	UNITS
t_d	Delay Time	13	I_C = 200 mA, $V_{BE(off)}$ = −1 V		10		ns
t_r	Rise Time		$I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA		14		ns
t_s	Storage Time		C_L = 15 pF, R_L = 50 Ω		10		ns
t_f	Fall Time				11		ns

Gates and Transistors Combined

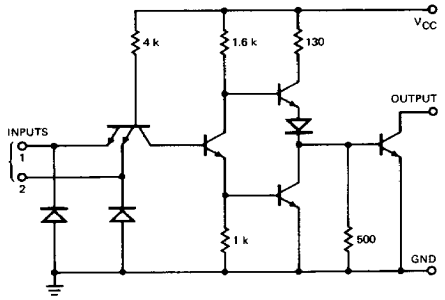
SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		22	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				22	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				10	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				14	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, I_C ≈ 300 mA, R_{BE} = 500 Ω	V_S −6.5			mV

NOTE 12. Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

7

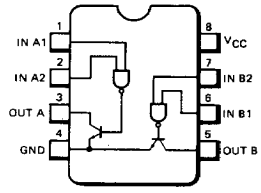
55451A/75451A
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	L	(on state)
L	H	L	(on state)
H	L	L	(on state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55451A	55451ARM
75451A	75451ARC
75451A	75451ATC

Positive Logic: Z = XY

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 13)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IH} = 2 V	55451A			300	μA
				75451A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55451A		0.25	0.5	V
				75451A		0.25	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55451A		0.5	0.8	
				75451A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 5 V			7.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			52	65	mA

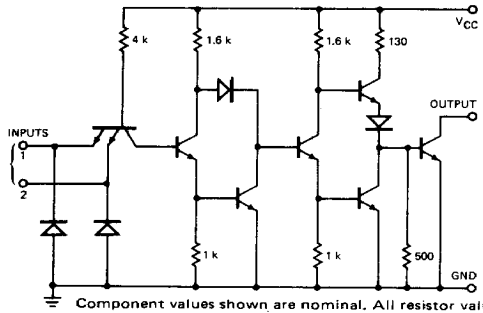
NOTE 13. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISICS: V_{CC} = 5 V, T_A = 25°C.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		20	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				20	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

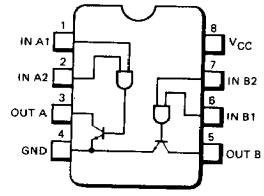
55452A/75452A
DUAL POSITIVE NAND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55452A	55452ARM
75452A	75452ARC
75452A	75452ATC

Positive Logic: $Z = \overline{XY}$

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ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 14)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IL} = 0.8 V	55452A			300	μA
				75452A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55452A		0.25	0.5	V
				75452A		0.25	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55452A		0.5	0.8	
				75452A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 0 V			11	14	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			56	71	mA

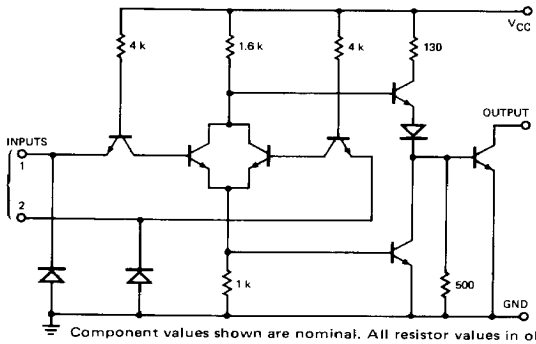
NOTE 14. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		25	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

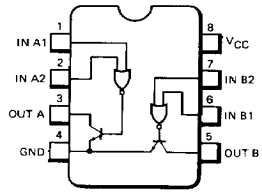
55453A/75453A
DUAL POSITIVE OR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



ORDER INFORMATION

TYPE	PART NO.
55453A	55453ARM
75453A	75453ARC
75453A	75453ATC

Positive Logic: $Z = X + Y$

TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 15)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IH} = 2 V	55453A			300	μA
				75453A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55453A		0.25	0.5	V
				75453A		0.25	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55453A		0.5	0.8	
				75453A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			−1.0	−1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			54	68	mA

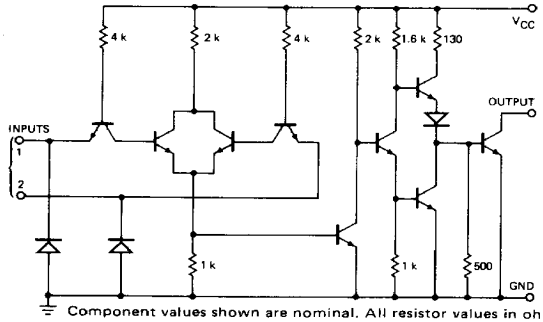
NOTE 15. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25 °C.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		20	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				20	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	25	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S −6.5			mV

55454A/75454A
DUAL POSITIVE NOR PERIPHERAL DRIVER

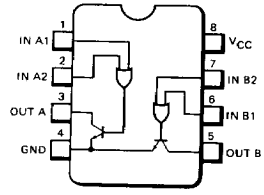
EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAM

8-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55454A	55454ARM
75454A	75454ARC
75454A	75454ATC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 16)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IL} = 0.8 V	55454A			300	μA
				75454A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55454A		0.25	0.5	V
				75454A		0.25	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55454A		0.5	0.8	
				75454A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			−1.0	−1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 0 V			13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			61	79	mA

NOTE 16. All typical values are at V_{CC} = 5 V, T_A = 25°C.

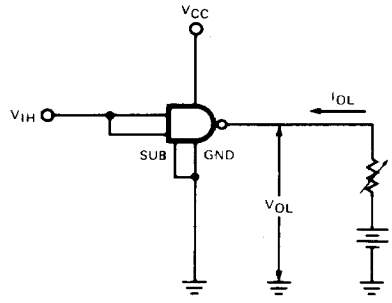
AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		25	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S −6.5			mV

CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUIT†

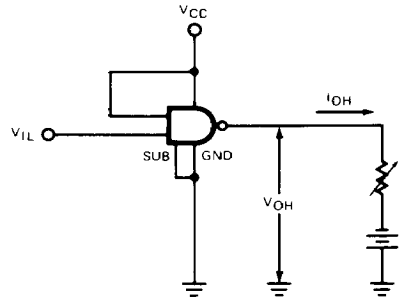
V_{IH}, V_{OL}



Both inputs are tested simultaneously.

Fig. 1

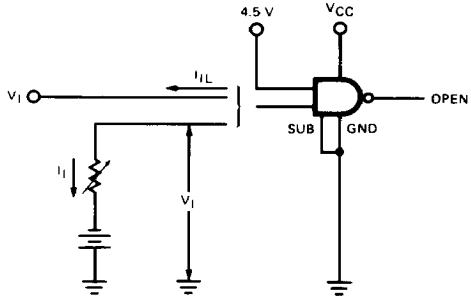
V_{IL}, V_{OH}



Each input is tested separately.

Fig. 2

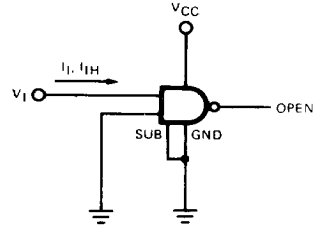
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing V_{CD}, input not under test is open.

Fig. 3

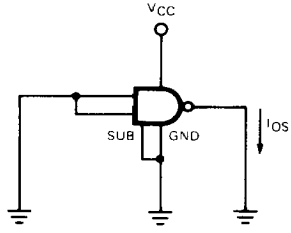
I_I, I_{IH}



Each input is tested separately

Fig. 4

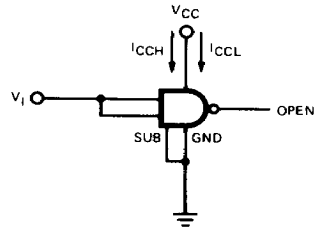
I_{OS}



Each gate is tested separately.
(55450A/75450A only)

Fig. 5

I_{CCH}, I_{CCL}

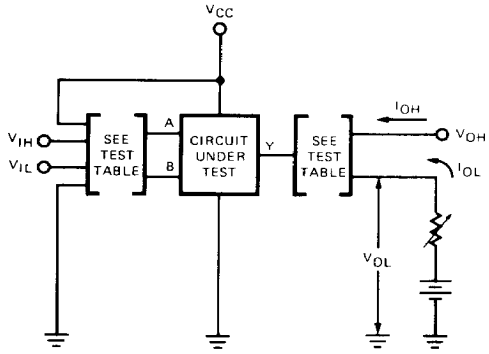


Both gates are tested simultaneously.

Fig. 6

CHARACTERISTICS MEASUREMENT INFORMATION

V_{IH}, V_{IL}, I_{OH}, V_{OL}



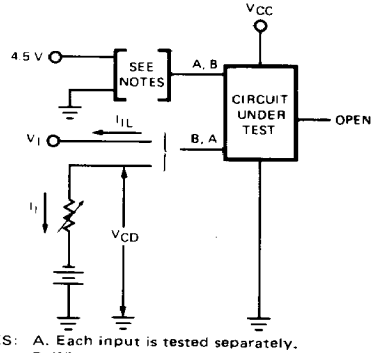
TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75451A	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
55/75452A	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
55/75453A	V_{IH}	GND	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
55/75454A	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

NOTE: Each input is tested separately.

Fig. 7

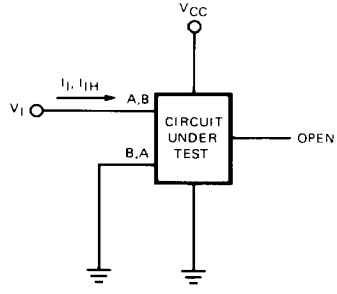
V_{CD}, I_{IL}



NOTES: A. Each input is tested separately.
B. When testing I_{IL} 55/75453A and 55/75454A, the input not under test is grounded. For all other circuits it is at 4.5 V.
C. When testing V_{CD}, input not under test is open.

Fig. 8

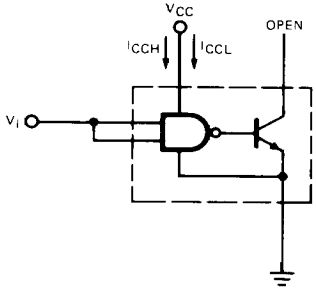
I_I, I_{IH}



Each input is tested separately.

Fig. 9

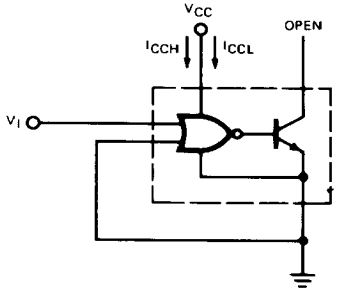
I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 10

I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

Fig. 11

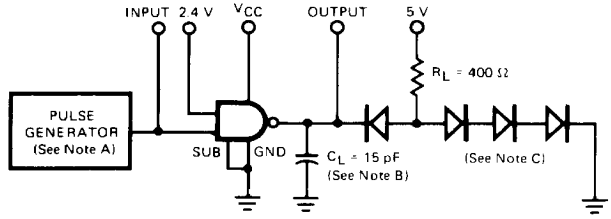
† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

CHARACTERISTICS MEASUREMENT INFORMATION

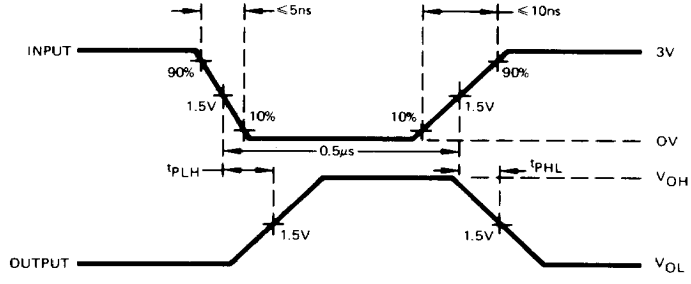
SWITCHING CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE
(55450A, 75450A ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are FD777.

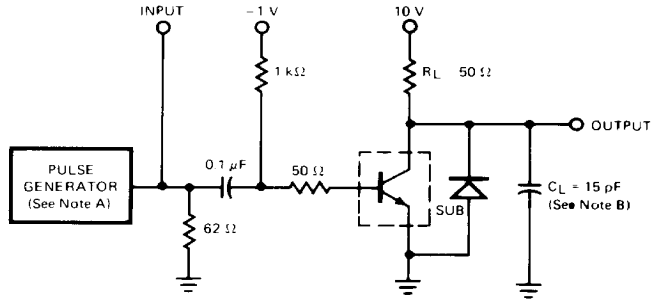
Fig. 12

CHARACTERISTICS MEASUREMENT INFORMATION

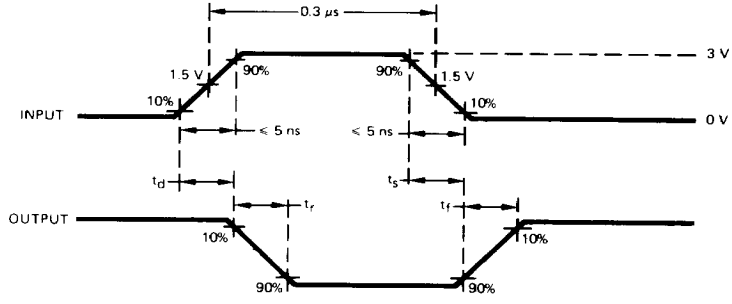
SWITCHING CHARACTERISTICS

SWITCHING TIMES, EACH TRANSISTOR (55450A, 75450A ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Fig. 13

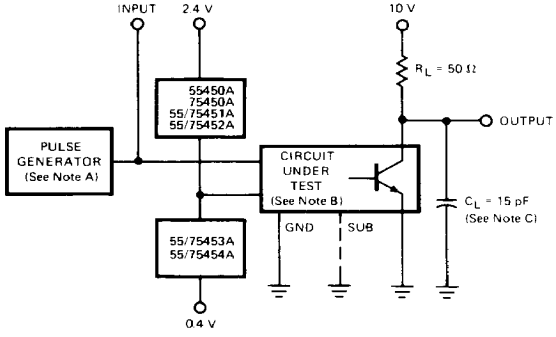
7

CHARACTERISTICS MEASUREMENT INFORMATION

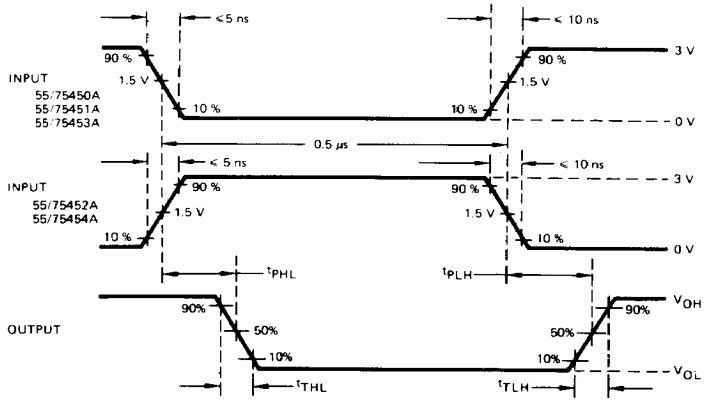
SWITCHING CHARACTERISTICS

SWITCHING TIMES OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When Testing 55450A/75450A, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

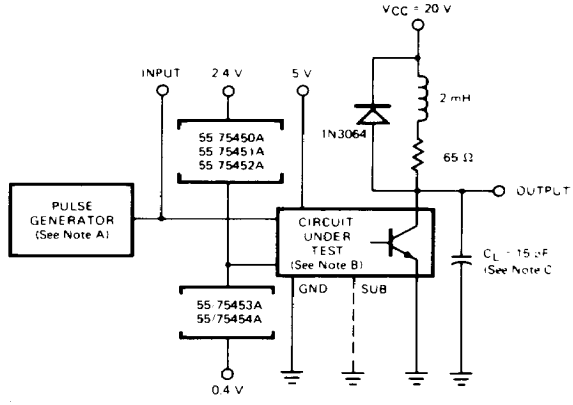
Fig. 14

CHARACTERISTICS MEASUREMENT INFORMATION

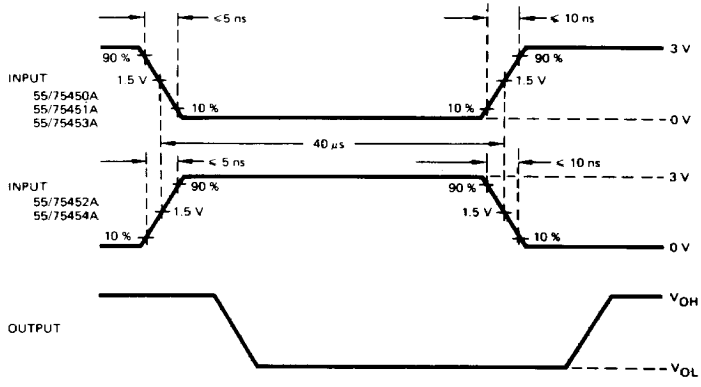
SWITCHING CHARACTERISTICS

LATCH-UP TEST OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS



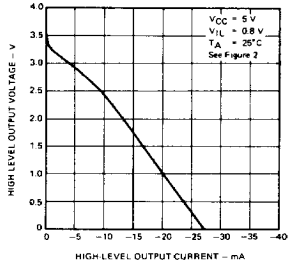
NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing 55450A or 75450A, connect output Y to transistor base with a 500 Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

Fig. 15

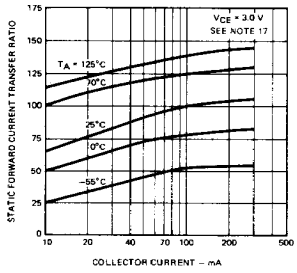
7

TYPICAL PERFORMANCE CURVES FOR 75450A SERIES

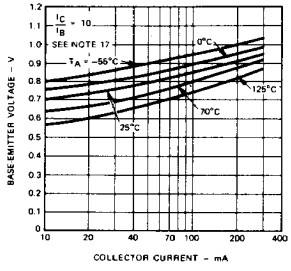
55450A/75450A TTL GATE HIGH-LEVEL OUTPUT VOLTAGE AS A FUNCTION OF HIGH-LEVEL OUTPUT CURRENT



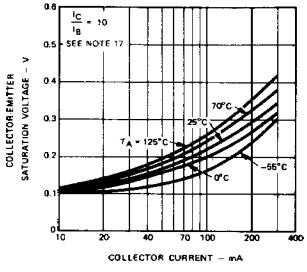
55450A/75450A TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT



55450A/75450A TRANSISTOR BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



NOTE 17: These parameters must be measured using pulse techniques. t_W = 300 μs, duty cycle ≤ 2%.