MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

LM139,A LM239,A, LM2901, LM339,A, MC3302

2

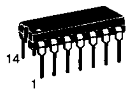
Quad Single Supply Comparators

These comparators are designed for use in level detection, low-level sensing and memory applications in consumer automotive and industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Low Input Offset Voltage: ±1.0 mV (Typ) LM139A Series
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation

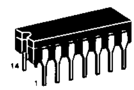
QUAD COMPARATORS

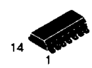
SILICON MONOLITHIC INTEGRATED CIRCUIT



N, P SUFFIX
PLASTIC PACKAGE
CASE 646

J, L SUFFIX
CERAMIC PACKAGE
CASE 632



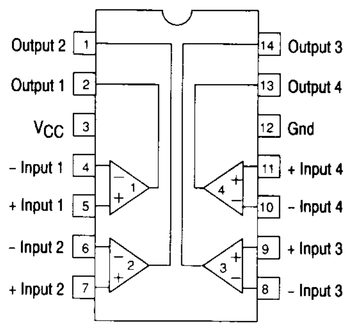


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

MAXIMUM RATINGS

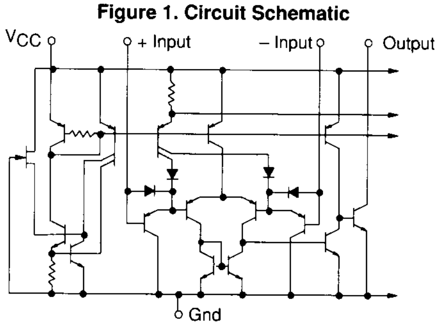
Rating	Symbol	Value	Unit
Power Supply Voltage LM139, A/LM239, A/LM339A/LM2901 MC3302	V_{CC}	 +36 or ±18 +30 or ±15	Vdc
Input Differential Voltage Range LM139, A/LM239, A/LM339, A/LM2901 MC3302	V_{IDR}	 36 30	Vdc
Input Common Mode Voltage Range	V_{ICMR}	–0.3 to V_{CC}	Vdc
Output Short Circuit to Ground (Note 1)	I_{SC}	Continuous	
Input Current (V_{in} < – 0.3 Vdc) (Note 2)	I_{in}	50	mA
Power Dissipation @ T_A = 25°C Ceramic Plastic Package Derate above 25°C	P_D	 1.0 8.0	 W mW/°C
Junction Temperature Ceramic & Metal Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range LM139, A LM239, A MC3302 LM2901 LM339, A	T_A	 –55 to +125 –25 to +85 –40 to +85 –40 to +105 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

PIN CONNECTIONS



(Top View)

Figure 1. Circuit Schematic



NOTE: Diagram shown is for 1 comparator.

ORDERING INFORMATION

Device	Temperature Range	Package
LM139J, AJ	–55° to +125°C	Ceramic DIP
LM239D, AD LM239J, AJ LM239N, AN	–25° to +85°C	SO-14 Ceramic DIP Plastic DIP
LM339D, AD LM339J, AJ LM339N, AN	0° to +70°C	SO-14 Ceramic DIP Plastic DIP
LM2901D LM2901N	–40° to +105°C	SO-14 Plastic DIP
MC3302L MC3302P	–40° to +85°C	Ceramic DIP Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = +25°C, unless otherwise noted)

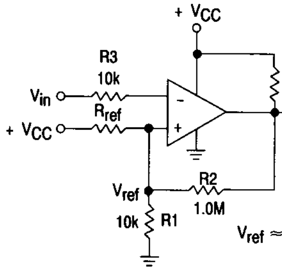
Characteristics	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	±1.0	±2.0	—	±1.0	±2.0	—	±2.0	±5.0	—	±2.0	±5.0	—	±2.0	±7.0	—	±3.0	±20	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	25	100	—	25	250	—	25	100	—	25	250	—	25	250	—	25	500	nA
Input Offset Current (Note 4)	I_{IO}	—	±3.0	±25	—	±5.0	±50	—	±3.0	±25	—	±5.0	±50	—	±5.0	±50	—	±3.0	±100	nA
Input Common Mode Voltage Range	V_{ICMR}	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	V
Supply Current R_L = ∞ (For All Comparators) R_L = ∞, V_{CC} = 30 Vdc	I_{CC}	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	mA
Voltage Gain $R_L \geq$ 15 kΩ, V_{CC} = 15 Vdc	A_{VOL}	50	200	—	50	200	—	—	200	—	—	200	—	25	100	—	2	30	—	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} = 1.4 Vdc, V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	—	—	300	—	—	300	—	—	300	—	—	300	—	—	300	—	—	300	—	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	µs
Output Sink Current $V_I(-) \geq$ +1.0 Vdc, $V_I(+)$ = 0, $V_O \leq$ 1.5 Vdc	I_{Sink}	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	mA
Saturation Voltage $V_I(-) \geq$ +1.0 Vdc, $V_I(+)$ = 0, $I_{sink} \leq$ 4.0 mA	V_{sat}	—	130	400	—	130	400	—	130	400	—	130	400	—	130	400	—	130	500	mV
Output Leakage Current $V_I(+) \geq$ +1.0 Vdc, $V_I(-)$ = 0, V_O = +5.0 Vdc	I_{OL}	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	nA

PERFORMANCE CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = T_{low} to T_{high} [Note 3])

Characteristic	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	—	±4.0	—	—	±4.0	—	—	±9.0	—	—	±9.0	—	—	±15	—	—	±40	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	—	300	—	—	400	—	—	300	—	—	400	—	—	500	—	—	1000	nA
Input Offset Current (Note 4)	I_{IO}	—	—	±100	—	—	±150	—	—	±100	—	—	±150	—	—	±200	—	—	±300	nA
Input Common Mode Voltage Range	V_{ICMR}	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	V
Saturation Voltage $V_I(-) \geq$ +1.0 Vdc, $V_I(+)$ = 0, $I_{sink} \leq$ 4.0 mA	V_{sat}	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	mV
Output Leakage Current $V_I(+) \geq$ +1.0 Vdc, $V_I(-)$ = 0, V_O = 30 Vdc	I_{OL}	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	µA
Differential Input Voltage All $V_I \geq$ 0 Vdc	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	Vdc

NOTES:
1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collectorbase junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when the inputs become ≥ ground or negative supply.
3. (LM139/139A) T_{low} = −55°C, T_{high} = +125°C; (LM339/339A) T_{low} = 0°C, T_{high} = +70°C
   (LM239/239A) T_{low} = −25°C, T_{high} = +85°C; (MC3302) T_{low} = −40°C, T_{high} = +85°C
   (LM2901) T_{low} = −40°C, T_{high} = +105°C
4. At the output switch point, $V_O \simeq$ 1.4 Vdc, $R_S \leq$ 100 Ω 5.0 Vdc ≤ $V_{CC} \leq$ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} −1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

Figure 2. Inverting Comparator with Hysteresis



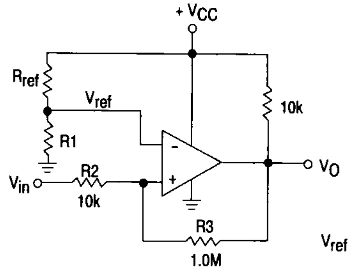
$$V_{ref} \approx \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R3 \approx R1\,//\,R_{ref}\,//\,R2$$

$$V_H = \frac{R1\,//\,R_{ref}}{R1//\,R_{ref} + R2}\,[V_{O(max)} - V_{O(min)}]$$

$$R2 \gg R_{ref}\,//\,R1$$

Figure 3. Noninverting Comparator with Hysteresis



$$V_{ref} = \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R2 \approx R1\,//\,R_{ref}$$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3}\,[(V_{O(max)} - V_{O(min)}]$$

Typical Characteristics

(V_{CC} = 1.5 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Figure 4. Normalized Input Offset Voltage

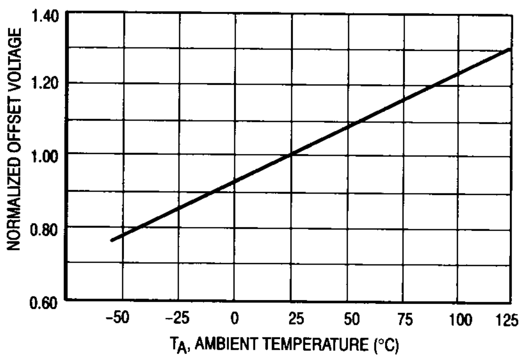


Figure 5. Input Bias Current

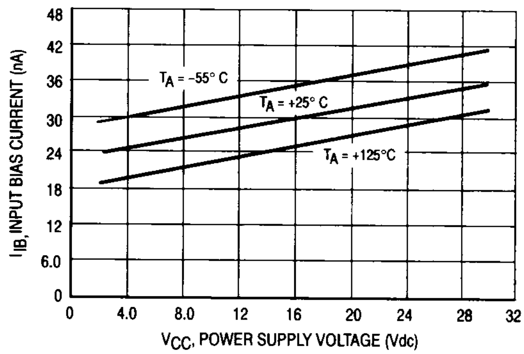


Figure 6. Output Sink Current versus Output Saturation Voltage

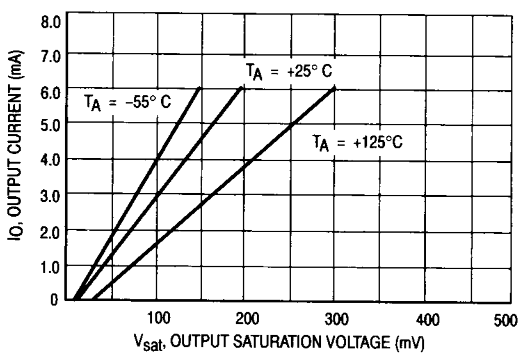
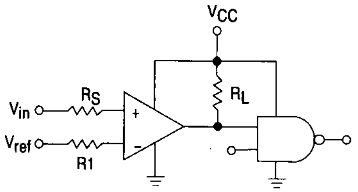


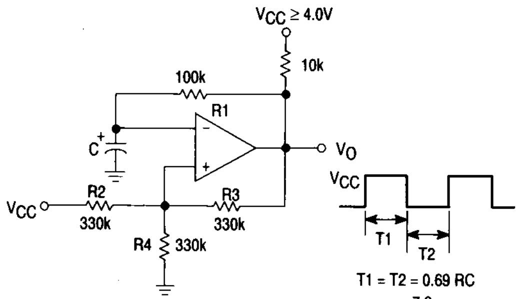
Figure 7. Driving Logic



R_S = Source Resistance
$R1 \approx R_S$

Logic	Device	V_{CC} (V)	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Figure 8. Squarewave Oscillator



$T1 = T2 = 0.69\ RC$

$f \approx \frac{7.2}{C(\mu F)}$

$R2 = R3 = R4$

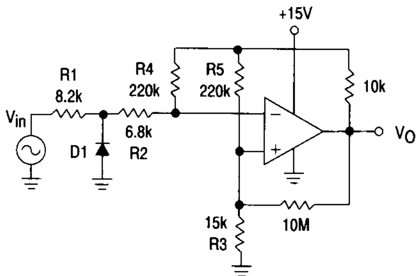
$R1 \approx R2 \,//\, R3 \,//\, R4$

APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than –300 mV should not be used.

Figure 9. Zero Crossing Detector (Single Supply)



D1 prevents input from going negative by more than 0.6 V.

$R1 + R2 = R3$

$R3 \le \frac{R5}{10}$ for small error in zero crossing

Figure 10. Zero Crossing Detector (Split Supplies)

$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion ($\Delta\Theta$).