PROGRAMMABLE INTERVAL TIMER

TMP82C54P-2 / TMP82C54M-2

The TMP82C54P-2 TMP82C54M-2 (hereafter called the TMP82C54) is a low power, CMOS general-purpose programmable timer/counter.

The TMP82C54 consists of 3 independent 16-bit counters to implement high-speed counting. It contributes to a greatly enhanced system throughput.

1. FEATURES

(1) Pin compatible with the TMP82C53P-2 (TMP82C54P-2)

(2) Three independent, 16-bit counters

(3) Count data read is available.

(4) Status read is available.

(5) Six programmable Counter modes

(6) Binary/decimal count selection

(7) High-speed operation
TMP82C54P-2/M-2 Clock input = 10MHz Max.

(8) Low power dissipation
In operation 30mA max.
In stand-by 10μA max.

(9) Extended operating temperature
$-40°C$ to $+85°C$

(10) Power supply voltage
$5V \pm 10\%$

2. PIN CONNECTIONS (TOP VIEW)

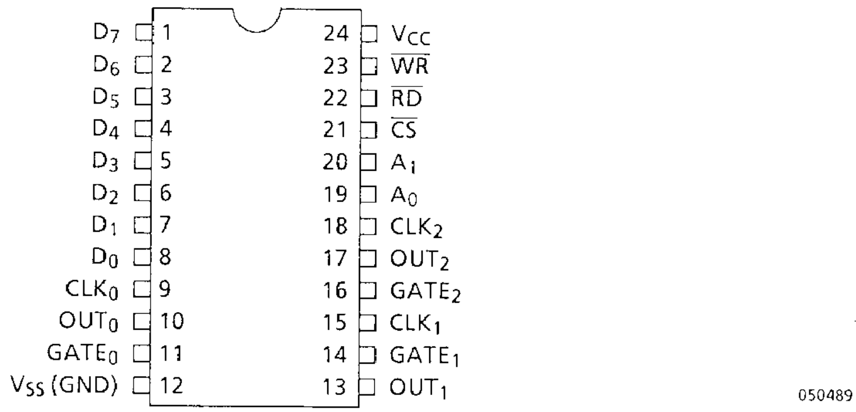

Figure 2.1 Pin Connections

3. BLOCK DIAGRAM

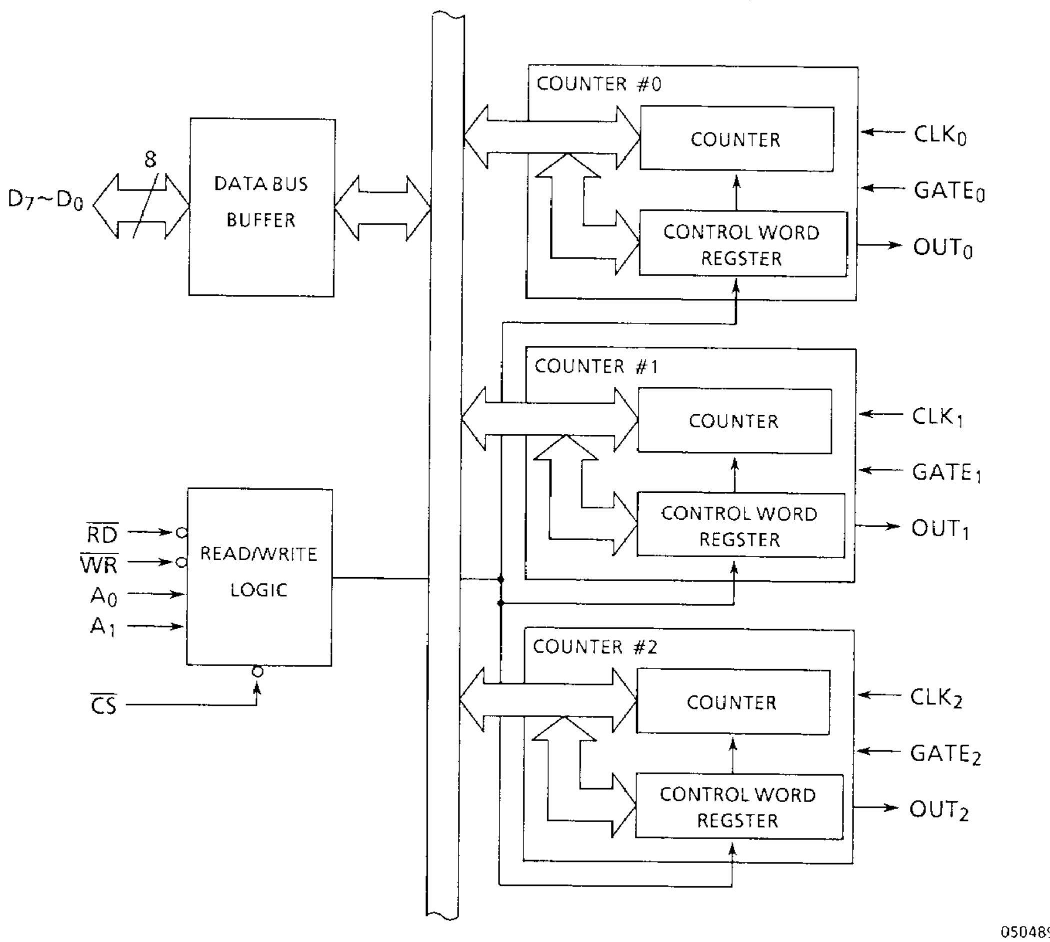

Figure 3.1 Block Diagram

4. I/O SIGNAL DESCRIPTION

- $\overline{CS}$ (Chip Select input)

  A low this input enables the TMP82C54. Unless $\overline{CS}$ is in the enabled state, the read/write operation is ignored. The $\overline{CS}$ input does not affect the actual counter operation.

- A_0, A_1 (Address inputs)

  These inputs are used to select one of the 3 internal counters or the control word register.

- $\overline{WR}$ (Write input)

  The low active write strobe signal for the TMP82C54 used, to set the mode or load data into the counters.

- $\overline{RD}$ (Read input)

  The low active read strobe signal for the TMP82C54 used, to read the value of the internal counter.

- $D_0 - D_7$ (Data bus I/O)

  The 8-bit bidirectional 3-state data bus pins connected to the microcomputer data bus.

- CLK $_{0\sim3}$ (Clock input)

  The clock input pin for the counter. The counter starts decrementing at the falling edge of this signal.

- GATE $_{0\sim3}$ (Gate input)

  The gate input pin for the counter. The function depends on the mode stored in the control word register.

- OUT $_{0\sim3}$ (Out output)

  The output pin form the counter. One of 6 different waveforms selected by the mode stored in the control word register is output.

5. OPERATIONAL DESCRIPTION

5.1 DATA BUS BUFFER

This is the bidirectional 3-state 8-bit data buffer to interface with the microcomputer system data bus. The transfer of the control word for mode set, data write to the counter, and data read from the counter are all performed through this buffer.

5.2 READ/WRITE LOGIC

This circuit receives the control signals ($\overline{RD}$, $\overline{WR}$) form the system bus to generate the control signals for the entire TMP82C54 system operations.

The chip select input ($\overline{CS}$) enables/desables these control signals. When the $\overline{CS}$ is in the disabled state, the control signal states do not affect the internal operations.

5.3 CONTROL WORD REGISTER

The control word register is selected when $A_0=1$ and $A_1=1$.

The information from the data bus buffer is stored in this register to select the counter operation mode, binary or decimal counting, and control the specification of the counter loading method. The control word can be read by using the read-back command.

5.4 COUNTERS #0-#2

These counters perform exactly the same operation independently.

The following description is made referring to only one counter for convenience. Figure 5.1 shows the block diagram of the counter.

The counter is the 16-bit presettable synchronous down-counter.

The status register, consisting of 8 bits, holds the current states of the control word register, output pin, and the null count flag information. (See "Read-back Command.")

The count latch, consisting of two 8 bits, normally follows the current value of the down-counter (non latch state). When the TMP82C54 receives an proper count latch command, the count latch holds the value of the down-counter at this time. When the latched data is read by the MPU, the latch is cleared and put in the non latch state again. After the count latch command, count value to be read is not the current value of the down-counter but the value of the count latch.

The count register consists of two 8 bits. When the count value is written to the counter, at first, the value is loaded into the counter register. Then the count value is loaded into the down-counter. Writing the count value to the count register is performed in units of 8 bits.

However, the count value is loaded into the down-counter in units of 16 bits.

When the counter value is written to the down-counter programmed in the read/load 1-byte mode, the other byte is automatically cleared to 00H.

The control logic is connected to the CLK input, GATE input, and OUT output signals. The operations of these signals specified by selecting one of modes 0-5 programmed in the control word register.

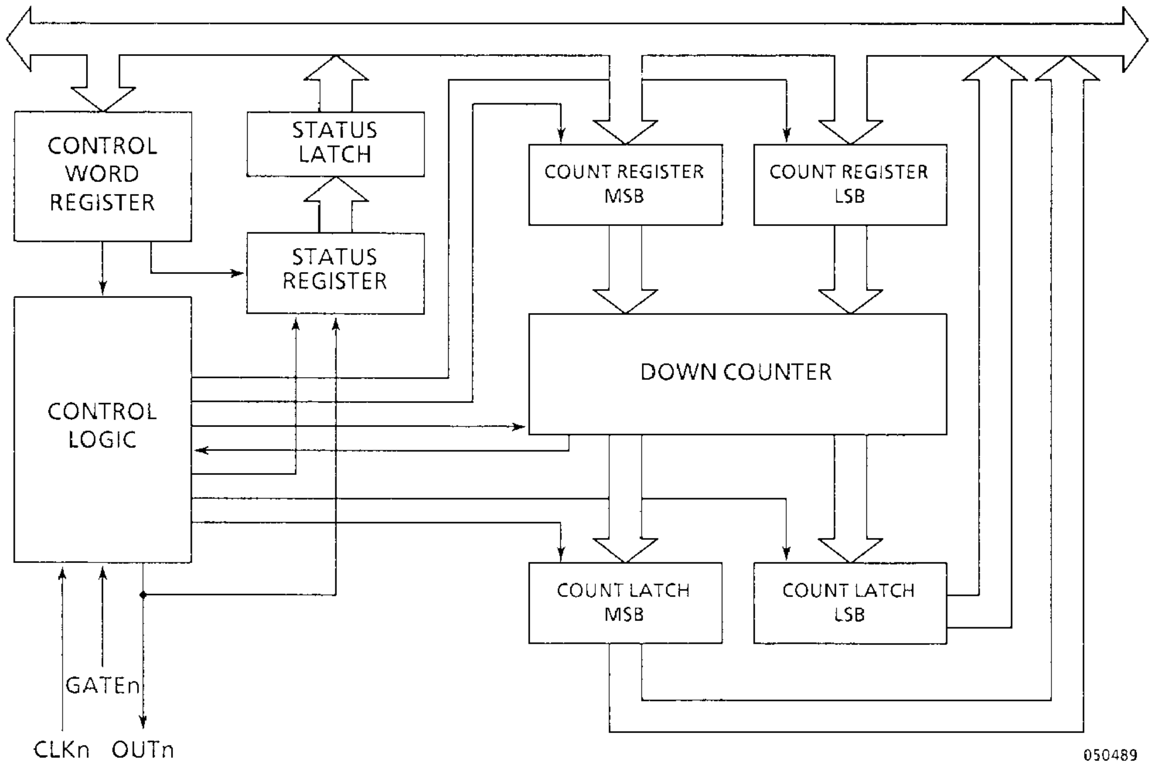

Figure 5.1 Block Diagram of Internal Counter

6. PROGRAMMING

The OUT output pin state, the counter mode, and the count register values of the TMP82C54 are still undefined immediately after the power is turned on.

This requires to program the counters to be used. However, the counters not to be used need not be programmed.

6.1 MODE SETTING

The count modes of the TMP82C54 can be set with a simple I/O instruction. Each counter of TMP82C54 can be programmed separately by writing the control word to the control word register ($\overline{CS}=0, A_0=1, A_1=1, \overline{WR}=0$).

6.1.1 Control Word

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC_1	SC_0	RW_1	RW_0	M_2	M_1	M_0	BCD

	SC_1	SC_0
Select Counter 0	0	0
Select Counter 1	0	1
Select Counter 2	1	0
Read Back Command	1	1

	RW_1	RW_0
Counter Latch Command	0	0
READ/LOAD LSB	0	1
READ/LOAD MSB	1	0
READ/LOAD LSB → MSB	1	1

M_2	M_1	M_0	
0	0	0	Mode 0
0	0	1	Mode 1
×	1	0	Mode 2
×	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD	
0	Binary Counter 16 bits
1	BCD Counter (4 Decades)

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Note : 1. Read/Load least significant byte first, then most significant byte
2. Read/Load is $\overline{RD}/\overline{WR}$
3. × : Don't care

Figure 6.1 Control Word

There is no specified order in which the counters are selected for mode setting. Mode setting can start from any counter.

6.2 COUNTER WRITING

Paying attention to the following two points makes it possible to program the TMP82C54 in any sequence.

(1) Writing of the control word to each counter must be performed before the count value is written.

(2) The count value must be written in the format specified in the control word (bits RW_0 and RW_1).

6.3 PROGRAM SEQUENCE EXAMPLES (IN THE LSB-MSB 2-BYTE MODE)

(1) Counter 0: Control word
Counter 0: Lower 8 bits
Counter 0: Upper 8 bits
Counter 1: Control word
Counter 1: Lower 8 bits
Counter 1: Upper 8 bits
Counter 2: Control word
Counter 2: Lower 8 bits
Counter 2: Upper 8 bits

(2) Counter 0: Control word
Counter 1: Control word
Counter 2: Control word
Counter 0: Lower 8 bits
Counter 1: Lower 8 bits
Counter 2: Lower 8 bits
Counter 0: Upper 8 bits
Counter 1: Upper 8 bits
Counter 2: Upper 8 bits

(3) Counter 0: Control word
Counter 1: Control word
Counter 2: Control word
Counter 0: Lower 8 bits
Counter 0: Upper 8 bits
Counter 1: Lower 8 bits
Counter 1: Upper 8 bits
Counter 2: Lower 8 bits
Counter 2: Upper 8 bits

(4) Counter 0: Control word
Counter 0: Lower 8 bits
Counter 1: Control word
Counter 2: Control word
Counter 1: Lower 8 bits
Counter 0: Upper 8 bits
Counter 1: Upper 8 bits
Counter 2: Lower 8 bits
Counter 2: Upper 8 bits

6.4 COUNTER READING

The counter value of the TMP82C54 can be read without disturbing the on-going count value. The counter value are read in one of the three methods as described below.

- One is simple I/O Read of the counter selected by A_0 and A_1. In this method, the GATE input must be controlled or the CLK input must be inhibited in order to read a stable count value. The procedure specified in the control word must always be followed. (That is, only the LSB 1 byte must be RW_1/RW_0 read when only the LSB 1 byte is specified; only the MSB 1 byte must be read when only the MSB 1 byte is selected; and, in the case of the continuous bytes form LSB to MSB, the LSB 1 byte and MSB 1 byte (a total of 2 bytes) must be read.)
- The on-going, momentary count value is read without stopping the counter operation. This can be achieved by specifying the counter latch operation in the control word (the counter latch command).
  When reading the value of the specified counter, a stable count value can be obtained by specifying the counter latch operation before reading the value of the specified counter. In this case, the procedure specified in the control word must be followed like the method shown above.
- The count latch is specified be the Read-Back command.

6.4.1 Counter Latch Command

$\overline{CS} = 0$, $A_0 = A_1 = 1$, $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC_1	SC_0	0	0	×	×	×	×

SC_1	SC_0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read Back Command

× : Don't Care

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Figure 6.2 Counter Latch Command

The selected counter holds the value of the down-counter when the counter latch command is executed. The count value remains held until the value is read or the counter is reprogrammed.

If the counter latch command is written to the same counter twice, the second one is ignored. The value to be read is the counter value counted at the time the first count latch command was written.

When the counter is in the 2-byte mode, the 2 bytes must be read.

The count value can be written as the following sequence :

1. Least significant byte: Read
2. Least significant byte: Write
3. Most significant byte : Read
4. Most significant byte : Write

6.4.2 Read-back Command

The read-back command is used to get the count value, the mode output pin state, and the null count flag information.

$\overline{CS} = 0$, $A0 = A1 = 1$, $\overline{WR} = 0$

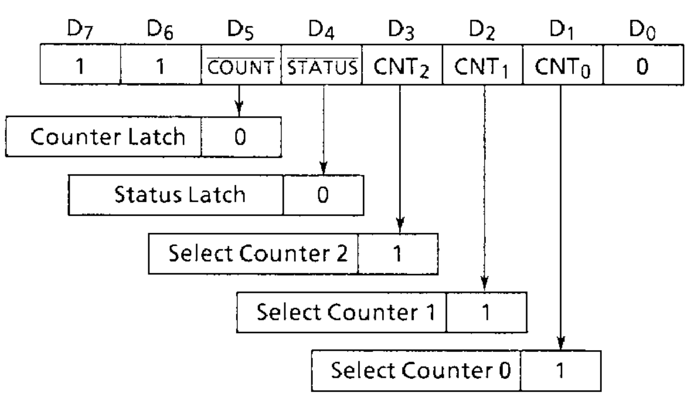

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Figure 6.3 Read-Back Command

The read-back command can latch multiple counters simultaneously by selecting the counter by CNT_2-CNT_0 with the $\overline{COUNT}$ bit $D_5=0$ (multiple count latch). This will provide the same operation on each command as the operation in which a count latch command has been merely written to each counter. The count value remains held in the count latch until the value is read or the counter is reprogrammed.

Reading the count value from any counter does not clear the counter latch of the other counters.

When multiple count latch is performed on a counter twice, the second one is ignored. The value to be read is the counter value counted at the time the first multiple count latch was performed.

The read-back command can latch the status information by selecting a counter by CNT_2-CNT_0 with the STATUS bit $D_4=0$. The status information are as follows.

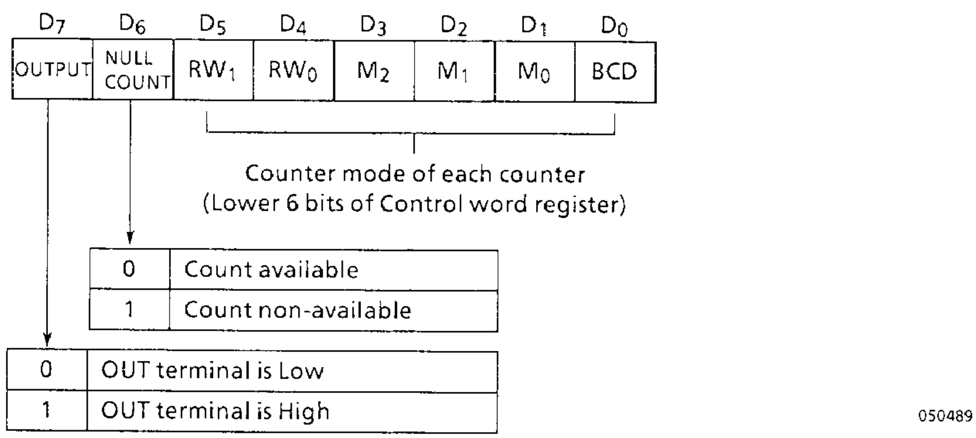

Figure 6.4 Status Data Format

Bits D_5-D_0 are the low-order 6 bits of the control word register currently programmed in that counter. These bits are held in the status register when the mode is set in the control word register and remain unchanged until the control word register is rewritten.

OUTPUT bit D_7 indicates the current OUT output pin state.

NULL COUNT bit D_6 is the flag indicating whether the count value has been loaded from the count register into the down-counter. When this flag is "0", it indicates that the count value has been loaded into the down-counter; when it is "1", it indicates that the count value has not been loaded. The following shows the NULL COUNT flag changes.

1. Write to the control word register NULL COUNT=1
2. Write a count value to the count register (Note): NULL COUNT=1
3. Load from the count register into the down-counter: NULL COUNT=0

Note : When the 2-byte mode is specified by the control word register, the NULL COUNT flag goes "1" upon writing the second byte.

The status latch is held until the status is read or the counter is reprogrammed. When the status latch is specified by the read-back command on a counter twice, the second one is ignored. The data to be read is the data present at the time the first status latch was performed.

The multiple count latch and status latch by the read-back command can be performed simultaneously by setting the $\overline{\text{COUNT}}$ and $\overline{\text{STATUS}}$ bits D_5 and D_4 to "0". This performs the same operation as the one in which multiple count latch and status latch are performed separately. Like the simultaneous latch, each latch in this case is held until it is read or the counter is reprogrammed.

If the multiple latch and status latch are performed on a counter twice, the second ones are ignored. The following shows a read-back command programming example.

Table 6.1 Read-back command programming example

Read back command	Counter 0 latch		Counter 1 latch		Counter 2 latch	
	Count	Status	Count	Status	Count	Status
Initial State	non	non	non	non	non	non
Counter 1 Status Latch	non	non	non	latch	non	non
Counter 2 Count & Status Latch	non	non	non	latch	latch	latch
Counter 0, 2 Status Latch	non	latch	non	latch	latch	ignore
Counter 0 Count Latch	latch	latch	non	latch	latch	latch
Counter 0 Status Count Read	non	non	non	latch	latch	latch
Counter 1 Count & Status Latch	non	non	latch	ignore	latch	latch
Counter 0, 2 Count & State Latch	latch	latch	latch	latch	ignore	ignore

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When both multiple count latch and status latch are performed by the read-back command, the status data is read in the first read of the counter regardless of the latch execution sequence. The value of the latched count register is read in the reading of the next 1 or 2 bytes (depending on the counter mode setting)

Table 6.2 Read/Write Addressing

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	Function
0	1	0	0	0	Write Counter 0
0	1	0	0	1	Write Counter 1
0	1	0	1	0	Write Counter 2
0	1	0	1	1	Write Control word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	
1	×	×	×	×	Non Operation (3 – State)
0	1	1	×	×	

× : Don't Care

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7. MODE DESCRIPTION

The TMP82C54 has the 6 count modes.
Each count mode has the following characteristics.

- When the control word is written, the output is initialized to the state unique to each mode.
- The GATE is sampled at each rising edge of CLK. In modes 0 and 4, the GATE operates by level sense; in modes 1 and 5, it operates by rising-edge sense; and in modes 2 and 3, it operates by level sense and rising-edge sense respectively.
- The down-counter performs count loading and decrement at the falling edge of CLK.
- The maximum counter value is 0. (2^{16} in binary, 10^4 in decimal)
- The counter keeps decrementing until 0 (terminal count) is reached.
- In modes 0, 1, 4, and 5, count continues even if the count value reaches 0. In modes 2 and 3, the initial value is reloaded upon reaching the terminal count for repeated counting.

Terminology

Clock pulse	:	From the rising edge to falling edge of CLK input.
Trigger	:	The rising edge of the GATE input.
Count loading	:	Loading of count value from the count register into the down-counter.
Mode setting	:	Writing of the control word.
Terminal count	:	Reaching of the down-counter to 0.

The following sample waveform of each mode shows the binary count and read/write LSB programming case. The numbers indicate down-counter values.

7.1 MODE 0: INTERRUPT ON TERMINAL COUNT

The output is initialized to the low level after setting the mode . The output remains low after count loading. When the GATE input is high, the down-counter starts counting.

When the terminal count has been reached, the output goes high, which is held until a new count value is written or another mode is set.

The GATE input only controls the down-counter operation: it does not affect the output state.

The count value is loaded to the counter by the clock pulse following the writing of the count value to the count register.

The down-counter continues counting after the terminal count has been reached.

Rewriting to the count register during counting will cause the following actions.

1. When the first byte is written, the current count is suspended. The output is set to the low level.
2. When the second byte is written, count starts with the next clock pulse upon which the now counting starts.

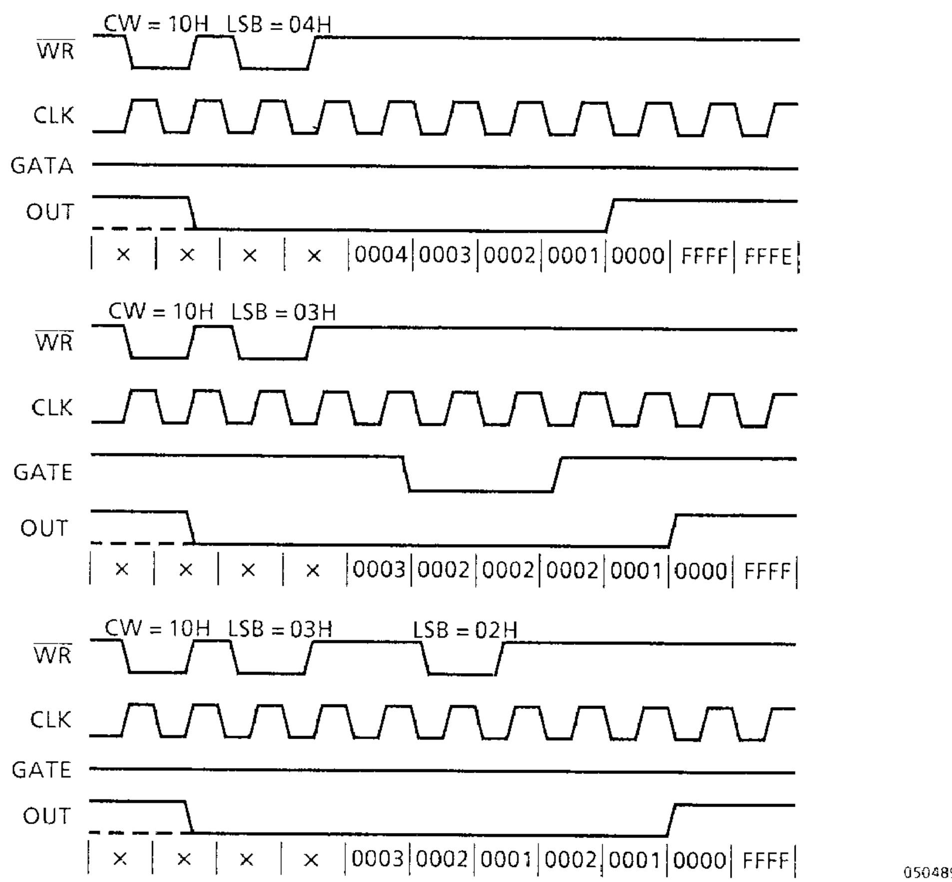

Figure 7.1 Mode 0

7.2 MODE 1: PROGRAMMABLE ONE-SHOT

The output is initialized to the high level after setting this mode and is reset to the low level by the clock pulse following the trigger. Then, the output goes high after the terminal count has been reached. The counter performs the following operations with the trigger:

1. Loading
2. Setting the output to the low level (reset)
3. Start counting

The one-shot pulse of GATE can be retriggered. Therefore, the output remians low until complete counting is made after triggering.

When a new count value is written while the output is low, the width of the one-shot pulse already output is not affected upon the next trigger.

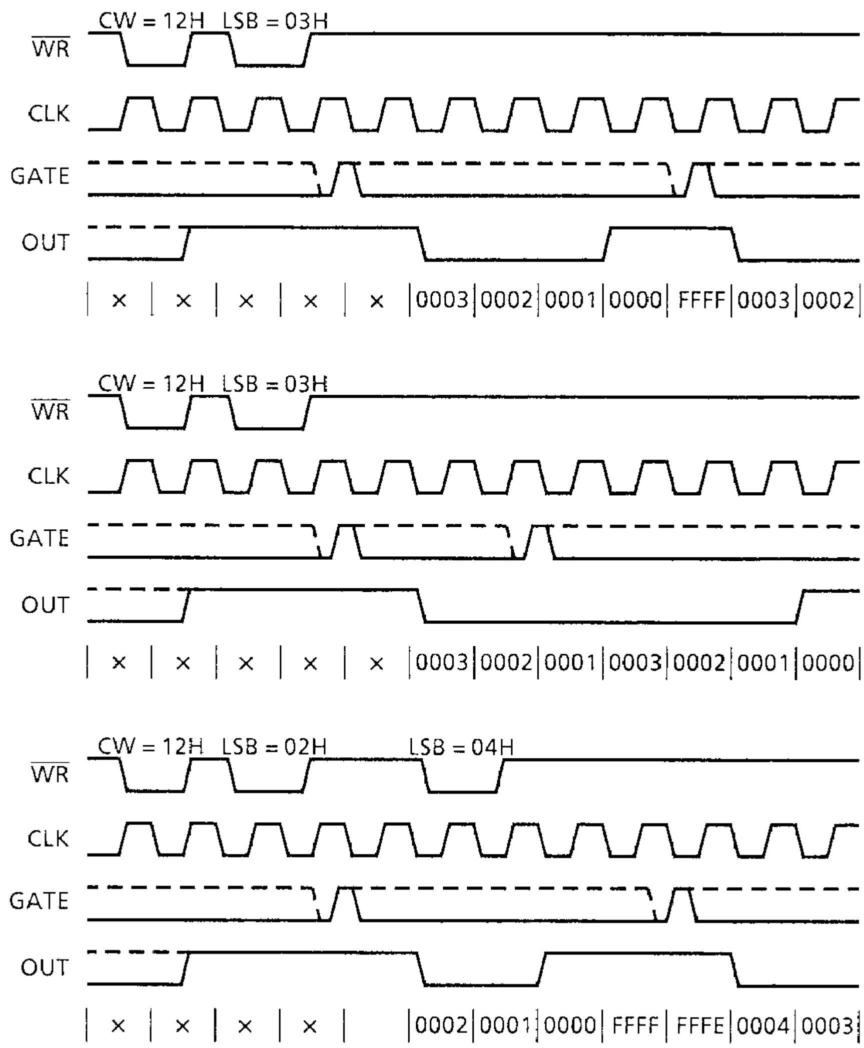

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Figure 7.2 Mode1

7.3 MODE 2: RATE GENERATOR

Division-by-N counter is performed.

The output is initialized to the high level after setting this mode, and goes low for 1 clock pulse when the counter has reached 1. Then, the output goes high again and the initial count is loaded for infinite counting.

When the GATE = 1, counting is enabled. When the GATE = 0, counting is disabled and the output is set to the high level. By the trigger, the initial value is loaded into the counter at the next clock pulse, starting new counting. Thus, the gate input can be used for counter synchronization. When mode 2 is set, the output goes high, which is held until count loading is performed, so that synchronization can be provided by software as well.

Rewriting to the count register being counted does not affect the current cycle. A new cycle starts after the end of the current cycle.

The minimum count of this mode is 2.

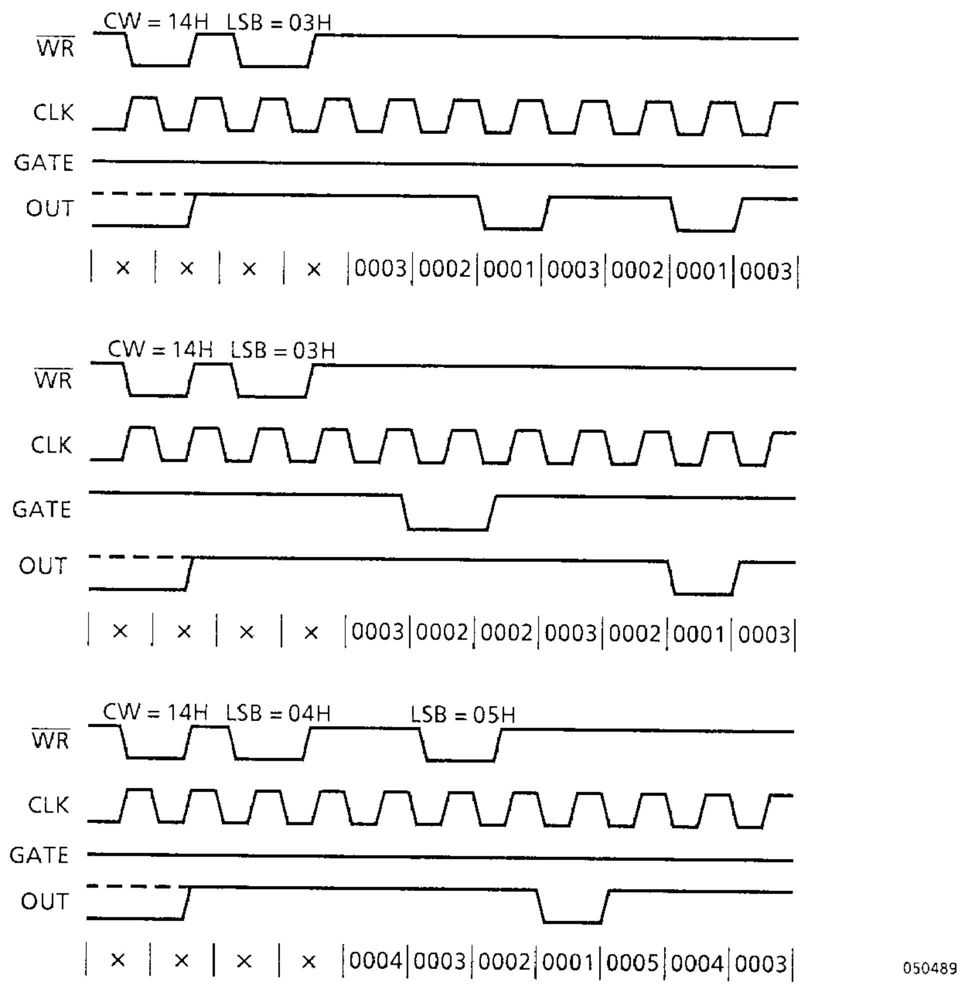

Figure 7.3 Mode 2

7.4 MODE 3: SQUARE WAVE RATE GENERATOR

The output is initialized to the high level after setting this mode. The half of the count setting value (even number) becomes high and the other half becomes low. The rest is the same as mode 2.

When the GATE = 1, counting is enabled. When the GATE = 0, counting is disabled and the output is set to the high level.

When the count setting value is an even number, counting is performed by decrementing the counter by 2 at the falling edge of the clock input.

When the terminal count has been reached, the output is inverted, the count setting value is reloaded into the counter, the counter is decremented by 2, this process is repeated.

If the count value is an odd number and its output is high, the value which is the setting value - 1 is loaded into the down-counter, which is decremented by 2. The output goes low at the clock pulse following the terminal count and the setting value - 1 is loaded into the down-counter again. Then, the count has been reached, this process is repeated.

Thus, when the count value is odd, the output is high for (N + 1)/2 and low for (N − 1)/2.

The minimum count of this mode is 2.

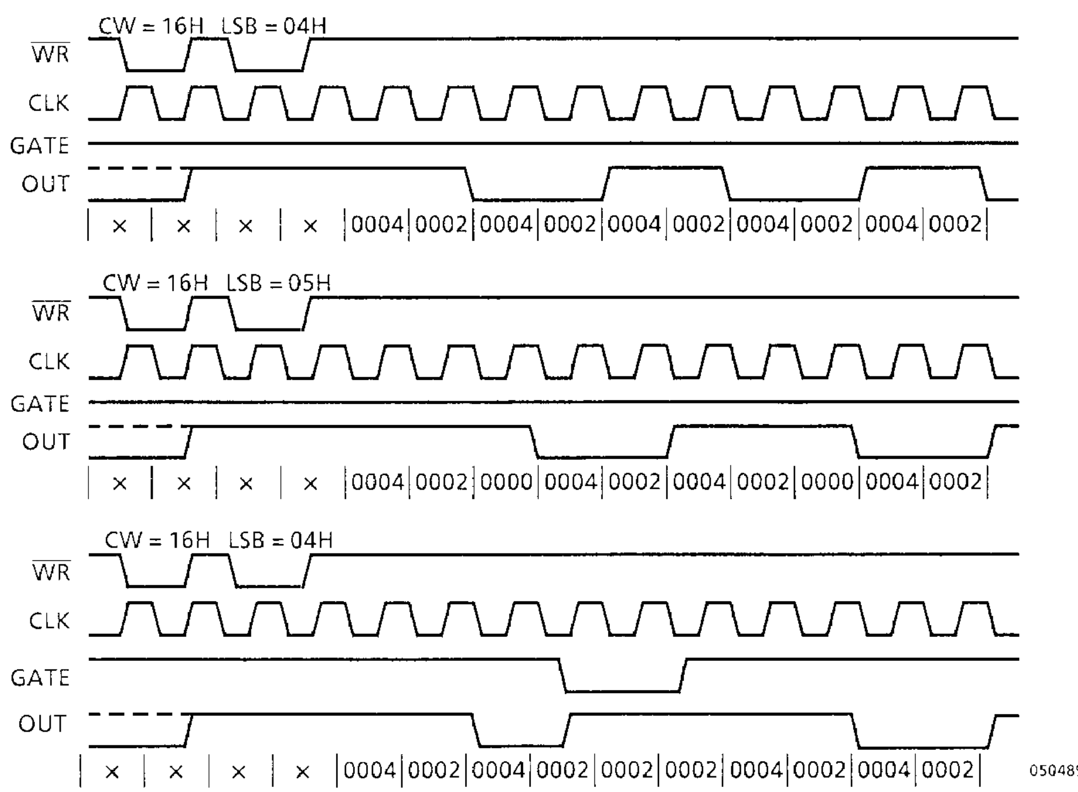

Figure 7.4 Mode 3

7.5 MODE 4: SOFTWARE-TRIGGERED STROBE

The output goes high after setting this mode. When the count value is loaded into the down counter and the GATE input is high, the down-counter starts counting.

When the terminal count has been reached, the output goes low for 1 clock pulse.

When GATE=0, counting is disabled. When GATE=1, counting is enabled. The GATE input dose not affect the output.

When the count value is written to the count register after setting the mode, count loading is performed with the next clock pulse.

When a new count value is written during counting, loading is performed with the following clock pulse and the counting continues with the new count value.

In the 2-byte mode, the following actions take place.

1. Writing of the first byte does not affect the counting.
2. With the clock pulse following the writing of the second byte, count loading starts.

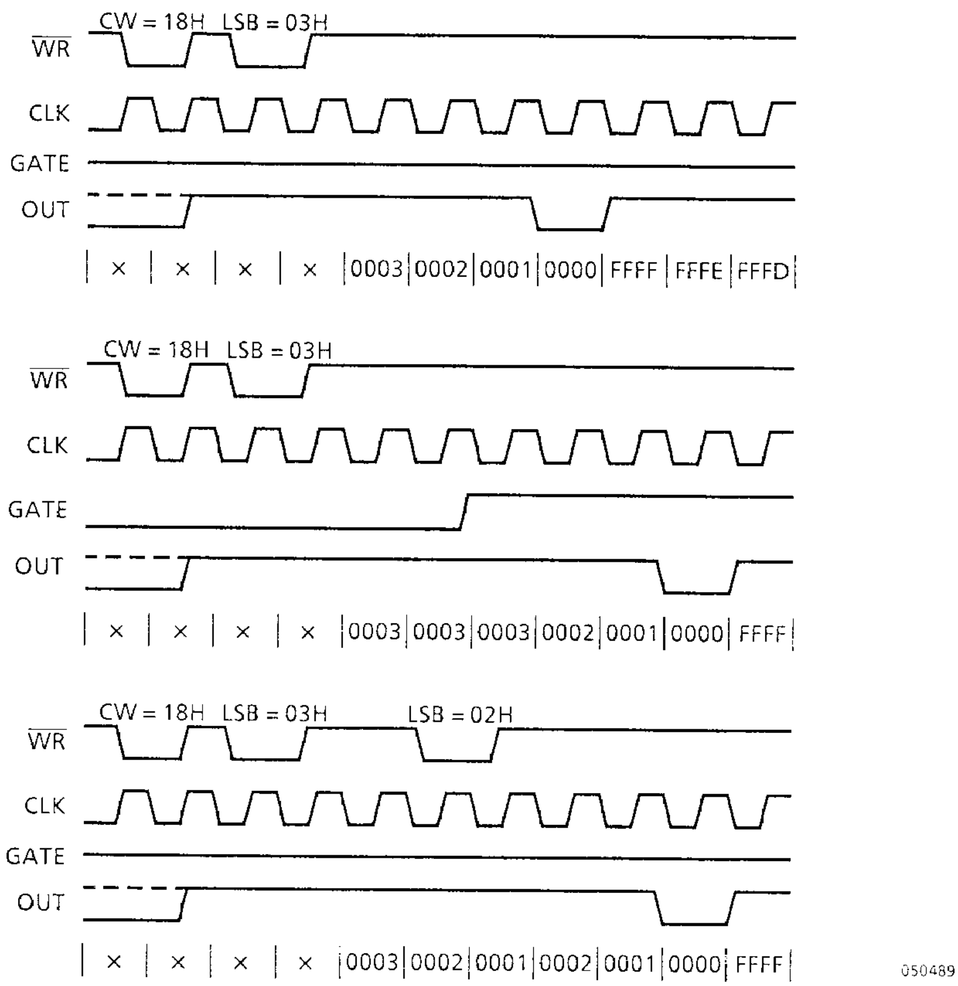

Figure 7.5 Mode 4

7.6 MODE 5: HARDWARE-TRIGGERED STROBE

The output is initialized to the high level after setting this mode. The counter starts counting after the GATE input is triggered. When the terminal count has been reached, the output goes low for 1 clock pulse.

Count loading starts with the clock pulse following the trigger after the mode is set and the count value is written.

The counter can be re-triggered.

The output remains high until a complete count is mode after triggering any GATE input.

If a new count value is written to the count register during counting, the current counting continues. If a trigger is encountered, the new count value is loaded with the following clock pulse and counting starts with the new count value.

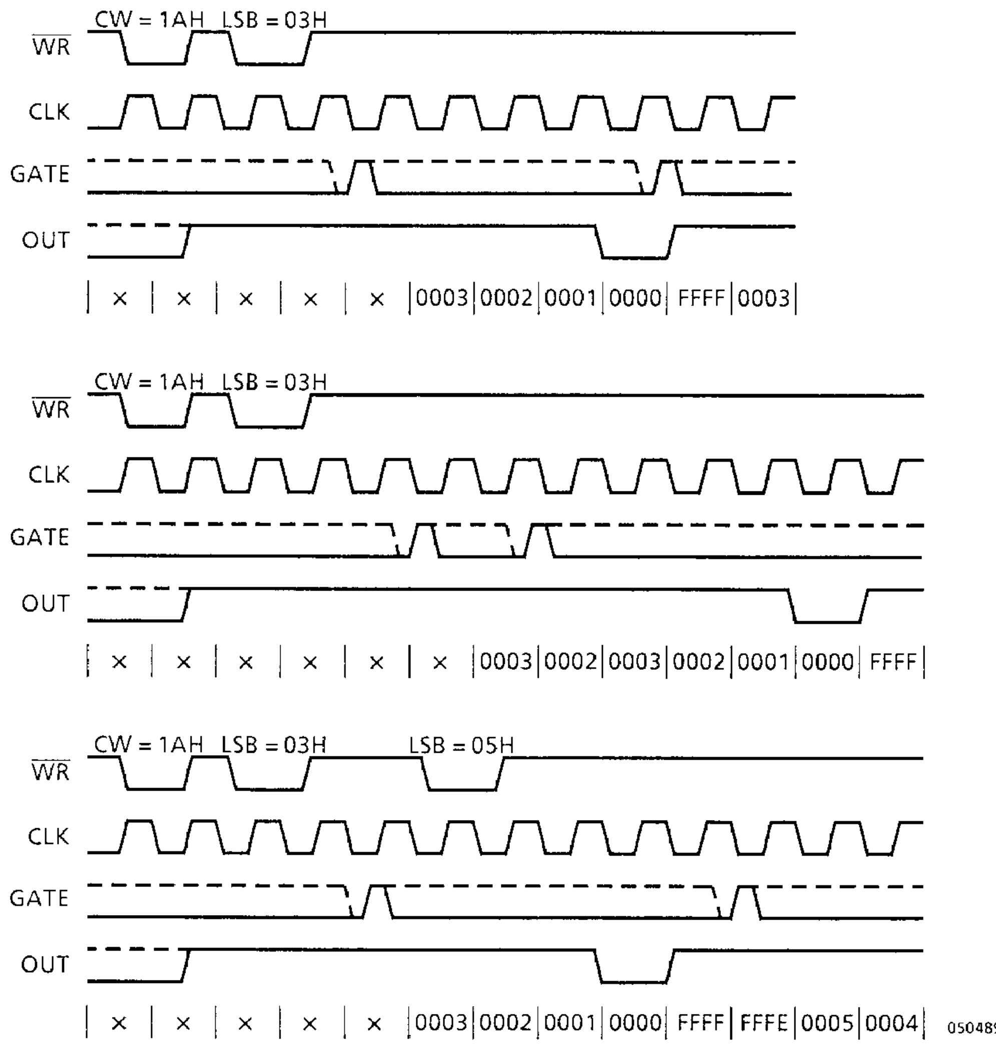

Figure 7.6 Mode 5

Table 7.1 Gate Input Operations

Status Modes	Low or Going Low	Rising	High
0	Disables counting	–	Enable counting
1	–	(1) Initiates counting (2) Resets output after next clock	–
2	(1) Disables counting (2) Sets output immediately High	Initiates counting	Enable counting
3	(1) Disables counting (2) Sets output immediately High	Initiates counting	Enable counting
4	Disables counting	–	Enable counting
5	–	Initiates counting	–

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Table 7.2 Minimum and Maximum Count Values

Mode	Min count	Max count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

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8. ELECTRIC CHARACTERISTICS

8.1 MAXIMUM RATINGS

SYMBOL	ITEMS	TEST CONDITION	RATING	UNIT
V_{CC}	Suply Voltage	With Respect To GND.	$-0.5 \sim +7.0$	V
V_{IN}	Input Voltage		$-0.5 \sim V_{CC}+0.5$	V
V_{OUT}	Output Voltage		$-0.5 \sim V_{CC}+0.5$	V
P_D	Power Dissipation		250	mW
T_{sol}	Solder Temperature		260 (10sec)	℃
T_{stg}	Storage Temperature		$-65 \sim +150$	℃
T_{opr}	Operating Temperature		$-40 \sim +85$	℃

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8.2 DC CHARACTERISTICS (TA = −40 to +85°C, VCC = 5V ± 10%, VSS (GND) = 0V)

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		−0.5	−	0.8	V
V_{IH}	Input High Voltage		2.2	−	$V_{CC}+0.5$	V
V_{OL}	Output Low Voltage	$I_{OL}=2.2mA$	−	−	0.45	V
V_{OH1}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	−	−	V
V_{OH2}	Output HIgh Voltage	$I_{OH}=-100\mu A$	$V_{CC}-0.8$	−	−	V
I_{IL}	Input Leak Current	$0V \leqq V_{IN} \leqq V_{CC}$	−	−	±10	μA
I_{OFL}	Output Leakage Current	$0.45V \leqq V_{OUT} \leqq V_{CC}$	−	−	±10	μA
I_{CC1}	Operating Supply Current	CLK = 10MHz $V_{IH}=V_{CC}-0.2V$ $V_{IL}=0.2V$	−	−	30	mA
I_{CC2}	Stand-by Supply Current	CLK = DC $V_{IH}=V_{CC}-0.2V$ $V_{IL}=0.2V$	−	−	10	μA

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8.3 AC CHARACTERISTICS (TA = − 40 to + 85°C, VCC = 5V ± 10%, VSS(GND) = 0V)

8.3.1 Read/Write

SYMBOL	ITEM	P-2/M-2 MIN.	P-2/M-2 MAX.	UNIT
t_{AR}	Address Set-up Time ($\overline{RD}$)	30	–	ns
t_{SR}	$\overline{CS}$ Set-up Time ($\overline{RD}$)	0	–	ns
t_{RA}	Address Hold Time ($\overline{RD}$)	20	–	ns
t_{RR}	$\overline{RD}$ Pulse Width	95	–	ns
t_{RD}	Valid Data ($\overline{RD}$)	–	85	ns
t_{AD}	Valid Data (Address)	–	185	ns
t_{DF}	Data Floating ($\overline{RD}$)	5	65	ns
t_{AW}	Address Set-up Time ($\overline{WR}$)	0	–	ns
t_{SW}	$\overline{CS}$ Set-up Time ($\overline{WR}$)	0	–	ns
t_{WA}	Address Hold Time ($\overline{WR}$)	0	–	ns
t_{WW}	$\overline{WR}$ Pulse Width	95	–	ns
t_{DW}	Data Set-up Time ($\overline{WR}$)	95	–	ns
t_{WD}	Data Hold Time ($\overline{WR}$)	0	–	ns
t_{RV}	Recovery Time	165	–	ns

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8.3.2 Clock/Gate

SYMBOL	ITEM	P-2/M-2 MIN.	P-2/M-2 MAX.	UNIT
t_{CLK}	Clock Period	100	DC	ns
t_{PWH}	CLK High Pulse Width	30	–	ns
t_{PWL}	CLK Low Pulse Width	30	–	ns
t_R	CLK Rise Time	–	25	ns
t_F	CLK Fall Time	–	25	ns
t_{GW}	GATE Width High	50	–	ns
t_{GL}	GATE Width LOW	50	–	ns
t_{GS}	GATE Set-up Time (CLK)	40	–	ns
t_{GH}	GATE Hold Time (CLK)	50	–	ns
t_{OD}	Output Delay From CLK	–	100	ns
t_{ODG}	Output Delay From GATE	–	100	ns
t_{WC}	Count Loading Set-up Time (CLK)	80	–	ns
t_{WG}	$\overline{WR}$ Set-up Time (GATE)	0	–	ns
t_{WO}	Output Delay From Command Write	–	240	ns
t_{CL}	CLK Set-up Time (Count Latch)	68	–	ns

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8.4 INPUT CAPACITY (TA = 25°C, VCC = VSS (GND) = 0V)

SYMBOL	ITEMS	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	fc = 1MHz Unmeasured pins, 0V			10	pF
$C_{I/O}$	Inut/Output Capacitance				20	pF

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8.5 AC TEST INPUT WAVEFORM

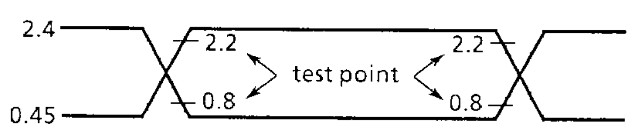

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Figure 8.1 AC test input waveform

9. TIMING DIAGRAM

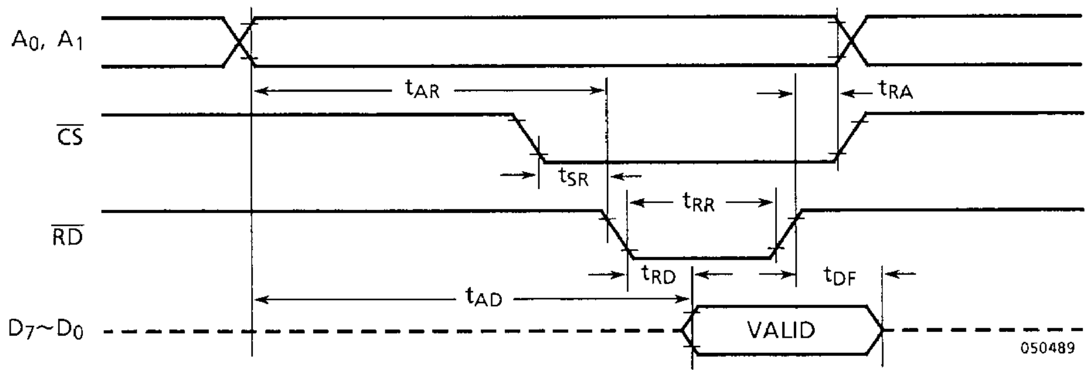


Figure 9.1 Read Operation

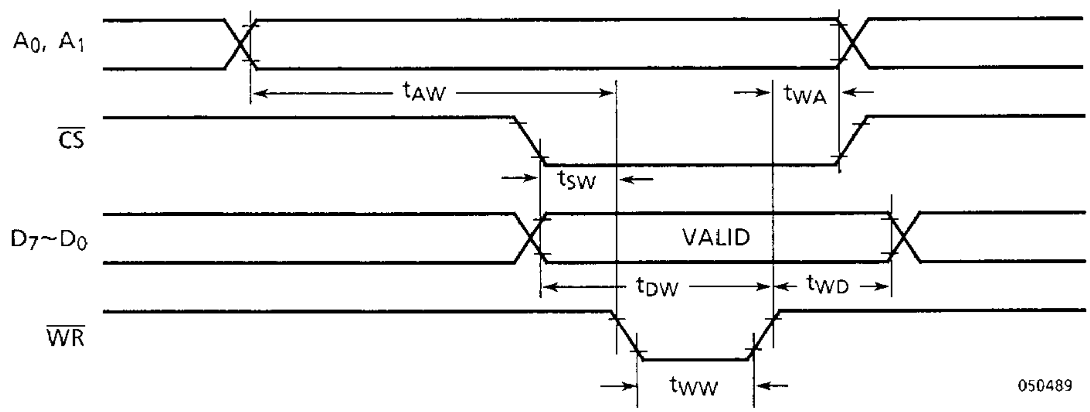


Figure 9.2 Write Operation

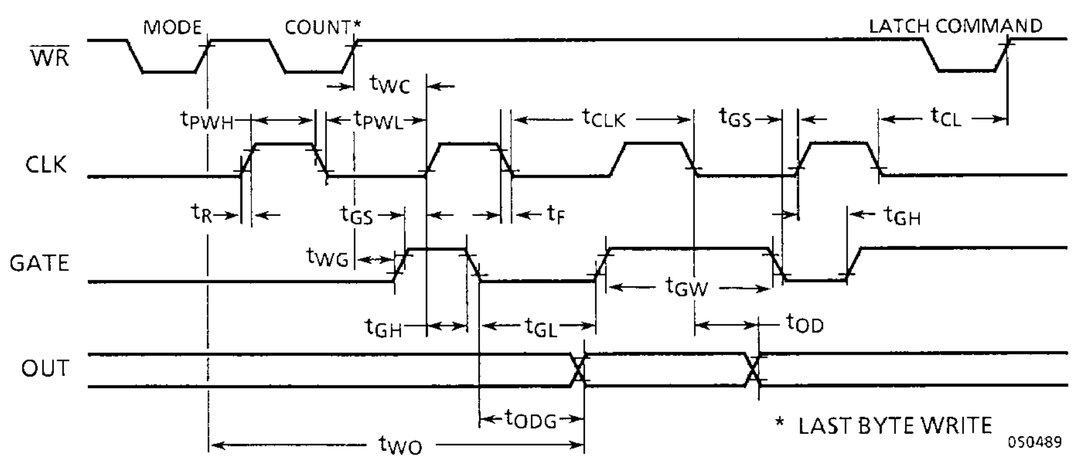


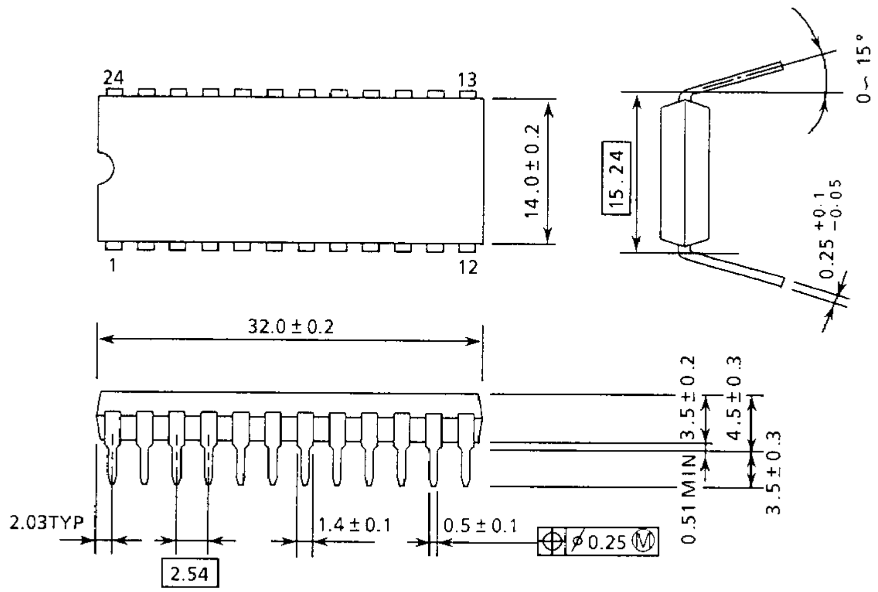
Figure 9.3 Clock and Gate Operations

10. EXTERNAL DIMENSIONS

10.1 24 PIN DIP EXTERNAL DIMENSIONS

DIP24-P-600

Unit : mm



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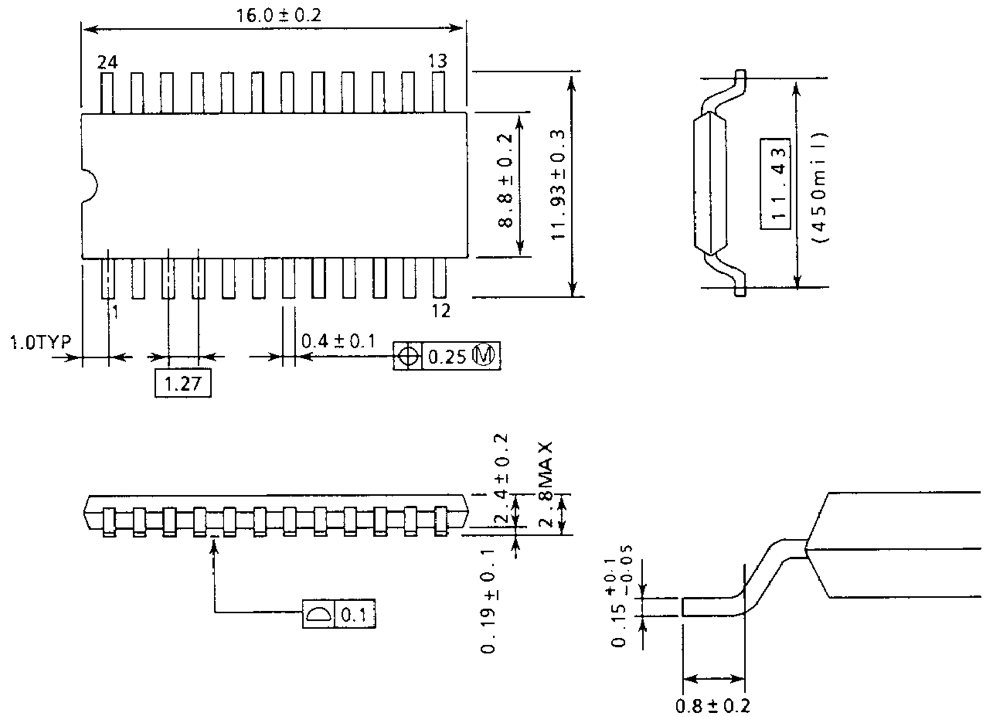
10.2 24 PIN SOP EXTERNAL DIMENSION

SOP24-P-450B

Unit : mm



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Note : Package Width and Length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.