LP3520

Second-Side Synchronous Rectifier

Description

The LP3520 is a high performance second side synchronous rectifier for isolated flyback application in which a synchronous power MOSFET is integrated. The LP3520 is suitable for charger application which the high transfer efficiency is required.

The LP3520 can avoid mis-operation caused by the demagnetization oscillation efficiently by using proprietary primary side turn on estimation and secondary side current discontinuous judgment technology. LP3520 also involves proprietary VCC supply technology which can ensure the IC can work normally in primary side CC and CV working mode.

The LP3520 provides many protections which include VCC UVLO, VCC over voltage clamping , output short max on time shunt down and the DRV pin interference suppression.

The LP3520 is available in SOP7

Features

- Isolated DCM mode application.
- 45V Power MOSFET integrated
- Proprietary Primary Side Turn On Estimation
- Secondary Side Current Discontinuous Judgment
- Proprietary VCC Supply Technology
- VCC Pin UVLO Protection
- VCC Over Voltage Clamping
- DRV Pin Noise Suppression
- Few Peripheral Device
- SOP7 Assembly

Application

- Schottky diode replacement for flyback.
- Suitable for 5V/2A US DoE IV application.
- Charger and Adapter.

Typical Application

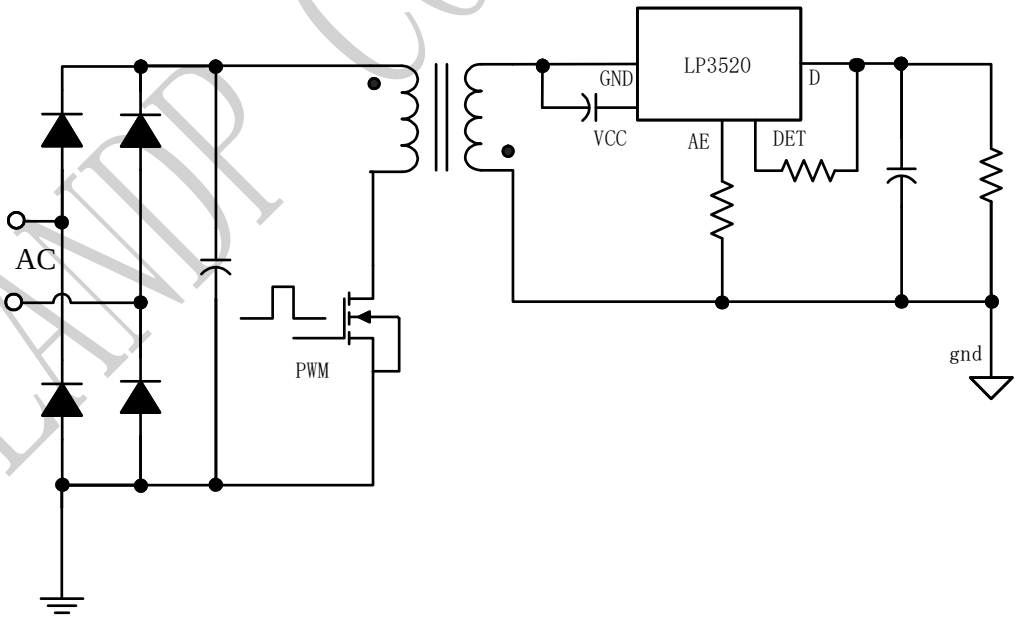


Figure 1: Typical Application Circuit

Ordering Information

Version	Package	Packing Form	Marking
LP3520	SOP7	Tape 3,000 piece/Roll	LP3520 Bxxxx

Pin Definition

Bxxxx： IC Indetifier

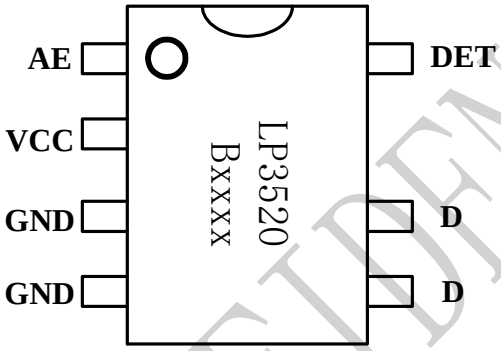


Figure 2: Pin Definition

Terminal Description

Number	Definition	Description
1	AE	Primary side turn on estimation setting pin
2	VCC	The power supply pin for the IC
3，4	GND	The ground pin of the IC
5，6	D	The Drain Pin of the integrated MOSFET
7	DET	The voltage supply and judgment pin of the IC

Absolute Maximum Ratings (note 1)

Symbol	Description	Parameter Scope	Unit
DET	Internal voltage supply and voltage sense pin	-0.3~48	V
D	The Drain Pin of the integrated MOSFET	-0.3~45	V
VCC	The IC supply voltage	-0.3~8	V
AE	Judgment Setting Pin	-0.3~8	V
P_{DMAX}	The power dissipation(note2)	0.45	W
θ_{JA}	The thermal resistance from junction to ambient	120	℃/W
θ_{JC}	The thermal resistance from junction to tube	60	℃/W
T_J	Operating junction temperature range	-40 to 150	℃
T_{STG}	The storage temperature range	-55 to 150	℃
	ESD (note 3)	2	KV

Note 1: *Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Under "recommended operating conditions" the device operation is assured, but some particular parameter may not be achieved. The electrical characteristics table defines the operation range of the device, the electrical characteristics is assured on DC and AC voltage by test program. For the parameters without minimum and maximum value in the EC table, the typical value defines the operation range, the accuracy is not guaranteed by spec.*

Note 2: *The maximum power dissipation decrease if temperature rise, it is decided by T_{JMAX}, θ_{JA}, and environment temperature (T_A). The maximum power dissipation is the lower one between $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ and the number listed in the maximum table.*

Note 3: *Human Body mode, 100pF capacitor discharge on 1.5KΩ resistor*

Electrical Characteristics (Notes 4, 5) **(Unless otherwise specified, V_{CC}=5V and T_A=25 ℃)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Section						
V_{CC}	V_{CC} Operating Voltage	Drain=20V		5.5		V
V_{CC_ON}	V_{CC} Startup Voltage	V_{CC} Rising		3.6		V
V_{CC_UVLO}	V_{CC} UVLO Voltage	V_{CC} Falling		3.2		V
I_{ST}	V_{CC} Startup Current	V_{CC}= V_{CC-ON} - 0.5V		50		uA
Icc	V_{CC} Working Current			120		uA
Vcc_clamp	V_{CC} Clamp Voltage	I_{CC}=40mA		6.2		V
Voltage Sense Section						
SR_ON	MOS Turn on Threshold			0.5		V
SR_OFF1	First Turn off Threshold			-15		mV
SR_OFF2	Second Turn off Threshold			-5		mV
Judgment Setting						
T_SRmin	The Minimum turn on time		2.1	2.2	2.3	us
S_AE	The primary voltage integration setting	R_{AE}=100Kohm	25.5	27.0	28.5	us*V
R_AE	Secondary discontinuous judgment ratio			80		%
Driving Ability						
T_{RISE}	Driving rising time	C_{GATE}=1nF			25	ns
T_{FALL}	Driving falling time	C_{GATE}=1nF			25	ns
MOSFET Section						
R_{DS_ON}	MOSFET On resistance	V_{GS}=6.5V/I_{DS}=0.1A			25	mΩ
BV_{DSS}	MOSFET BVdss	V_{GS}=0V/I_{DS}=25uA	45			V

Note 4: *production testing of the chip is performed at 25 ℃.*

Note 5: *the maximum and minimum parameters specified are guaranteed by test, the typical value are guaranteed by design, characterization and statistical analysis*

Internal Block Diagram

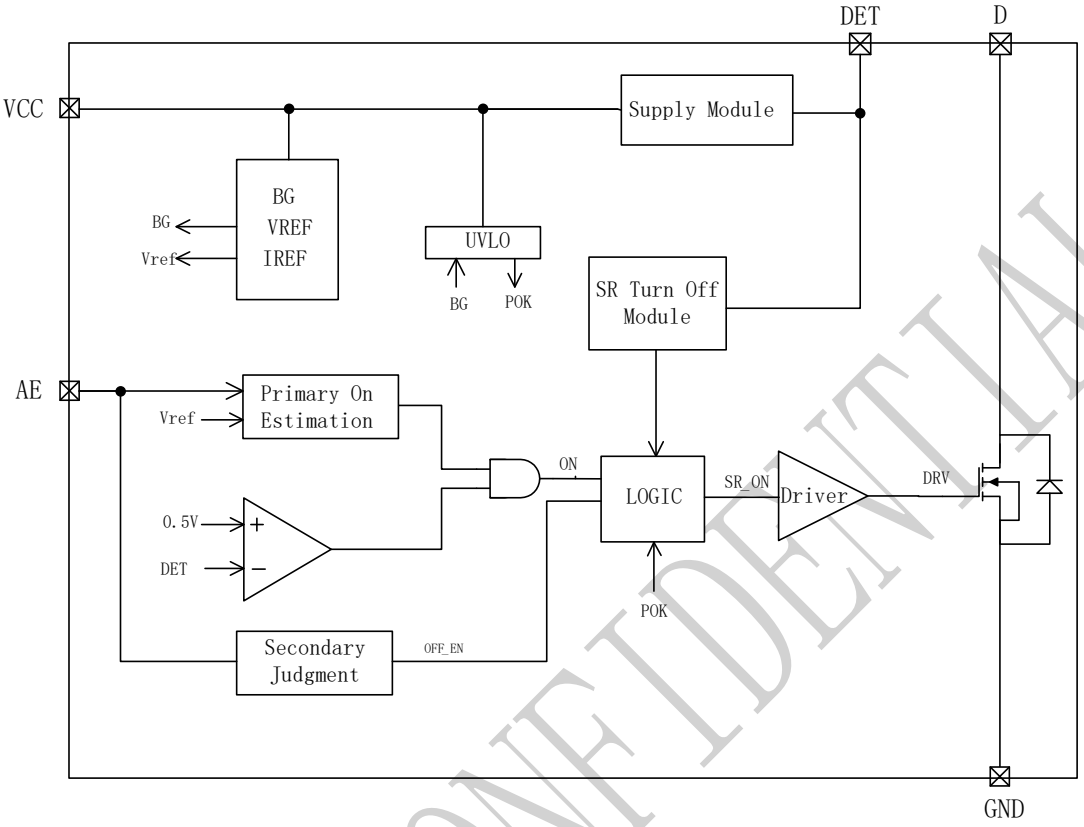


Figure 3: Internal Block Diagram

Application Information

The LP3520 is a high performance second side synchronous rectifier for isolated flyback application in which a synchronous power MOSFET is integrated. The LP3520 can avoid mis-operation caused by the demagnetization oscillation efficiently by using proprietary primary side turn on estimation and secondary side current discontinuous judgment technology. LP3520 also involves proprietary VCC supply technology which can ensure the IC can work normally in primary side CC and CV working mode.

Startup

When the system power on, the output capacitor will be charged by the parasitic body diode of the MSFET and the output voltage will rise .The VCC capacitor of the IC will be charged by the DET pin and when the VCC voltage rise above the startup voltage the IC will operate normally.

Turn On of the SR

When the flyback working at the DCM mode, the DET voltage will oscillate after the second side current fall to zero because of the demagnetization effect. In order to avoid the mistakenly turning on of the SR, the LP3520 uses proprietary primary side turn on estimation technology. When the primary side IC turn on, a flyback voltage will be generated between the secondary side gnd and the LP3520 GND, when the integrated value of the said flyback voltage excess a setting value and the DET pin

voltage falls below 0.5V, the LP3520 will turn on the synchronous MOSFET correctly.

Turn Off of the SR

After the SR is turned on , the DET pin voltage will oscillate because of the parasitic capacitor and the leakage inductor. The said oscillate DET voltage will cause the mistakenly turning off of the MOSFET. In order to avoid this phenomenon, the LP3520 involves secondary side current discontinuous judgment technology.

Through managing the flyback voltage sensed by the AE pin internally and setting the first and second voltage threshold, the LP3520 will turn off the MOSFET correctly.

AE Resistor Setting

$R_{AE}=3.7\times S_{AE}$

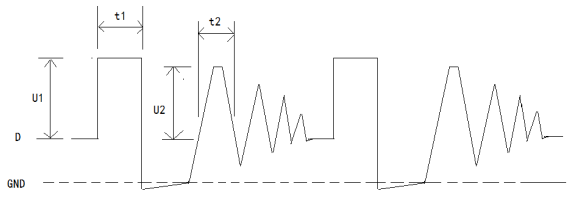
R_{AE}：AE resistor，units: KΩ

S_{AE}：The voltage seconds Size，Units: uS*V

How to set S_{AE}

In light load and 85V~265V, please measure the voltage between the DET pin and the GND pin of the LP3520 which is shown by the following waveform. The S_{AE} must satisfies the following formula:

$$（1.2\times U2\times t2）<S_{AE}<（0.9\times U1\times t1）$$



The Resistor Setting between DET and D Pin

The reasonable resistor value show be smaller than 200 ohm. Higher resistor value will increase the ESD ability and decrease the supply current.

Protection Functions

The LP3520 provides many protections which include VCC UVLO, VCC over voltage clamping , output short max on time shunt down and the DRV pin interference suppression.

PCB Layout

The following rules should be followed in LP3783 PCB layout:

Bypass Capacitor

The bypass capacitor on V_{CC} pin should be as close as possible to the V_{CC} Pin and GND pin.

AE Resistor

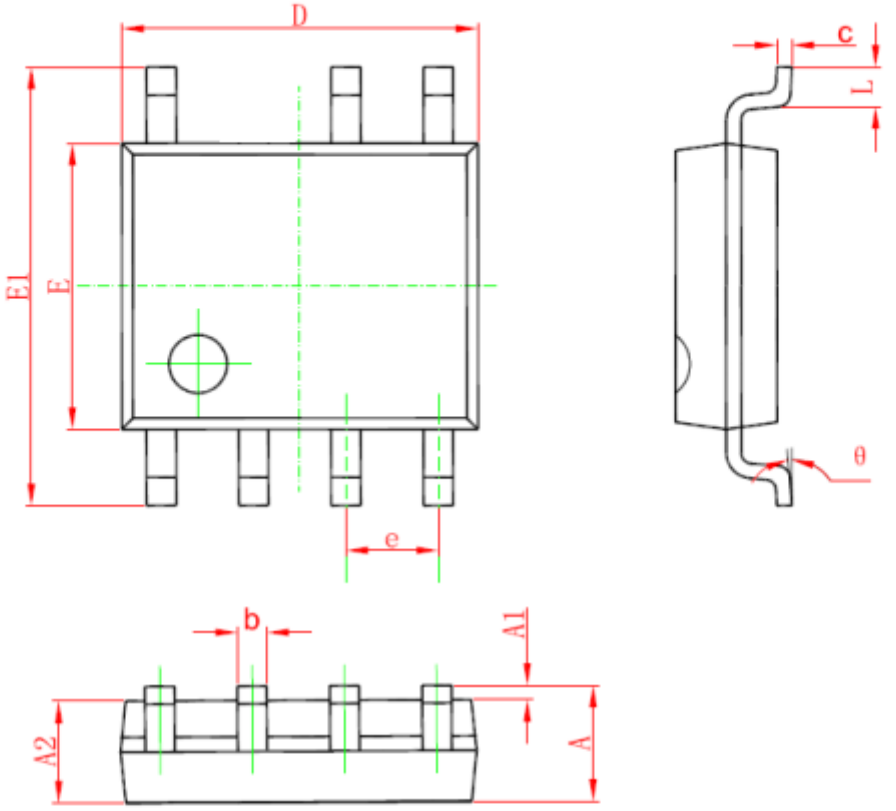
AE resistor should be put as close as to the AE pin and the secondary gnd.

D Pin

To increase the copper area of D pin for better thermal dissipation.

Physical Dimensions

SOP7 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°