Quad SPST CMOS Analog Switch with Latches

DESCRIPTION

The DG221B is a monolithic quad single-pole, single-throw analog switch designed for precision switching applications in communication, instrumentation and process control systems.

Featuring independent onboard latches and a common $\overline{WR}$ pin, each DG221B can be memory mapped, and addressed as a single data byte for simultaneous switching.

The DG221B combines low power and low on-resistance (60 typical) while handling continuous currents up to 20 mA. An epitaxial layer prevents latchup.

The device features true bidirectional performance in the on condition.

FEATURES

- Accepts 150 ns write pulse width
- 5 V on-chip regulator
- Latches are transparent with WR low
- Low on-resistance: 60 W

Pb-free Available

RoHS* COMPLIANT

BENEFITS

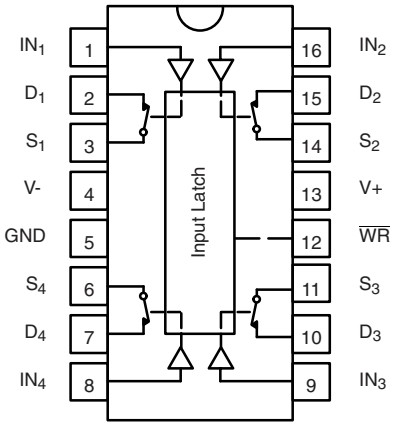
- Compatible with most µP buses
- Allows wide power supply tolerance without affecting TTL compatibility
- Reduced power consumption
- Allows flexibility of design

APPLICATIONS

- µP based systems
- Automatic test equipment
- Communication systems
- Data acquisition systems
- Medical instrumentation
- Factory automation

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line and SOIC



Top View

Four latchable SPST switches per package

TRUTH TABLE		
IN_X	$\overline{WR}$	Switch
0	0	ON
1	0	OFF
X	↑	Control data latched-in, switches on or off as selected by last IN_X
X	1	Maintains previous state

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply.

ORDERING INFORMATION

Temp. Range	Package	Standard Part Number	Lead (Pb)-free Part Number
- 40 °C to 85 °C	16-Pin Plastic DIP	DG221BDJ	DG221BDJ-E3
	16-Pin Narrow SOIC	DG221BDY DG221BDY-T1	DG221BDY-E3 DG221BDY-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Voltages Referenced V+ to V-		34	V
GND		25	
Digital Inputs[a], V_S, V_D		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Continuous Current (Any Terminal)		30	mA
Continuous Current, S or D		20	
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)		70	
Storage Temperature	(DJ and DY Suffix)	- 65 to 125	°C
Power Dissipation (Package)[b]	16-Pin Plastic DIP[c]	470	mW
	16-Pin SOIC[d]	600	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.5 mW/°C above 25 °C.
d. Derate 7.7 mW/°C above 75 °C.

SCHEMATIC DIAGRAM Typical Channel

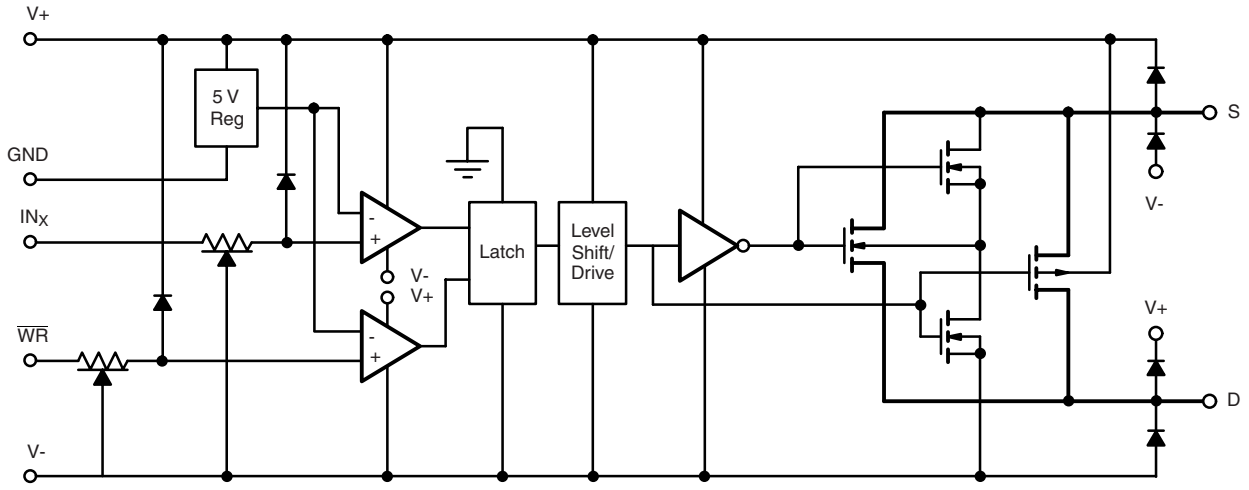


Figure 1.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V V_{IN} = 2.4 V, 0.8 V[f], $\overline{WR}$ = 0	Temp.[b]	Limits - 40 °C to 85 °C Min.[d]	Typ.[c]	Max.[d]	Unit
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	- 15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = - 10 mA, V_D = ± 10 V	Room Full		60	90 135	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ± 14 V, V_D = ± 14 V	Room Full	- 5 - 100	± 0.01	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$		Room Full	- 5 - 100	± 0.02	5 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ± 14 V	Room Full	- 5 - 200	± 0.01	5 200	
Digital Control							
Input Current	I_{INL}, I_{INH}	V_{IN} = 0 V or = 2.4 V	Room Full	- 1 - 10	- 0.0004	1 10	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	See Figure 2	Room			550	ns
Turn-Off Time	t_{OFF}		Room			340	
Turn-On Time Write	t_{ON}, $\overline{WR}$	See Figure 3	Room			550	
Turn-Off Time Write	t_{OFF}, $\overline{WR}$		Room			340	
Write Pulse Width	t_W	See Figure 4	Room	150	120		
Input Setup Time	t_S		Room	180	130		
Input Hold Time	t_H		Room	20	18		
Charge Injection	Q	C_L = 1000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		20		pC
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S, V_D = 0 V	Room		8		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		9		
Channel On Capacitance	$C_{D(on)}$		Room		29		
Off-Isolation	OIRR	V_S = 1 V_{p-p}, f = 100 kHz C_L = 15 pF, R_L = 1 kΩ	Room		70		dB
Interchannel Crosstalk	X_{TALK}		Room		90		
Power Supplies							
Positive Supply Current	I+	All Channels On or Off V_{IN} = 0 V or 2.4 V	Full		0.8	1.5	mA
Negative Supply Current	I–		Room	- 1	- 0.4		

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, Full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

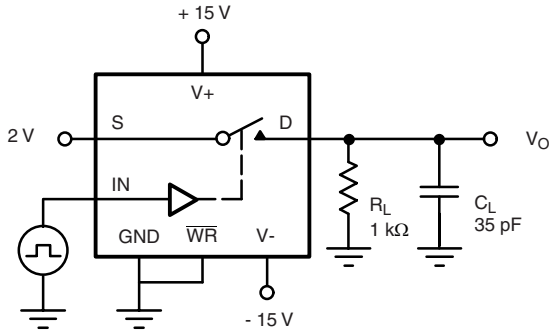
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

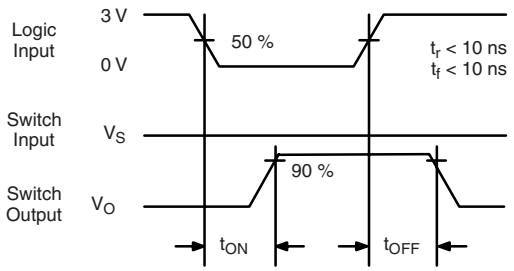
e. Guaranteed by design, not subject to production test.

f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TEST CIRCUITS

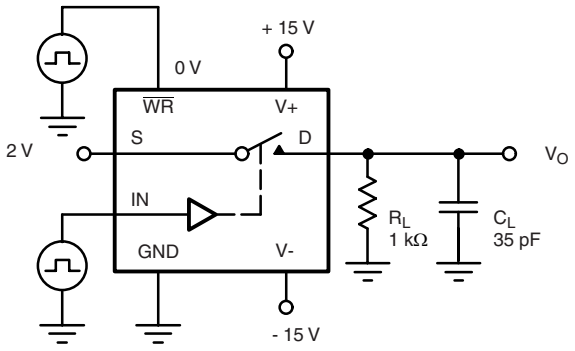


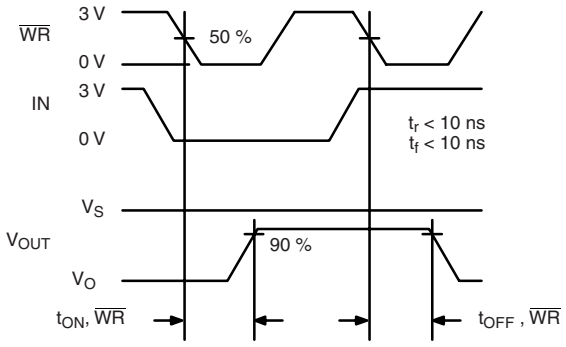


C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2. Switching Time

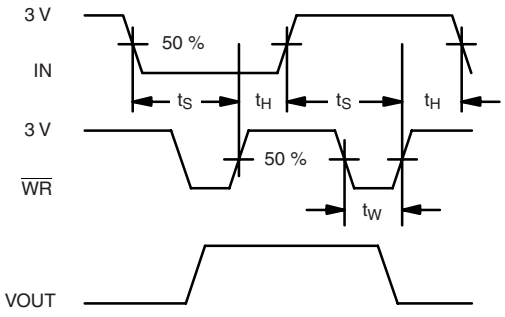




C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

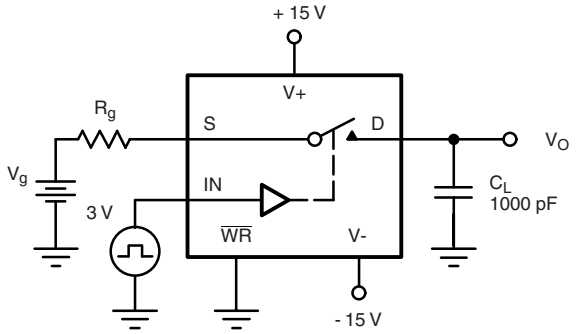
Figure 3. $\overline{WR}$ Switching Time

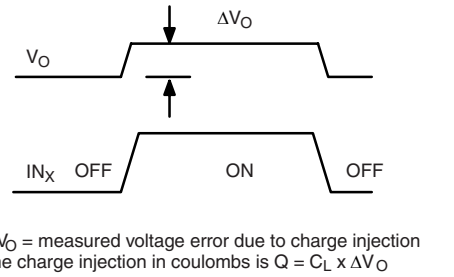


t_H = Hold Time
t_S = Setup Time
t_W = $\overline{WR}$ Pulse Width

Figure 4. $\overline{WR}$ Setup Conditions

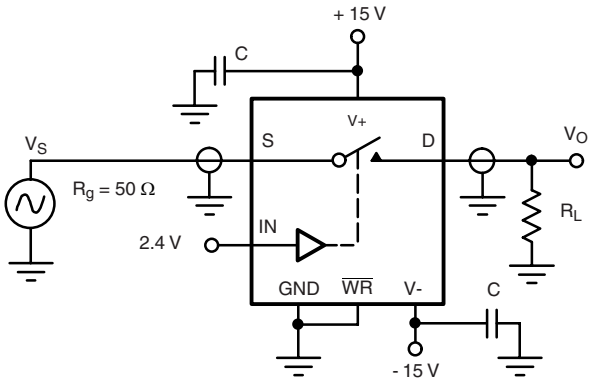
TEST CIRCUITS





ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

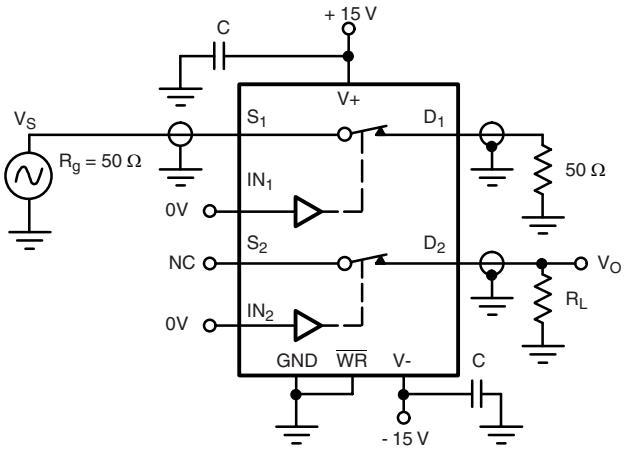
Figure 5. Charge Injection



Off Isolation = 20 log $\left| \frac{V_S}{V_O} \right|$

C = RF bypass

Figure 6. Off Isolation



X_{TALK} Isolation = 20 log $\left| \frac{V_S}{V_O} \right|$

C = RF bypass

Figure 7. Channel-to-Channel Crosstalk

APPLICATION HINTS[a]					
V+ Positive Supply Voltage (V)	**V- Negative Supply Voltage (V)**	**GND (V)**	**$\overline{WR}$ (V)**	**V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)**	**V_S or V_D Analog Voltage Range (V)**
15	- 15	0	2.4/0.8	2.4/0.8	- 15 to 15
10	- 10	0	2.4/0.8	2.4/0.8	- 10 to 10
10	- 5	0	2.4/0.8	2.4/0.8	- 5 to 10

Notes:
a. Application hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

APPLICATIONS

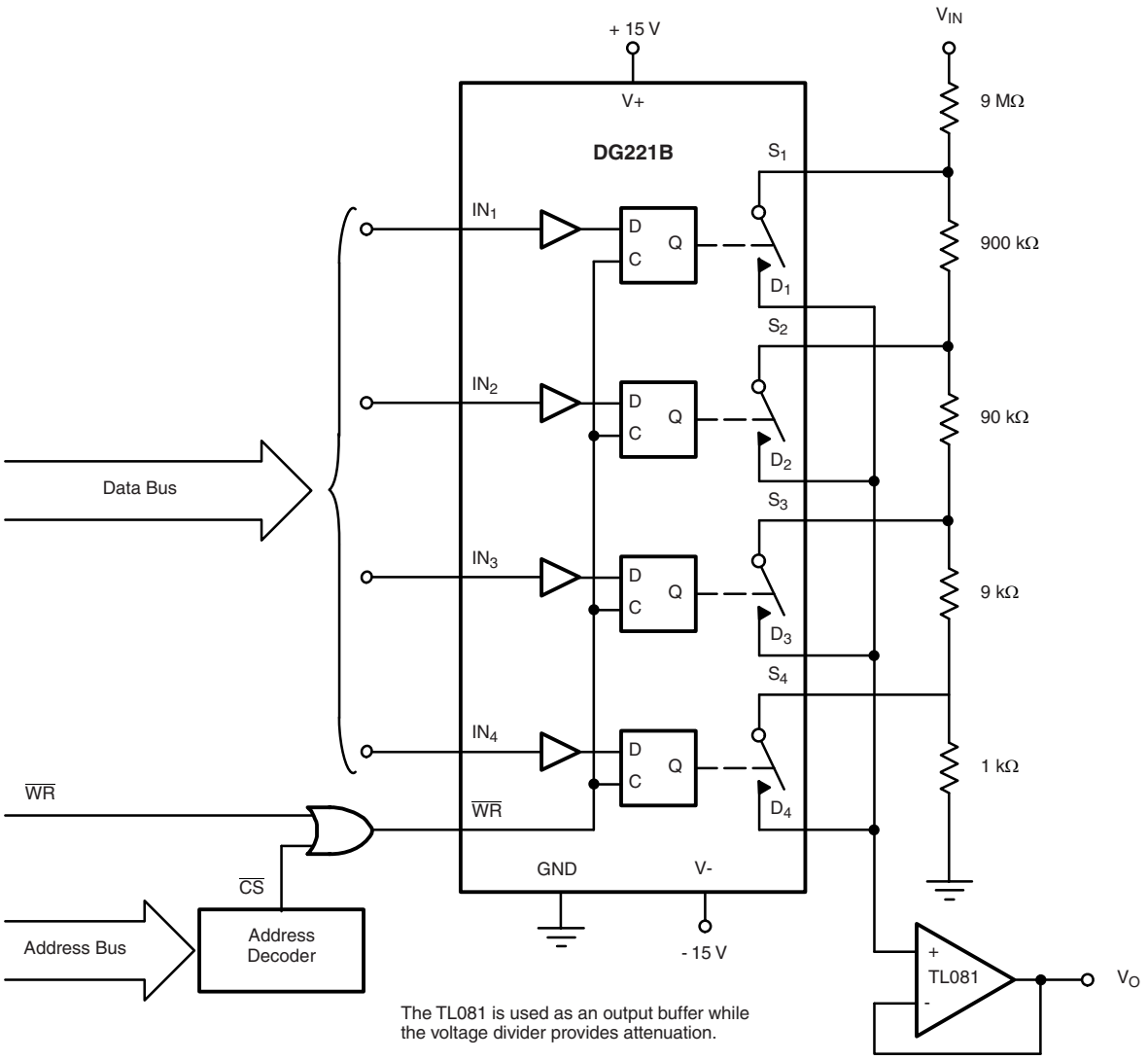


Figure 7. µP-Controlled Analog Signal Attenuator

TRUTH TABLE					
IN_1	IN_2	IN_3	IN_4	$\overline{WR}$[a]	ON SWITCH
0	0	0	0	0	All
1	1	1	1	0	None
0	1	1	1	0	1
1	0	1	1	0	2
1	1	0	1	0	3
1	1	1	0	0	4

OUTPUT ATTENUATION FOR FIGURE 7					
$\overline{WR}$	IN_1	IN_2	IN_3	IN_4	Gain
0	0	1	1	1	0.1
0	1	0	1	1	0.01
0	1	1	0	1	0.001
0	1	1	1	0	0.0001

Notes:

a. $\overline{WR}$ may be held at "0" for temporary operation similar to DG201A/DG201B. With $\overline{WR}$ at “0” SW_1 will remain on as long as IN_1 is held at "0" V.

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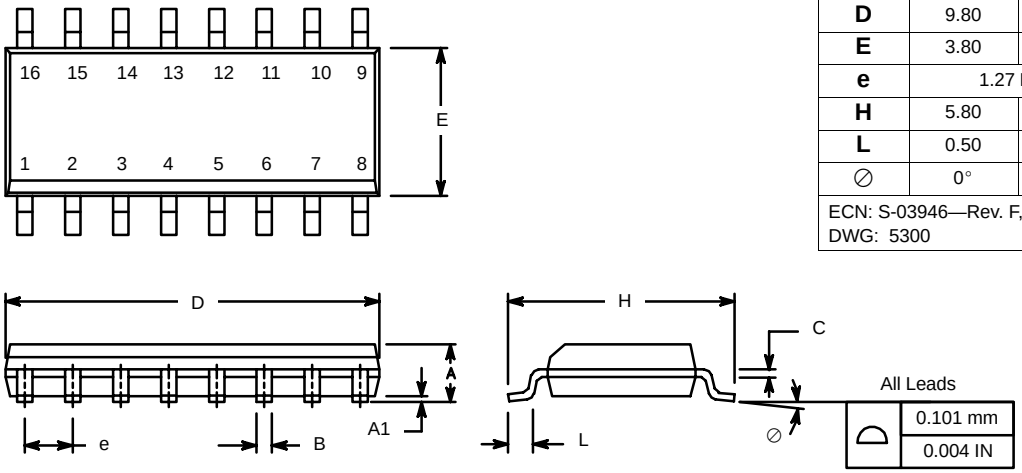
SOIC (NARROW): 16-LEAD

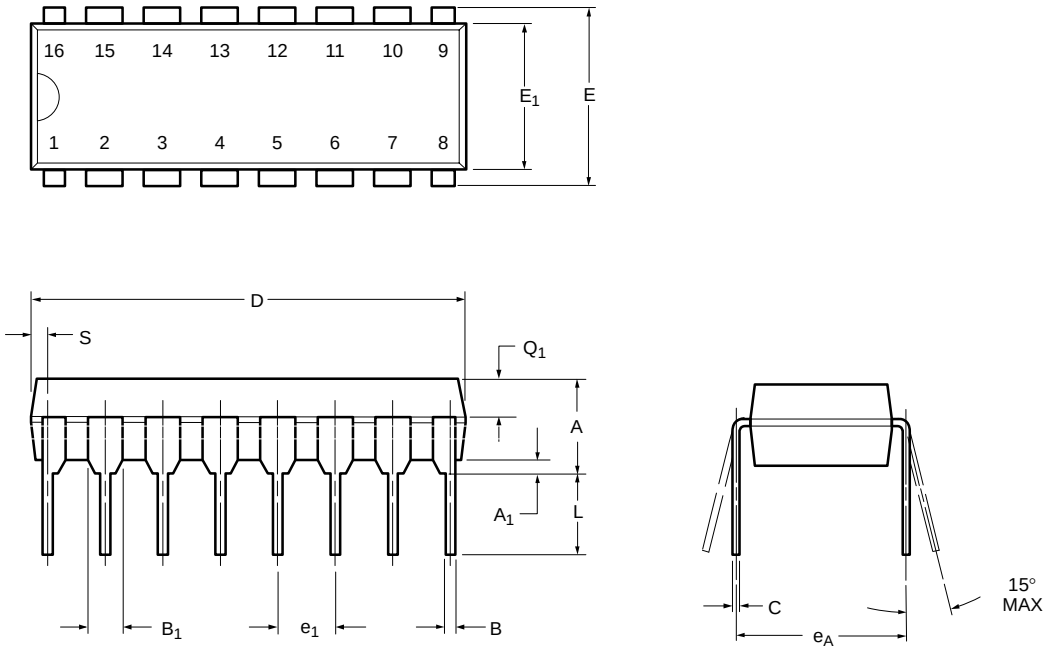
JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

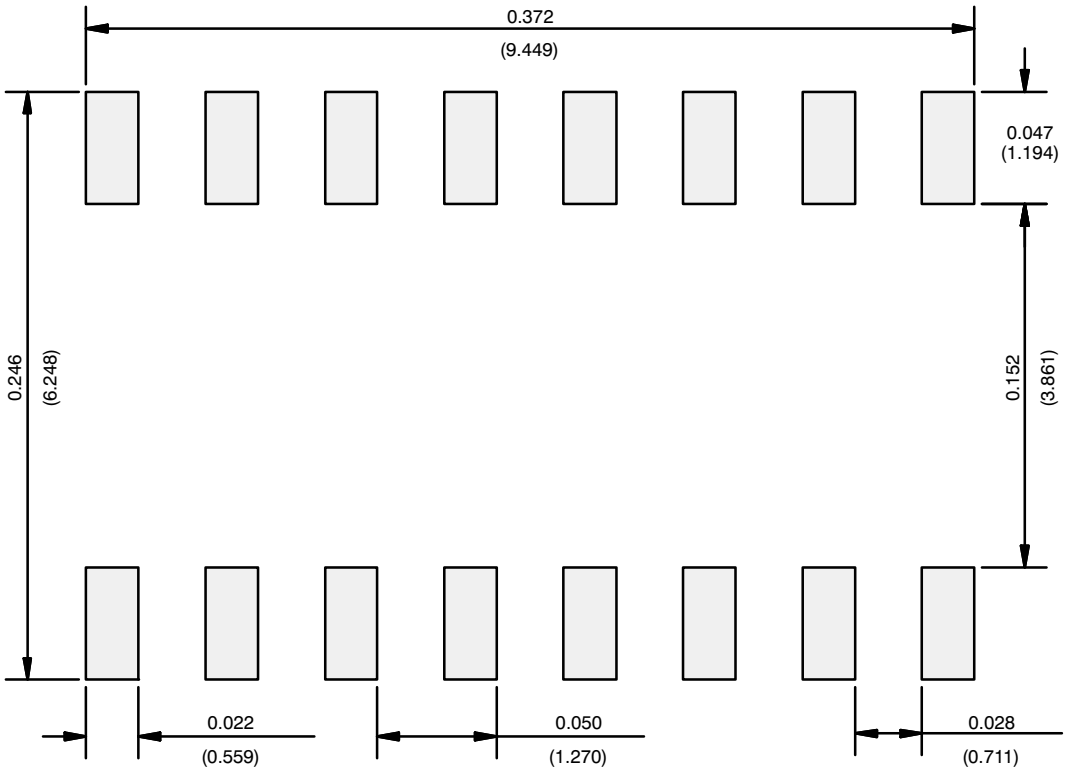


PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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