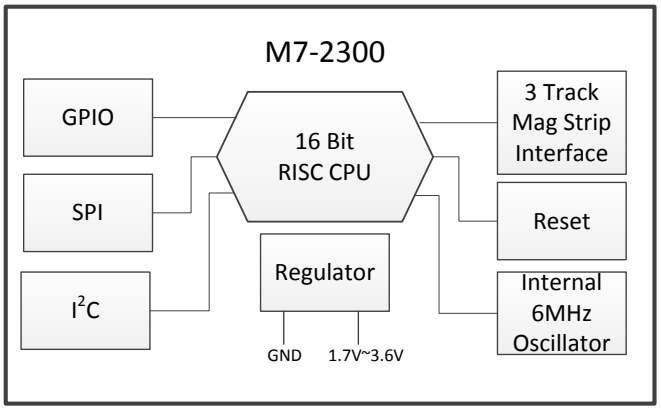
# M7-2300 *Magnetic Card Reader IC*

## Feature

- 1.7V to 3.6V Operating Voltage.
- ISO 7811/7812/7813 Compliant.
- Triple-Track Magnetic Stripe Head Interface.
- Acceptable amplitude from 10% to 155% of ISO reference voltage.
- Low-Power Operation.
- SPI or $I^2C$ interface.
- 6MHz Internal Oscillator (±10%).

## Functional block diagram




The M7-2300 is a RISC-based microcontroller intended for integration into magnetic card readers. It can be interfaced directly to a 3-track magnetic card reader head. Communication peripherals include a hardware SPI and a hardware $I^2C$.

## Description

Magnetic Card Reader (M7-2300) is an integrated triple-track magnetic stripe reader IC. The M7-2300 communicates to a host processor through an SPI or $I^2C$ interface.

## Applications

- Magnetic stripe card reader
- ATM/Financial Terminals
- POS
- Security Control

## Ordering information

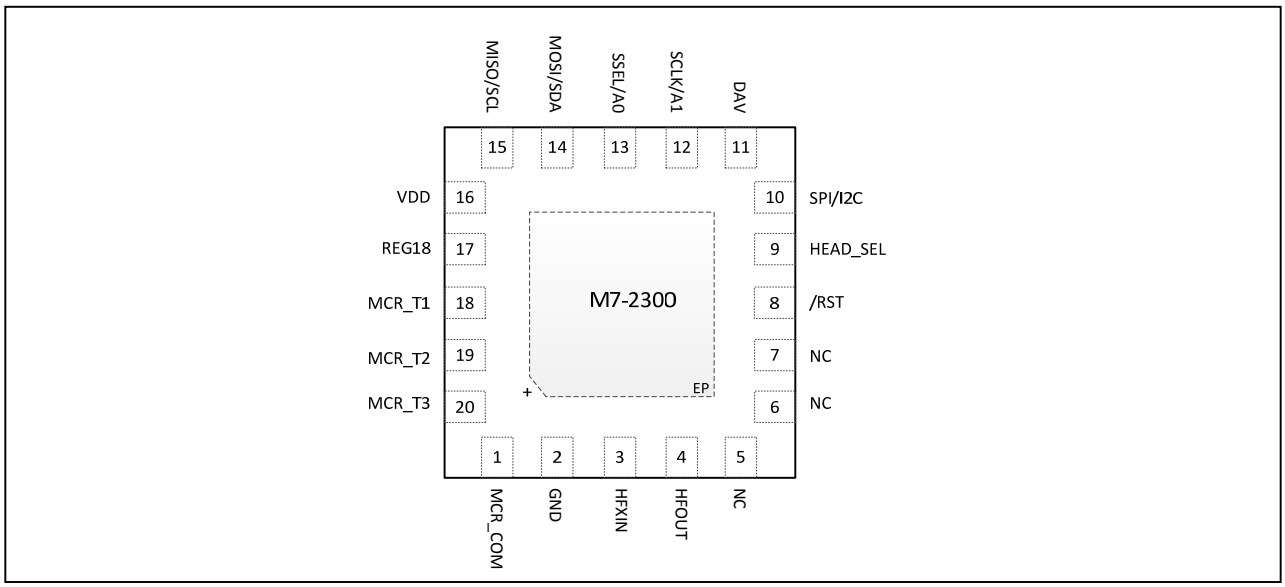
| No | Interface | Part Number |
|---|---|---|
| 1 | SPI / $I^2C$ | M7-2300 |

## Coded character

| Item | | Content | | |
|---|---|---|---|---|
| **ISO 7811 ~ 7813** | **Track** | Track 1 | Track 2 | Track 3 |
| | **Recording Density** | 210 BPI | 75 BPI | 210 BPI |
| | **Capacity** | 79 Characters (7 Bit Code) | 40 Characters (5 Bit Code) | 107 Characters (5 Bit Code) |
| | **Start / End Code** | % / ? | ; / ? | ; / ? |

# M7-2300 *Magnetic Card Reader IC*

## Pin Configuration




## PinDescription

| PIN | NAME | FUNCTION |
|---|---|---|
| **POWER PINS** | | |
| 16 | $V_{DD}$ | Digital Supply Voltage |
| 17 | REG18 | Regulator Capacitor. This pin must be connected to ground through an external 1μF external ceramic chip capacitor. This capacitor should be placed as close to this pin as possible. |
| 2 | GND | Digital Ground |
| **RESET PIN** | | |
| 8 | /RST | Active-Low Reset. This bidirectional pin serves as the active low external reset. When an external low pulse of more than 400μs is recognized, the device will assert and hold an internal reset as long as the pin is held low. It also acts as an output when the source of the reset is internal to the device (e.g., power-fail). In this case, the pin is low as long as the processor is in the reset state. |
| **CLOCK PINS** | | |
| 3 | HFXIN | Oscillator Inputs. Connect HFXIN to GND and leave HFXOUT unconnected to select the internal oscillator as the clock source. An external crystal or resonator connected between HFXIN and HFXOUT selects the external crystal or resonator as the clock source. |
| 4 | HFXOUT | |

| PIN | NAME | FUNCTION | |
|---|---|---|---|
| **PROGRAMMING/CONFIGURATION INTERFACE PINS** | | | |
| These pins are the programming and configuration interface for the device. Unconnected pins read as a logic 1. | | | |
| 5 | NC | Reserved for Future Use. Do not connect this pin. | |
| 6 | NC | Reserved for Future Use. Do not connect this pin. | |
| 7 | NC | Reserved for Future Use. Do not connect this pin. | |
| 9 | HEAD_SEL | Head Inductance Select Default.<br>HEAD_SEL = 1: Low inductance (20mH~60mH).<br>HEAD_SEL = 0: High inductance (80mH~140mH). | |
| 10 | SPI/I2C | SPI or $I^2C$ Communication Interface.<br>SPI/I2C = 1: Select SPI Mode.<br>SPI/I2C = 0: Select $I^2C$ Mode. | |
| 11 | DAV | Data available output. | |
| 12 | SCLK/A1 | **SPI/I2C = 1** | **SPI/I2C = 0** |
| | | SPI Slave Clock Input | $I^2C$ Slave Address A[1:0] Default. The least-significant bit is ignored when comparing addresses. |
| 13 | SSEL/A0 | SPI Slave Select Input | **A[1:0]** / **Slave Address**<br>00 / 0101_000x<br>01 / 0101_001x<br>10 / 0101_010x<br>11 / 0101_011x |
| 14 | MOSI/SDA | SPI Master Out, Slave In Input | $I^2C$ SDA |
| 15 | MISO/SCL | SPI Master In, Slave Out Output | $I^2C$ SCL |
| **MAGNETIC STRIPE READER PINS** | | | |
| 18 | MCR_T1 | Magnetic Stripe Reader Track 1 Signal. This analog input should be connected to the magnetic stripe reader associated with track 1. This pin must be connected to MCR_COM if not used. | |
| 19 | MCR_T2 | Magnetic Stripe Reader Track 2 Signal. This analog input should be connected to the magnetic stripe reader associated with track 2. This pin must be connected to MCR_COM if not used. | |
| 20 | MCR_T3 | Magnetic Stripe Reader Track 3 Signal. This analog input should be connected to the magnetic stripe reader associated with track 3. This pin must be connected to MCR_COM if not used. | |
| 1 | MCR_COM | Magnetic Stripe Reader Common Node. This pin is the common node for all three track signal inputs. | |
| **EXPOSED PAD** | | | |
| — | EP | Exposed Pad. Connected to GND. | |

# M7-2300 *Magnetic Card Reader IC*

## Absolute Maximum Ratings

(All voltages with respect to GND.)

Voltage Range on $V_{DD}$.....-0.3V to +3.6V
Voltage Range on Any Lead.....-0.3V to ($V_{DD}$ + 0.5V)
Continuous Output Current
Any Single I/O Pin.....25mA
All I/O Pins Combined.....25mA

Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

## Electrical Characteristics

(Limits are 100% tested at $T_A$ = +25°C and $T_A$ = +85°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

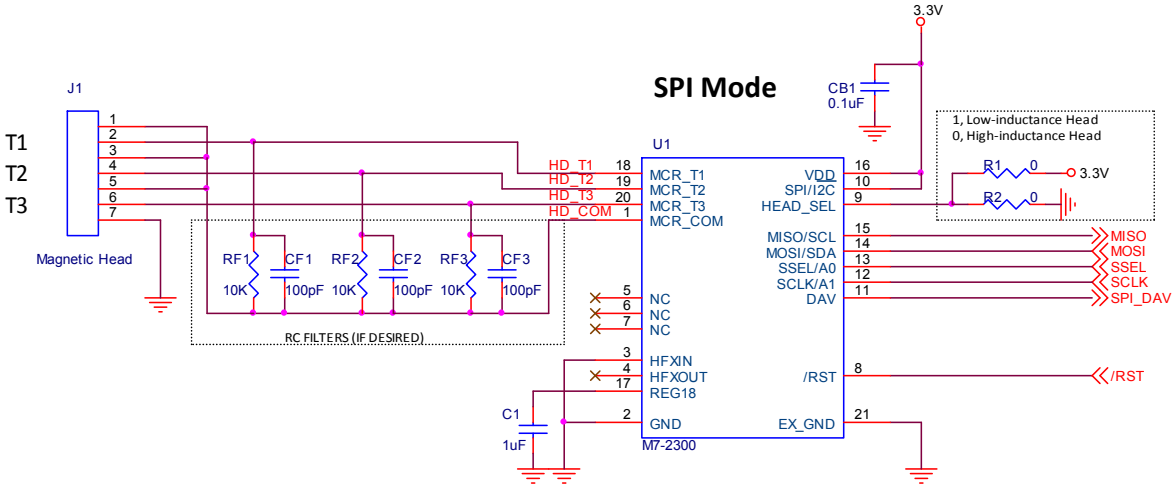
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | Do not execute the lock or unlock commands if $V_{DD}$ < 1.85V | $V_{RST}$ | | 3.6 | V |
| Power-Fail Reset Voltage | $V_{RST}$ | Monitors $V_{DD}$ (Note 1) | 1.64 | 1.67 | 1.7 | V |
| Power-On-Reset Voltage | $V_{POR}$ | Monitors $V_{DD}$ | | 1.6 | | V |
| Supply Current | $I_{DD}$ | Measured on $V_{DD}$ pin, device not in reset, all inputs connected to GND or $V_{DD}$; outputs do not source/sink any current; not including MCR AFE current ($I_{TRACK}$) | | 1.5 | 2.0 | mA |
| **DIGITAL I/O (SPI, I²C, DAV, RST)** | | | | | | |
| Input High Voltage (MOSI, SSEL, SDA, SCL, /RST) | $V_{IH}$ | | 0.7 x $V_{DD}$ | | $V_{DD}$ | V |
| Input Hysteresis | $V_{IHYS}$ | GBD | | 300 | | mV |
| Input Low Voltage (MOSI, SSEL, SDA, SCL, /RST) | $V_{IL1}$ | | $V_{GND}$ | | x $V_{DD}$ | V |
| Output Low Voltage (MISO, DAV, SDA, SCL, /RST) | $V_{OL}$ | $V_{DD}$ = 2.4V, $I_{OL}$ = 4mA | $V_{GND}$ | | 0.5 | V |
| Output High Voltage (MISO, DAV, SDA, SCL, /RST) | $V_{OH}$ | $V_{DD}$ = 2.4V,$I_{OH}$ = -2mA | $V_{DD}$ - 0.5 | | $V_{DD}$ | V |
| Input Leakage Current | $I_L$ | Internal pullup disabled | -100 | | +100 | nA |
| Input Pullup Resistance Low Voltage (MOSI, SSEL, SDA, SCL, /RST) | $R_{PU}$ | | | 28 | | kΩ |
| **MAGNETIC CARD READER HEAD INPUTS** | | | | | | |
| Recommended Voltage Level Input | $V_{MHI}$ | (Note 2) | 2 | | 200 | mV |
| MCR AFE Current (per Track) | $I_{TRACK}$ | Typical value measured with fixed gain of 3, max value measured with fixed gain of 7 | | 0.6 | 1.15 | mA |

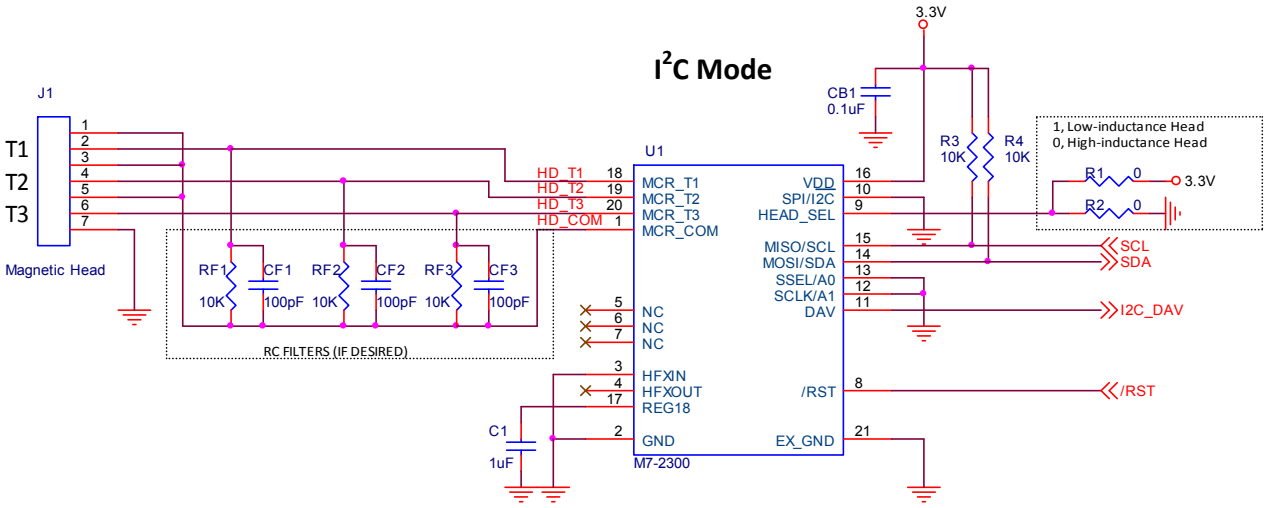
**Note 1:** The power-fail reset and power-on-reset detectors operate in tandem so one or both of these signals are active at all times when $V_{DD}$ < $V_{RST}$, ensuring the device maintains the reset state until minimum operating voltage is achieved.

**Note 2:** Value is the amplitude with a DC offset of MCR_COM output voltage. The 2mV to 200mV is the flux event min/max amplitude from MCR_COM (which is $V_{DD}$/2). The 2mV to 200mV can be above MCR_COM as well as below MCR_COM. The magnetic card reader tolerates as much as 20% noise amplitude.

# M7-2300 *Magnetic Card Reader IC*

## Typical Application Circuit:

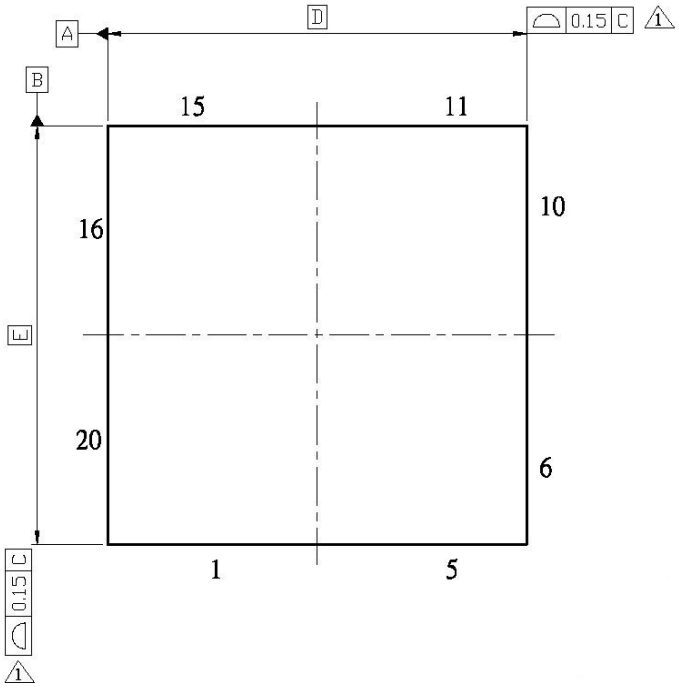


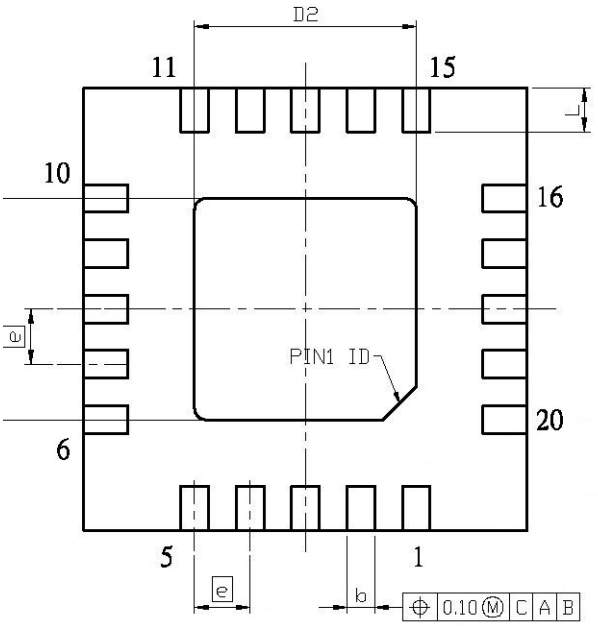



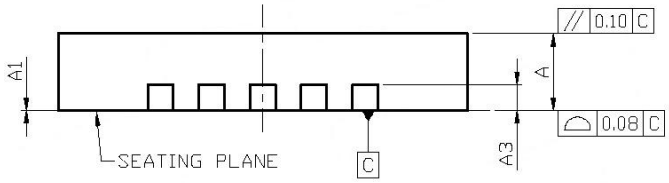

| | Inductance Value | HEAD_SEL | RF(1/2/3) | CF(1/2/3) |
|---|---|---|---|---|
| **Low inductance** | 20mH ~ 60mH | 1 | 3.6kΩ | 100pF |
| **High inductance** | 80mH ~ 140mH | 0 | 10kΩ | 100pF |

# M7-2300 *Magnetic Card Reader IC*

## Package outline




| SYMBOL | DIMENSION (MM) | | | DIMENSION (MIL) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 27.56 | 29.53 | 31.50 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.79 | 1.97 |
| A3 | 0.203 REF | | | 8 REF | | |
| b | 0.18 | 0.25 | 0.30 | 7.09 | 9.84 | 11.81 |
| D | 3.90 | 4.00 | 4.10 | 153.5 | 157.5 | 161.4 |
| D2 | 1.90 | 2.00 | 2.10 | 74.8 | 78.7 | 82.7 |
| E | 3.90 | 4.00 | 4.10 | 153.5 | 157.5 | 161.4 |
| E2 | 1.90 | 2.00 | 2.10 | 74.8 | 78.7 | 82.7 |
| e | 0.50 BSC | | | 19.69 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 11.81 | 15.74 | 19.69 |

**MSL Rating:** Level 3

MSL Standard: IPC/JEDEC J-STD-020

Packing Standard: IPC/JEDEC J-STD-033

**ESD Testing:**

ESD Standard: JESD22-A114

Human Body Model: 2KV passed

# Appendix A

## I²C Serial Peripheral Specifications

(See Figure 1 and Figure 2.)

| PARAMETER | SYMBOL | CONDITIONS | STANDARD MODE | | FAST MODE | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| Input Low Voltage | $V_{IL\_I2C}$ | Supply voltages that mismatch I²C bus levels must relate input levels to the $R_P$ pullup voltage | -0.5 | 0.3 x $V_{DD}$ | -0.5 | 0.3 x $V_{DD}$ | V |
| Input High Voltage | $V_{IH\_I2C}$ | Supply voltages that mismatch I²C bus levels must relate input levels to the $R_P$ pullup voltage | 0.7 x $V_{DD}$ | | 0.7 x $V_{DD}$ | $V_{DD}$ + 0.5V | V |
| Input Hysteresis (Schmitt) | $V_{IHYS\_I2C}$ | $V_{DD}$ > 2V | | | 0.05 x $V_{DD}$ | | V |
| Output Logic-Low (Open Drain or Open Collector) | $V_{OL\_I2C}$ | $V_{DD}$ > 2V, 3mA sink current | 0 | 0.4 | 0 | 0.4 | V |
| Capacitive Load for Each Bus Line | $C_B$ | | | 400 | | 400 | pF |
| Output Fall Time from $V_{IH\_MIN}$ to $V_{IL\_MAX}$ with Bus Capacitance from 10pF to 400pF | $t_{OF\_I2C}$ | $t_{R/F\_I2C}$ exceeds $t_{OF\_I2C}$, which permits RS to be connected as shown in figure | | 250 | 20 + 0.1$C_B$ | 250 | ns |
| Pulse Width of Spike Filtering That Must Be Suppressed by Input Filter | $t_{SP\_I2C}$ | | | | 0 | 50 | ns |
| Input Current on I/O | $I_{IN\_I2C}$ | Input voltage from 0.1 x $V_{DD}$ to 0.9 x $V_{DD}$ | -10 | +10 | -10 | +10 | µA |
| I/O Capacitance | $C_{IO\_I2C}$ | | | 10 | | 10 | pF |
| I²C Bus Operating Frequency | $f_{I2C}$ | | 0 | 100 | 0 | 400 | kHz |
| System Frequency | $f_{SYS}$ | | 0.90 | | 3.60 | | MHz |
| I²C Bit Rate | $f_{I2C}$ | | | $f_{SYS}$/8 | | $f_{SYS}$/8 | Hz |
| Hold Time After (Repeated) START | $t_{HD:STA}$ | | 4.0 | | 0.6 | | µs |
| Clock Low Period | $t_{LOW\_I2C}$ | | 4.7 | | 1.3 | | µs |
| Clock High Period | $t_{HIGH\_I2C}$ | | 4.0 | | 0.6 | | µs |
| Setup Time for Repeated START | $t_{SU:STA}$ | | 4.7 | | 0.6 | | µs |

## I²C Serial Peripheral Specifications (continued)

(See Figure 1 and Figure 2.)

| PARAMETER | SYMBOL | CONDITIONS | STANDARD MODE | | FAST MODE | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| Hold Time for Data | $t_{HD:DAT}$ | A device must internally provide a hold time of at least 300ns for $V_{IH\_I2C(MIN)}$ to bridge the undefined region of the falling edge of SCL. The maximum $t_{HD:DAT}$ needs to be met only if the device does not stretch the SCL low period | 0 | 3.45 | 0 | 0.9 | µs |
| Setup Time for Data | $t_{SU:DAT}$ | A fast-mode I²C bus device can be used in a standard-mode I²C bus system; if such a device does not stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R\_I2C(MAX)} + t_{SU:DAT}$ = 1000 + 250 = 1250ns (according to the standard-mode I²C specification) before the SCL line is released | 250 | | 100 | | ns |
| SDA/SCL Fall Time | $t_{F\_I2C}$ | | | 300 | 20 + $0.1C_B$ | 300 | ns |
| SDA/SCL Rise Time | $t_{R\_I2C}$ | | | 1000 | 20 + $0.1C_B$ | 300 | ns |
| Setup Time for STOP | $t_{SU:STO}$ | | 4.0 | | 0.6 | | µs |
| Bus Free Time Between STOP and START | $t_{BUF}$ | | 4.7 | | 1.3 | | µs |
| Noise Margin at the Low Level for Each Connected Device (Including Hysteresis) | $V_{nL\_I2C}$ | | 0.1 x $V_{DD}$ | | 0.1 x $V_{DD}$ | | V |
| Noise Margin at the Low Level for Each Connected Device (Including Hysteresis) | $V_{nH\_I2C}$ | | 0.2 x $V_{DD}$ | | 0.2 x $V_{DD}$ | | V |

## I²C Serial Diagrams

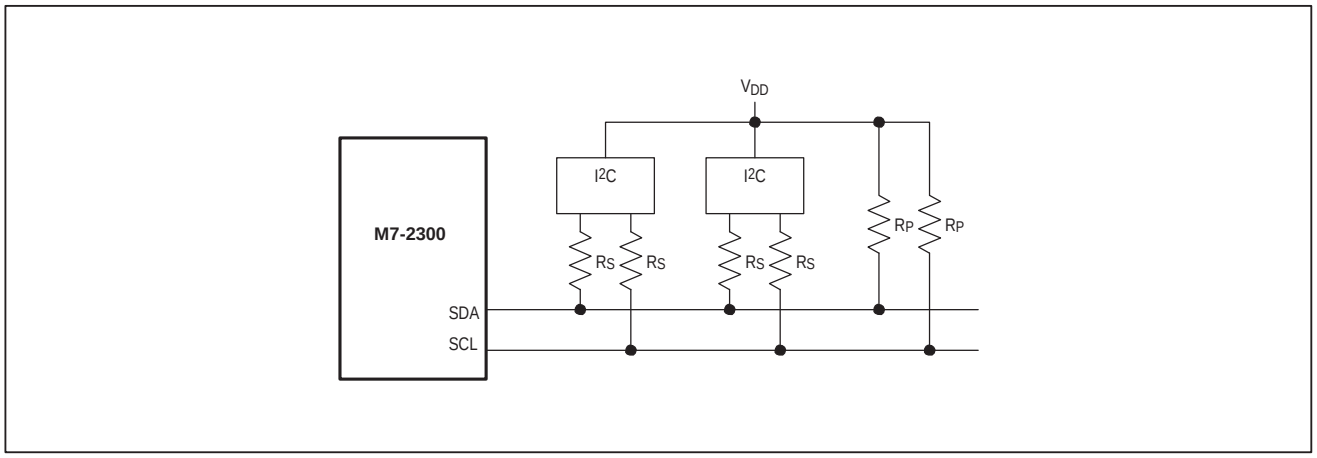



*Figure 1. Series Resistors ($R_S$) for Protecting Against High-Voltage Spikes*

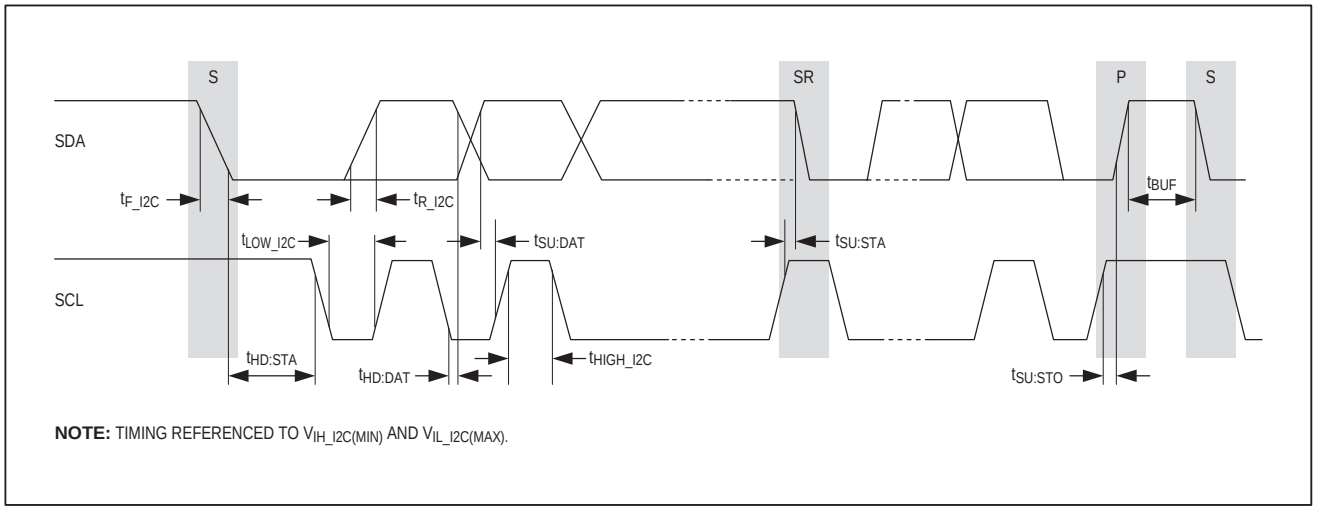



*Figure 2. I²C Bus Controller Timing Diagram*

## Serial Peripheral Interface (SPI) Specifications

(See Figure 3 and Figure 4.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SPI Master Operating Frequency | $1/t_{MCK}$ | | | | $f_{CK}/2$ | MHz |
| SPI Slave Operating Frequency | $1/t_{SCK}$ | | | | $f_{CK}/4$ | MHz |
| SCLK Output Pulse-Width High/ Low | $t_{MCH}$, $t_{MCL}$ | | $t_{MCK}/2$ - 35 | | | ns |
| MOSI Output Hold Time After SCLK Sample Edge | $t_{MOH}$ | | $t_{MCK}/2$ - 35 | | | ns |
| MOSI Output Valid to Sample Edge | $t_{MOV}$ | | $t_{MCK}/2$ - 35 | | | ns |
| MISO Input Valid to SCLK Sample Edge Rise/Fall Setup | $t_{MIS}$ | | 35 | | | ns |
| MISO Input to SCLK Sample Edge Rise/Fall Hold | $t_{MIH}$ | | 0 | | | ns |
| SCLK Input Pulse-Width High/Low | $t_{SCH}$, $t_{SCL}$ | | | $t_{SCK}/2$ | | ns |
| SSEL Active to First Shift Edge | $t_{SSE}$ | | | 50 | | ns |
| MOSI Input to SCLK Sample Edge Rise/Fall Setup | $t_{SIS}$ | | 35 | | | ns |
| MOSI Input from SCLK Sample Edge Transition Hold | $t_{SIH}$ | | 35 | | | ns |
| MISO Output Valid After SCLK Shift Edge Transition | $t_{SOV}$ | | | | 70 | ns |
| SCLK Inactive to SSEL Rising | $t_{SD}$ | | 35 | | | ns |

## SPI Timing Diagrams

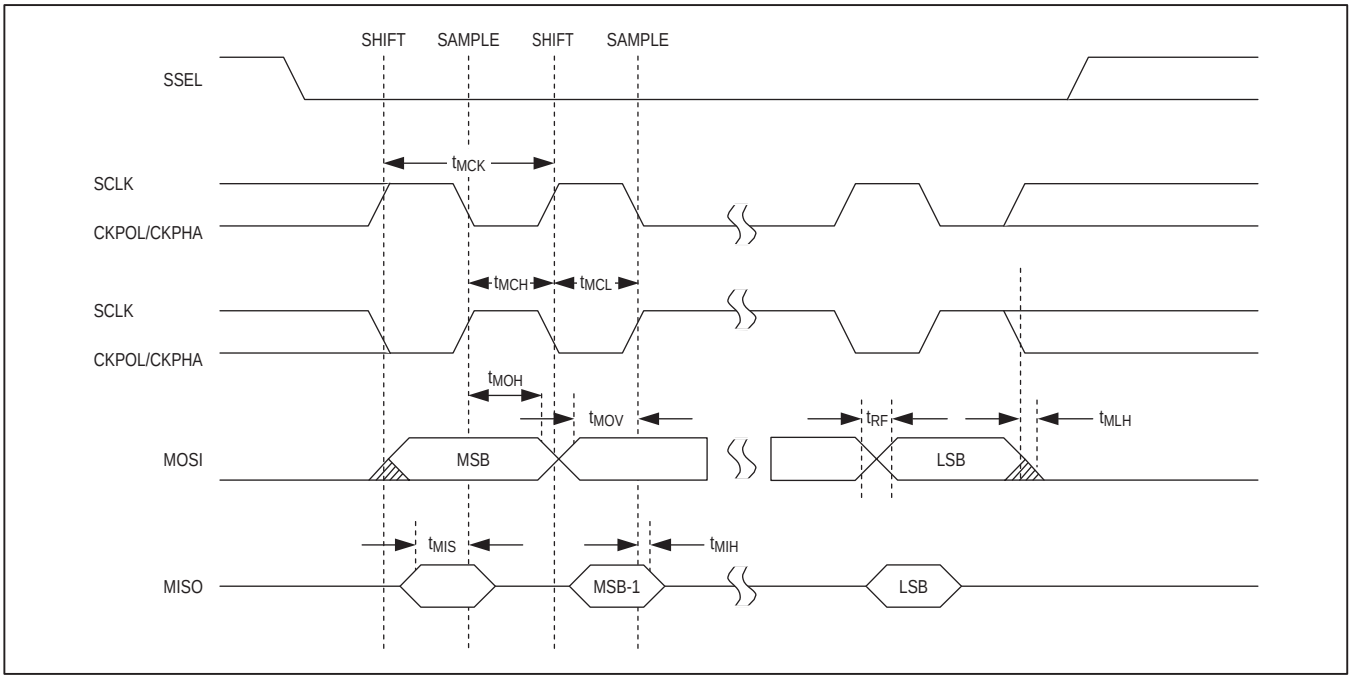



*Figure 3. SPI Master Communication Timing*

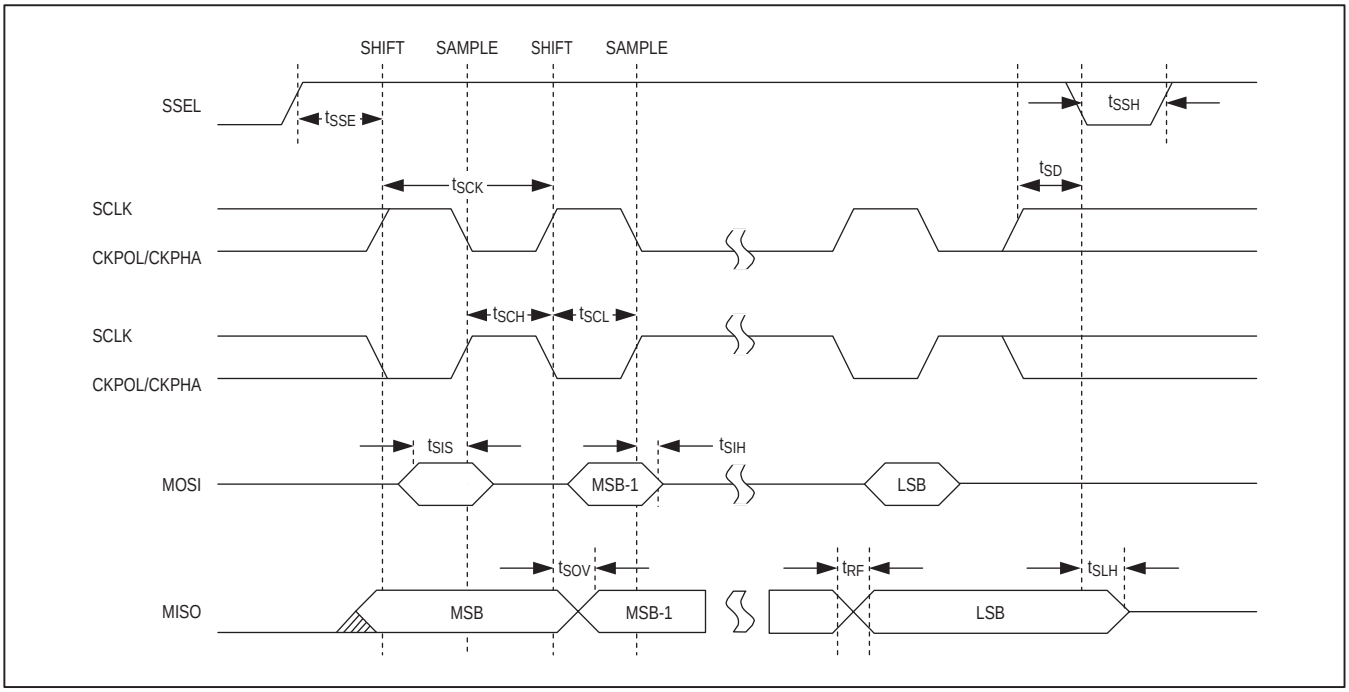



*Figure 4. SPI Slave Communication Timing*

## REVISION HISTORY

| REVISION | DATE | DESCRIPTION OF CHANGES |
|---|---|---|
| 1.0 | 19 SEP/2016 | First creation. |
| | | |
| | | |