

Document Title

256Kx16 Bit High Speed Static RAM(5V Operating), Revolutionary Pin out.  
Operated at Commercial, Extended and Industrial Temperature Ranges.

Revision History

RevNo.	History	Draft Data	Remark																					
Rev. 0.0	Initial release with Design Target.	Jun. 14th, 1996	Design Target																					
Rev. 0.5	Release to Preliminary Data Sheet. 0.1. Replace Design Target to Preliminary. 0.2. Delete 12ns part but add 17ns part. 0.3. Relax D.C and A.C parameters and insert new parameter(Icc1) with the test condition. 0.3.1. Insert Icc1 parameter with the test condition as address is increased with binary count. 0.3.2. Relax D.C and A.C parameters. <table><tr><td>Items</td><td>Previous spec. (15/ - /20ns part)</td><td>Relaxed spec. (15/17/20ns part)</td></tr><tr><td>Icc</td><td>250/ - /240mA</td><td>280/275/270mA</td></tr><tr><td>tCW</td><td>10/ - /12ns</td><td>12/13/14ns</td></tr><tr><td>tAW</td><td>10/ - /12ns</td><td>12/13/14ns</td></tr><tr><td>tWP(OE=H)</td><td>10/ - /12ns</td><td>12/13/14ns</td></tr><tr><td>tWP1(OE=L)</td><td>12/ - /14ns</td><td>15/17/20ns</td></tr><tr><td>tdW</td><td>7/ - /9ns</td><td>8/ 9/10ns</td></tr></table>	Items	Previous spec. (15/ - /20ns part)	Relaxed spec. (15/17/20ns part)	Icc	250/ - /240mA	280/275/270mA	tCW	10/ - /12ns	12/13/14ns	tAW	10/ - /12ns	12/13/14ns	tWP(OE=H)	10/ - /12ns	12/13/14ns	tWP1(OE=L)	12/ - /14ns	15/17/20ns	tdW	7/ - /9ns	8/ 9/10ns	Sep. 16th, 1996	Preliminary
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Icc	250/ - /240mA	280/275/270mA																						
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tdW	7/ - /9ns	8/ 9/10ns																						
Rev. 1.0	Release to Final Data Sheet. 1.1. Delete Preliminary. 1.2. Delete Icc1 parameter with the test condition. 1.3. Update D.C parameters. <table><tr><td>Items</td><td>Previous spec. (15/17/20ns part)</td><td>Updated spec. (15/17/20ns part)</td></tr><tr><td>Icc</td><td>280/275/270mA</td><td>210/205/200mA</td></tr></table> 1.4. Add the test condition for VOH1 with Vcc=5V±5% at 25°C. 1.5. Add timing diagram to define tWP1 as "(Timing Wave Form of Write Cycle(OE=Low fixed))".	Items	Previous spec. (15/17/20ns part)	Updated spec. (15/17/20ns part)	Icc	280/275/270mA	210/205/200mA	Jun. 5th, 1997	Final															
Items	Previous spec. (15/17/20ns part)	Updated spec. (15/17/20ns part)																						
Icc	280/275/270mA	210/205/200mA																						
Rev.2.0	2.1 Add extended and industrial temperature range parts.	Feb. 25th, 1998	Final																					
Rev.2.1	Add 44-TSOP2 Package.	Dec. 14th, 1998	Final																					

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.



## 256K x 16 Bit High-Speed CMOS Static RAM

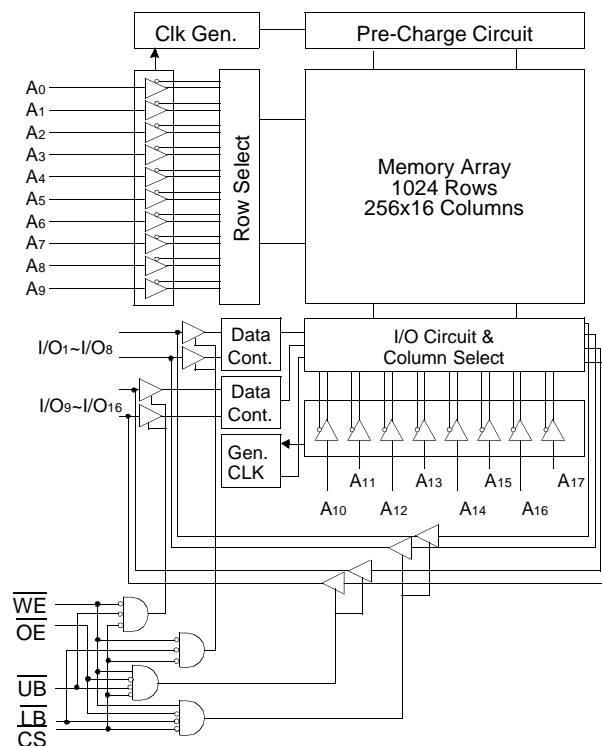
### FEATURES

- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM6164002A - 15 : 210mA(Max.)
  - KM6164002A - 17 : 205mA(Max.)
  - KM6164002A - 20 : 200mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Devices
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control ;  $\overline{LB}$ : I/O<sub>1</sub>~ I/O<sub>8</sub>,  $\overline{UB}$ : I/O<sub>9</sub>~ I/O<sub>16</sub>
- Standard Pin Configuration
  - KM6164002AJ : 44-SOJ-400
  - KM6164002AT : 44-TSOP2-400F

### ORDERING INFORMATION

KM6164002A-15/17/20	Commercial Temp.
KM6164002AE-15/17/20	Extended Temp.
KM6164002AI-15/17/20	Industrial Temp.

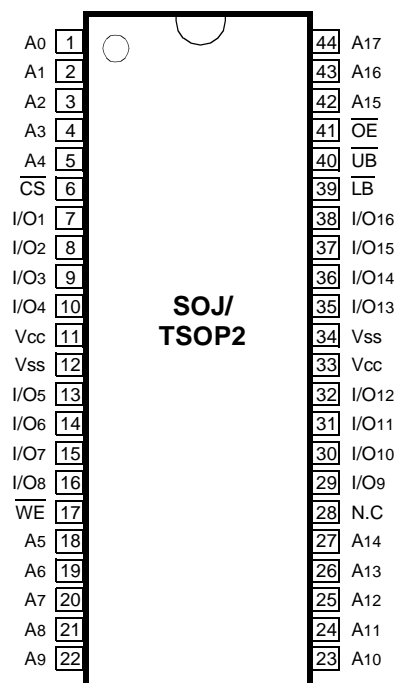
### FUNCTIONAL BLOCK DIAGRAM



### GENERAL DESCRIPTION

The KM6164002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM6164002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control( $\overline{UB}$ ,  $\overline{LB}$ ). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6164002A is packaged in a 400mil 44-pin plastic SOJ or TSOP(II) forward.

### PIN CONFIGURATION (Top View)



### PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O <sub>1</sub> ~I/O <sub>8</sub> )
$\overline{UB}$	Upper-byte Control(I/O <sub>9</sub> ~I/O <sub>16</sub> )
I/O <sub>1</sub> ~ I/O <sub>16</sub>	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

**ABSOLUTE MAXIMUM RATINGS\***

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V <sub>CC</sub>	-0.5 to 7.0	V
Power Dissipation		P <sub>D</sub>	1.0	W
Storage Temperature		T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	Commercial	T <sub>A</sub>	0 to 70	°C
	Extended	T <sub>A</sub>	-25 to 85	°C
	Industrial	T <sub>A</sub>	-40 to 85	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS\*(T<sub>A</sub>=0 to 70°C)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> + 0.5**	V
Input Low Voltage	V <sub>IL</sub>	-0.5*	-	0.8	V

\* The above parameters are also guaranteed at extended and industrial temperature ranges.

\*\* V<sub>IL</sub>(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA.

\*\*\* V<sub>IH</sub>(Max) = V<sub>CC</sub> + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA.

**DC AND OPERATING CHARACTERISTICS\*(T<sub>A</sub>=0 to 70°C, V<sub>CC</sub>=5.0V±10%, unless otherwise specified)**

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>		-2	2	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>		-2	2	μA
Operating Current	I <sub>CC</sub>	Min. Cycle, 100% Duty $\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	15ns	-	210	mA
			17ns	-	205	
			20ns	-	200	
Standby Current	I <sub>SB</sub>	Min. Cycle, $\overline{CS}=V_{IH}$		-	50	mA
	I <sub>SB1</sub>	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V		-	10	
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> =8mA		-	0.4	V
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> =-4mA		2.4	-	V

\* The above parameters are also guaranteed at extended and industrial temperature ranges.

**CAPACITANCE\*(T<sub>A</sub>=25°C, f=1.0MHz)**

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	-	8	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	7	pF

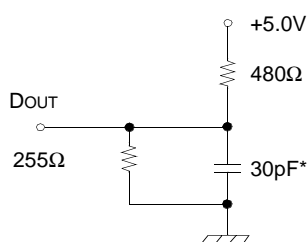
\* Capacitance is sampled and not 100% tested.

**AC CHARACTERISTICS**( $T_A=0$  to  $70^\circ\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 10\%$ , unless otherwise noted.)**TEST CONDITIONS\***

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

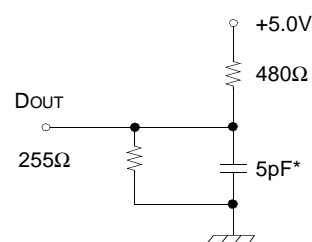
\* The above parameters are also guaranteed at extended and industrial temperature ranges.

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ &amp; tOHZ



\* Including Scope and Jig Capacitance

**READ CYCLE\***

Parameter	Symbol	KM6164002A-15		KM6164002A-17		KM6164002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	15	-	17	-	20	-	ns
Address Access Time	t <sub>AA</sub>	-	15	-	17	-	20	ns
Chip Select to Output	t <sub>CO</sub>	-	15	-	17	-	20	ns
Output Enable to Valid Output	t <sub>OE</sub>	-	7	-	8	-	9	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Access Time	t <sub>BA</sub>	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	t <sub>LZ</sub>	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	0	-	0	-	0	-	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Enable to Low-Z Output	t <sub>BLZ</sub>	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t <sub>HZ</sub>	0	7	0	8	0	9	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	7	0	8	0	9	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Disable to High-Z Output	t <sub>BHZ</sub>	0	7	0	8	0	9	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	ns

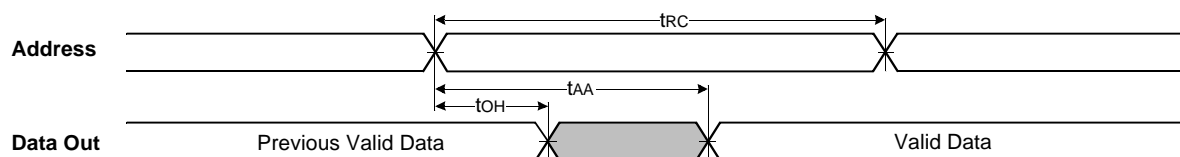
\* The above parameters are also guaranteed at extended and industrial temperature ranges.

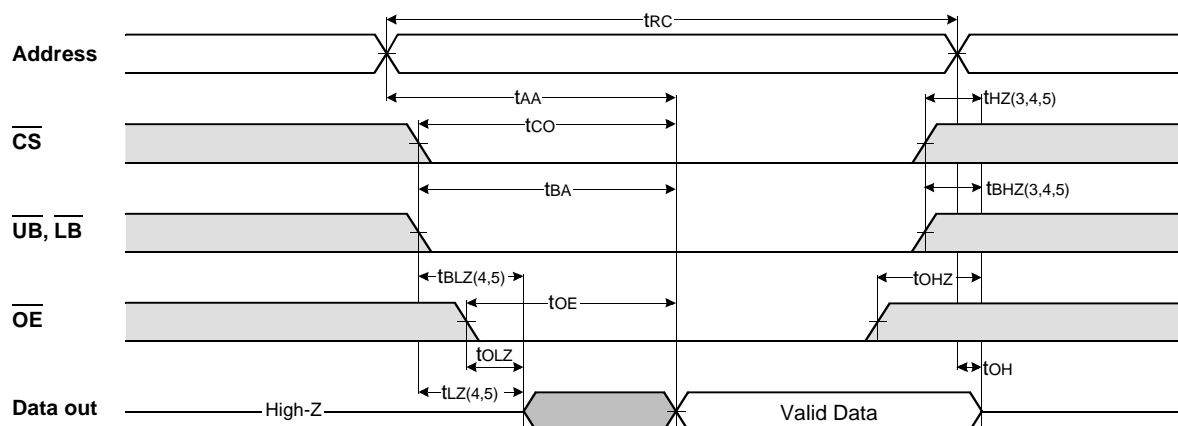
## WRITE CYCLE\*

Parameter	Symbol	KM6164002A-15		KM6164002A-17		KM6164002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width( $\overline{\text{OE}}$ High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width( $\overline{\text{OE}}$ Low)	tWP1	15	-	17	-	20	-	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Valid to End of Write	tBW	12	-	13	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tdW	8	-	9	-	10	-	ns
Data Hold from Write Time	tdH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

\* The above parameters are also guaranteed at extended and industrial temperature ranges.

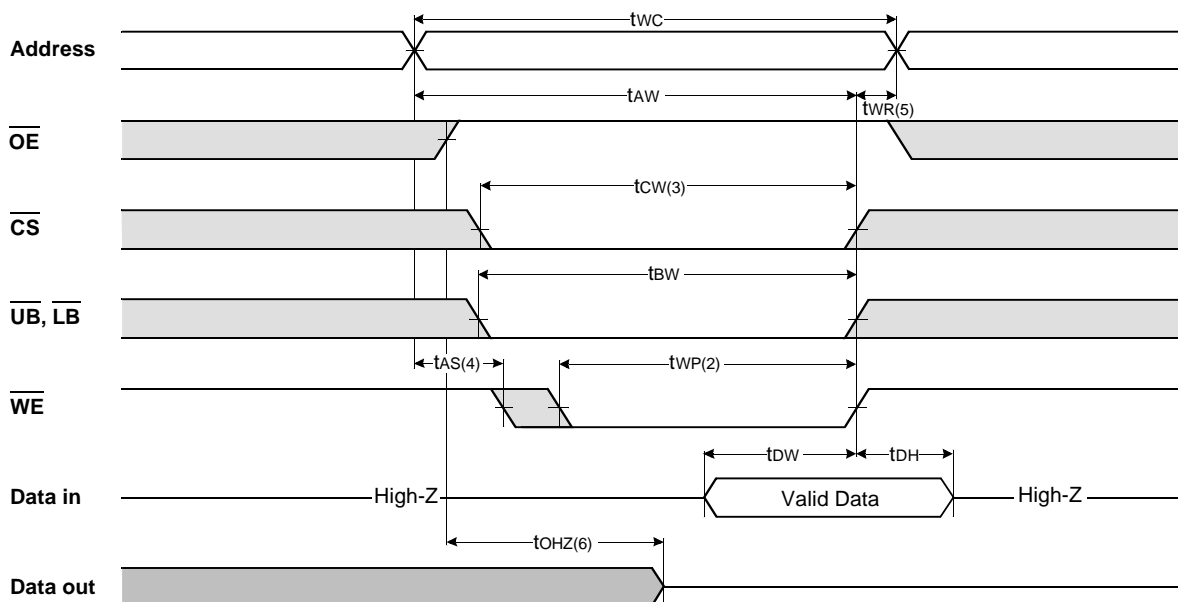
## TIMMING DIAGRAMS

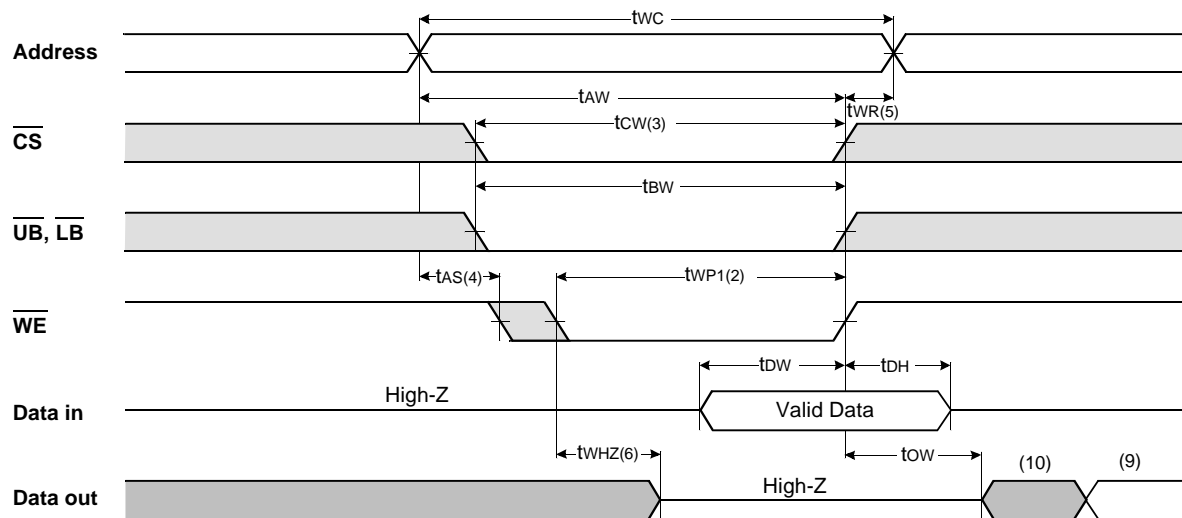
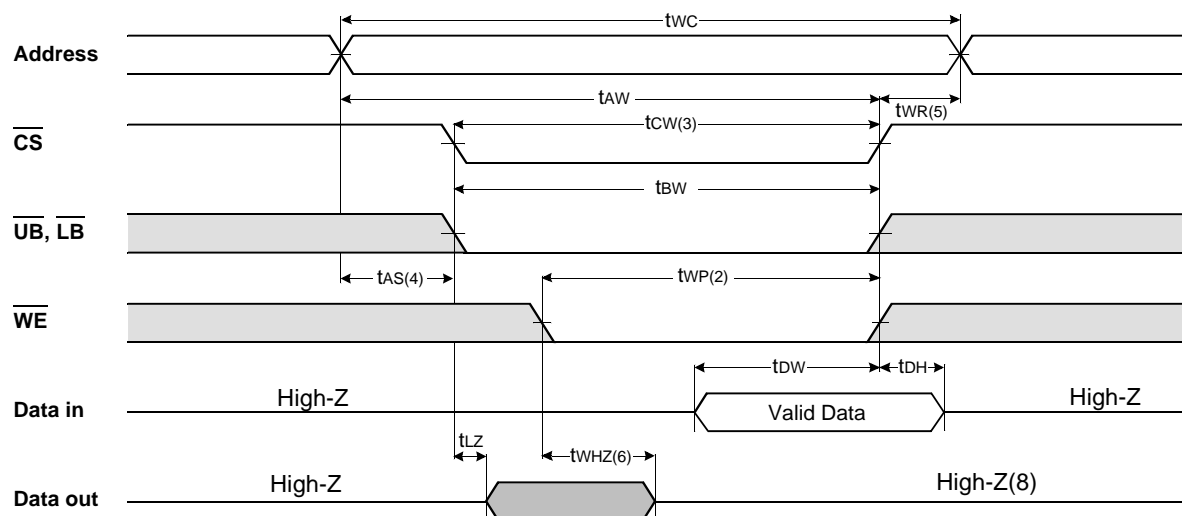
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{\text{CS}}=\overline{\text{OE}}=V_{\text{IL}}$ ,  $\overline{\text{WE}}=V_{\text{IH}}$ ,  $\overline{\text{UB}}$ ,  $\overline{\text{LB}}=V_{\text{IL}}$ )

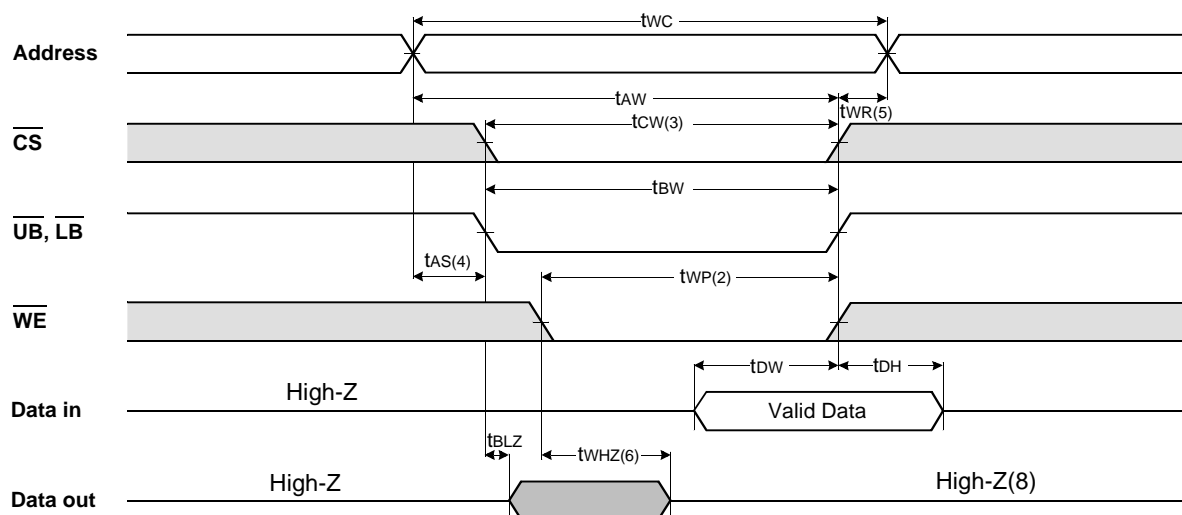
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )

## NOTES(READ CYCLE)

1.  $\overline{WE}$  is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device.
5. Transition is measured  $\pm 200\text{mV}$  from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CS}=V_{IL}$ .
7. Address valid prior to coincident with  $\overline{CS}$  transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}$  Clock)

TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{OE}$  = Low fixed)TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{CS}$  = Controlled)

TIMING WAVEFORM OF WRITE CYCLE(4) ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)

## NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low  $\overline{CS}$ ,  $\overline{WE}$ ,  $\overline{LB}$  and  $\overline{UB}$ . A write begins at the latest transition  $\overline{CS}$  going low and  $\overline{WE}$  going low; A write ends at the earliest transition  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
3.  $t_{CW}$  is measured from the later of  $\overline{CS}$  going low to end of write.
4.  $t_{AS}$  is measured from the address valid to the beginning of write.
5.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.
6. If  $\overline{OE}$ ,  $\overline{CS}$  and  $\overline{WE}$  are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If  $\overline{CS}$  goes low simultaneously with  $\overline{WE}$  going or after  $\overline{WE}$  going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When  $\overline{CS}$  is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

## FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	Icc
L	X	X	H	H	Read	DOUT	High-Z	Icc
L	H	L	L	H		High-Z	DOUT	
L	H	L	H	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	Icc
L	L	X	H	L		High-Z	DIN	
L	L	X	L	L		DIN	DIN	

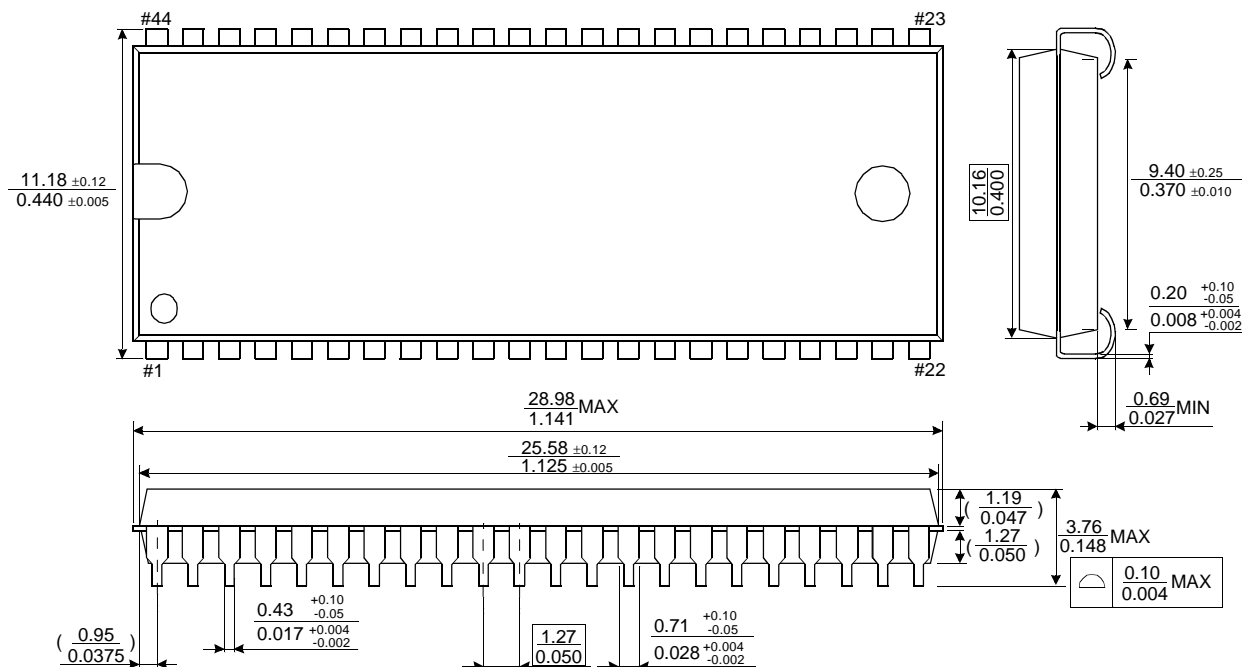
\* X means Don't Care.



## PACKAGE DIMENSIONS

Units: millimeters/Inches

## 44-SOJ-400



## 44-TSOP2-400F

