8XC196MH INDUSTRIAL MOTOR CONTROL CHMOS MICROCONTROLLER

- **High Performance CHMOS 16-bit CPU**
- **16 MHz Operating Frequency**
- **32 Kbytes of On-chip OTPROM/ROM**
- **744 Bytes of On-chip Register RAM**
- **Register-to-register Architecture**
- **16 Prioritized Interrupt Sources**
- **Peripheral Transaction Server (PTS) with 15 Prioritized Sources**
- **Up to 52 I/O Lines**
- **3-phase Complementary Waveform Generator**
- **8-channel 8- or 10-bit A/D with Sample and Hold**
- **2-channel UART**
- **Event Processor Array (EPA) with 2 High-speed Capture/Compare Modules and 4 High-speed Compare-only Modules**
- **Two Programmable 16-bit Timers with Quadrature Counting Inputs**
- **Two Pulse-width Modulator (PWM) Outputs with High Drive Capability**
- **Flexible 8- or 16-bit External Bus**
- **1.75 µs 16 × 16 Multiply**
- **3 µs 32/16 Divide**
- **Extended Temperature Available**
- **Idle and Powerdown Modes**
- **Watchdog Timer**

The 8XC196MH is a member of Intel's family of 16-bit MCS® 96 microcontrollers. It is designed primarily to control three-phase AC induction and DC brushless motors. It features an enhanced three-phase waveform generator specifically designed for use in "inverter" motor-control applications. This peripheral provides pulse-width modulation and three-phase sine wave generation with minimal CPU intervention. It generates three complementary non-overlapping PWM pulses with resolutions of 0.125 µs (edge triggered) or 0.250 µs (centered).

The 8XC196MH has two dedicated serial port peripherals, allowing less software overhead. The watchdog timer can be programmed with one of four time options.

The 8XC196MH is available as the 80C196MH, which does not have on-chip ROM, the 87C196MH, which contains 32 Kbytes of on-chip OTPROM* or factory programmed ROM, and the 83C196MH, which contains 32 Kbytes of factory programmed MASK ROM. It is available in 84-lead PLCC, 80-lead Shrink EIAJ/QFP, and 64-lead SDIP. The 64-lead package does not contain pins for the P5.1/INST and P6.7/PWM1 signals.

Operational characteristics are guaranteed over the temperature range of – 40°C to + 85°C.

*One-Time Programmable Read-Only Memory (OTPROM) is similar to EPROM but comes in an unwindowed package and cannot be erased. It is user programmable.

May 2002 Order Number: 272543-002

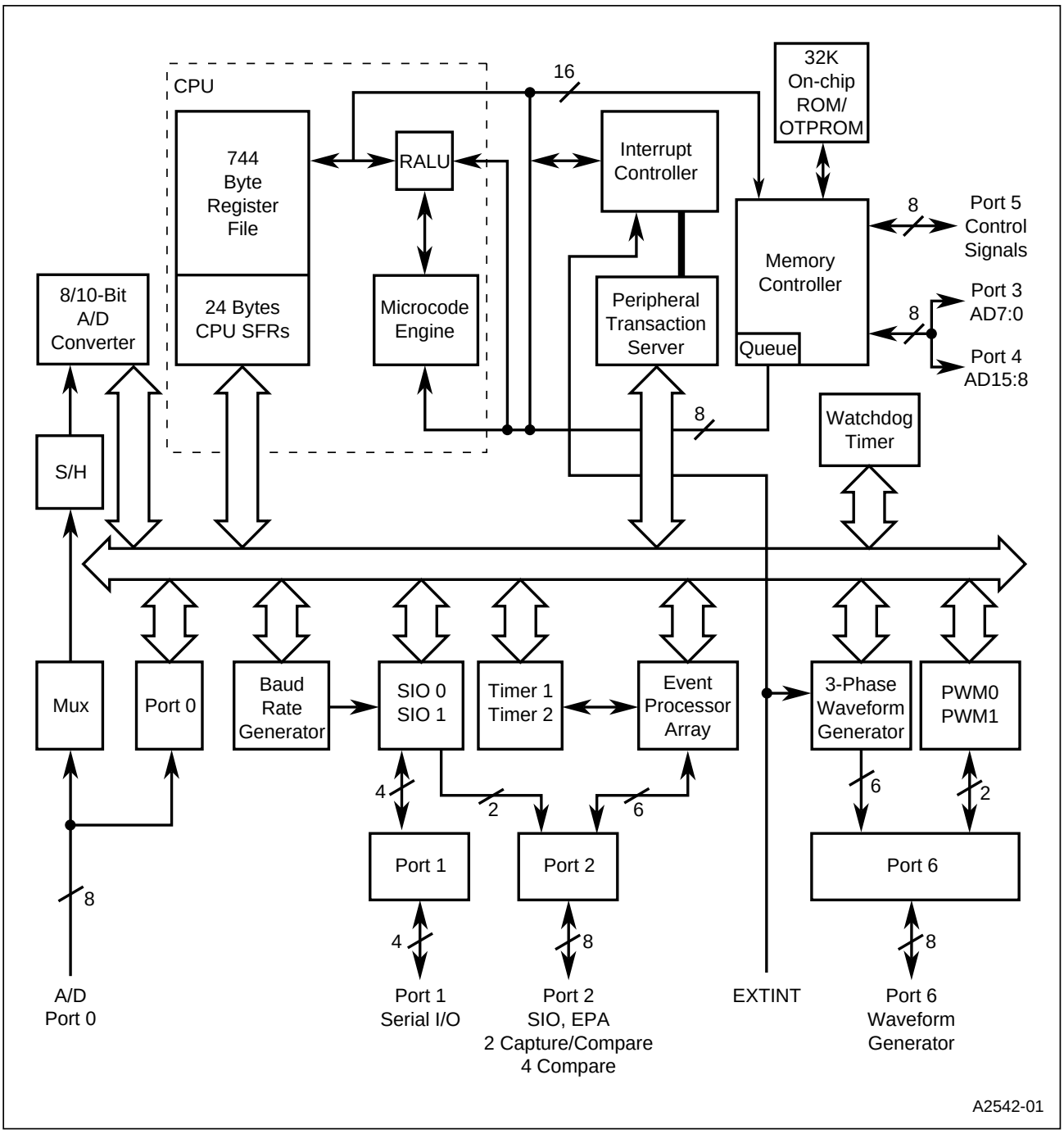


Figure 1. 8XC196MH Block Diagram

PROCESS INFORMATION

This device is manufactured on PX29.5, a CHMOS IV process. Additional process and reliability information is available in Intel's *Components Quality and Reliability* Handbook (order number 210997).

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values will change depending on operating conditions and the application. The Intel *Packaging* Handbook (order number 240800) describes Intel's thermal impedance test methodology.

Table 1. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
84-lead PLCC	33°C/W	11°C/W
80-lead QFP	56°C/W	12°C/W
64-lead SDIP	56°C/W	N/A

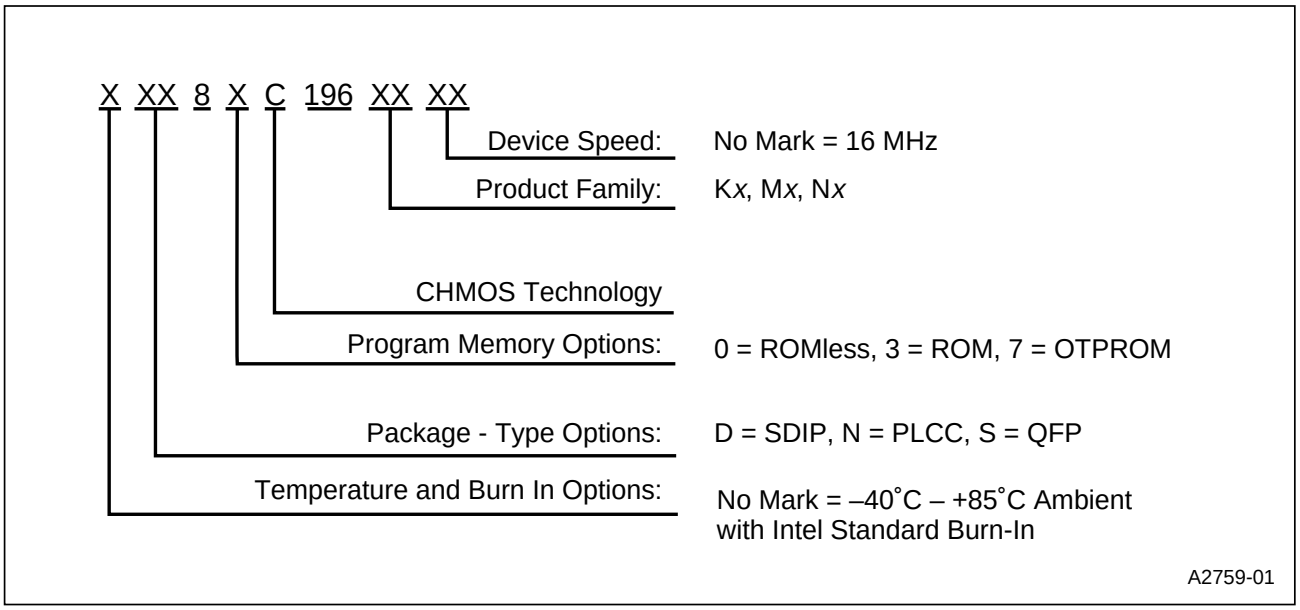


Figure 2. The 8XC196MH Family Nomenclature

Table 2. 8XC196MH Memory Map

Address (1)	Description	Notes
0FFFFH 0A000H	External Memory	
09FFFH 02080H	Internal ROM/OTPROM or External Memory	
0207FH 0205EH	Reserved	1, 2
0205DH 02040H	PTS Vectors	
0203FH 02030H	Interrupt Vectors (upper)	
0202FH 02020H	ROM/OTPROM Security Key	
0201FH 0201CH	Reserved	1, 2
0201BH	Reserved (must contain 20H)	
0201AH	CCB1	
02019H	Reserved (must contain 20H)	
02018H	CCB0	
02017H 02014H	Reserved	
02013H 02000H	Interrupt Vectors (lower)	
01FFFH 01F00H	Internal SFRs	1
1EFFH 300H	External Memory	
2FFH 18H	Register RAM	3
17H 00H	CPU SFRs	1

NOTES:
1. Unless otherwise noted, write 0FFH to reserved memory locations and write 0 to reserved SFR bits.
2. **WARNING:** The contents and/or function of reserved locations may change with future revisions of the device.
3. Code executed in locations 0000H to 02FFH will be forced external.

Table 3. Signals Arranged by Functional Categories

Address & Data
AD15:0

Bus Control & Status
ALE/ADV#
BHE#/WRH#
BUSWIDTH
INST
READY
RD#
WR#/WRL#

Power & Ground
ANGND
V_{CC}
V_{PP}
V_{REF}
V_{SS}

Programming Control
AINC#
CPVER
PACT#
PALE#
PBUS15:0
PMODE.3:0
PROG#
PVER

Processor Control
EA#
EXTINT
NMI
ONCE#
RESET#
XTAL1
XTAL2

Input/Output
P0.0/ACH0
P0.1/ACH1
P0.2/ACH2
P0.3/ACH3
P0.4/ACH4
P0.5/ACH5
P0.6/ACH6/T1CLK
P0.7/ACH7/T1DIR
P1.0/TXD0
P1.1/RXD0
P1.2/TXD1
P1.3/RXD1
P2.0/EPA0
P2.1/SCLK0#/BCLK0
P2.2/EPA1
P2.3/COMP3
P2.4/COMP0

Input/Output (Cont'd)
P2.5/COMP1
P2.6/COMP2
P2.7/SCLK1#/BCLK1
P3.7:0
P4.7:0
P5.7:0
P6.0/WG1#
P6.1/WG1
P6.2/WG2#
P6.3/WG2
P6.4/WG3#
P6.5/WG3
P6.6/PWM0
P6.7/PWM1

NOTE: The following signals are not available in the 64-pin package: P5.1, P6.7, INST, and PWM1.

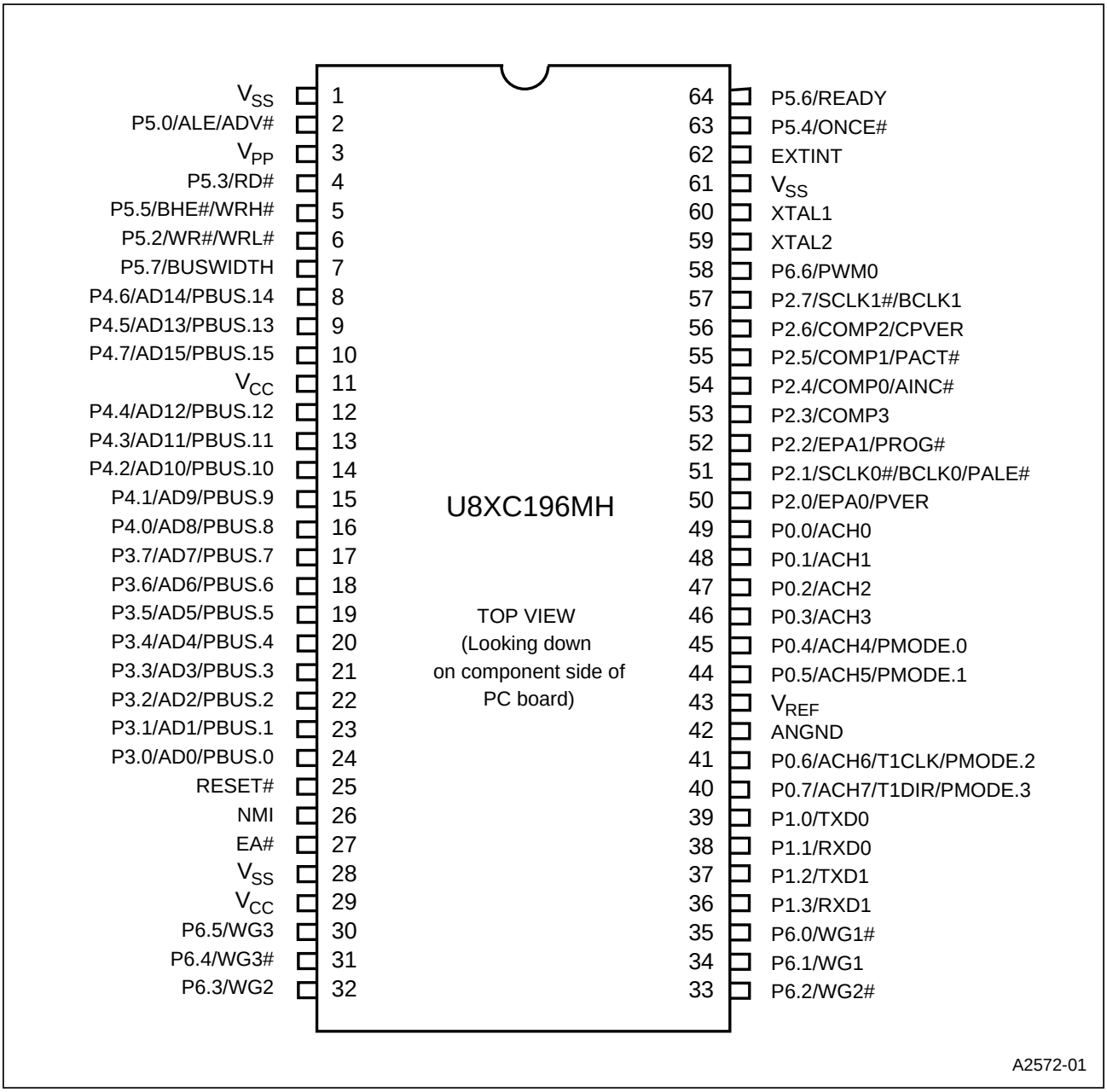


Figure 3. 8XC196MH 64-lead Shrink DIP (SDIP) Package

Table 4. 64-lead Shrink DIP (SDIP) Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	17	P3.7/AD7 /PBUS.7	33	P6.2/WG2#	49	P0.0/ACH0
2	P5.0/ALE/ADV#	18	P3.6/AD6 /PBUS.6	34	P6.1/WG1	50	P2.0/EPA0/PVER
3	V_{PP}	19	P3.5/AD5 /PBUS.5	35	P6.0/WG1#	51	P2.1/SCLK0# /BCLK0/PALE#
4	P5.3/RD#	20	P3.4/AD4 /PBUS.4	36	P1.3/RXD1	52	P2.2/EPA1 /PROG#
5	P5.5/BHE#/WRH#	21	P3.3/AD3 /PBUS.3	37	P1.2/TXD1	53	P2.3/COMP3
6	P5.2/WR#/WRL#	22	P3.2/AD2 /PBUS.2	38	P1.1/RXD0	54	P2.4/COMP0 /AINC#
7	P5.7/BUSWIDTH	23	P3.1/AD1 /PBUS.1	39	P1.0/TXD0	55	P2.5/COMP1 /PACT#
8	P4.6/AD14 /PBUS.14	24	P3.0/AD0 /PBUS.0	40	P0.7/ACH7/T1DIR /PMODE.3	56	P2.6/COMP2 /CPVER
9	P4.5/AD13 /PBUS.13	25	RESET#	41	P0.6/ACH6 /T1CLK/PMODE.2	57	P2.7/SCLK1# /BCLK1
10	P4.7/AD15 /PBUS.15	26	NMI	42	ANGND	58	P6.6/PWM0
11	V_{CC}	27	EA#	43	V_{REF}	59	XTAL2
12	P4.4/AD12 /PBUS.12	28	V_{SS}	44	P0.5/ACH5 /PMODE.1	60	XTAL1
13	P4.3/AD11 /PBUS.11	29	V_{CC}	45	P0.4/ACH4 /PMODE.0	61	V_{SS}
14	P4.2/AD10 /PBUS.10	30	P6.5/WG3	46	P0.3/ACH3	62	EXTINT
15	P4.1/AD9/PBUS.9	31	P6.4/WG3#	47	P0.2/ACH2	63	P5.4/ONCE#
16	P4.0/AD8/PBUS.8	32	P6.3/WG2	48	P0.1/ACH1	64	P5.6/READY

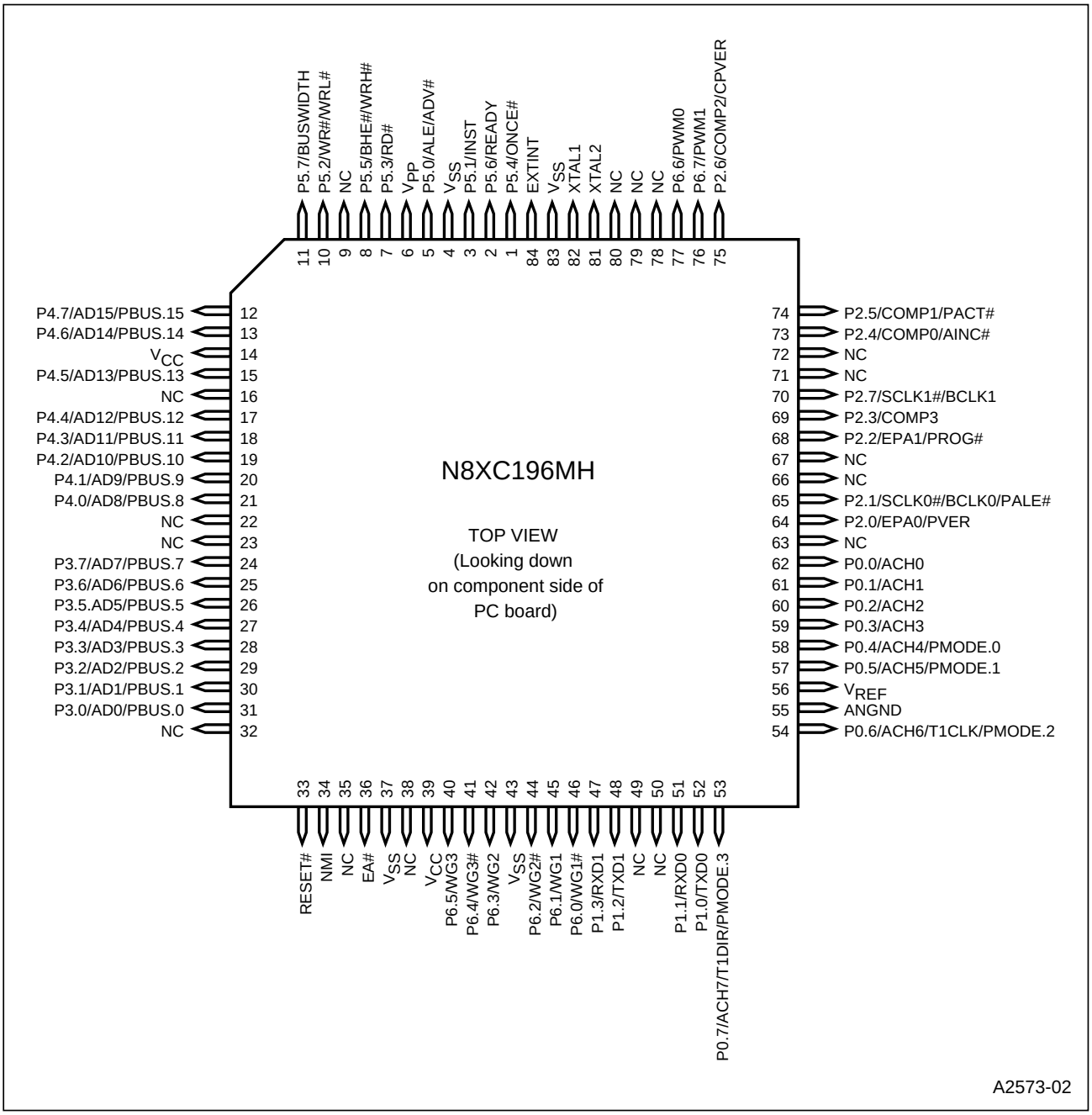


Figure 4. 8XC196MH 84-lead PLCC Package

Table 5. 84-lead PLCC Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	P5.4/ONCE#	22	NC	43	V_{SS}	64	P2.0/EPA0/PVER
2	P5.6/READY	23	NC	44	P6.2/WG2#	65	P2.1/SCLK0# /BCLK0/PALE#
3	P5.1/INST	24	P3.7/AD7 /PBUS.7	45	P6.1/WG1	66	NC
4	V_{SS}	25	P3.6/AD6 /PBUS.6	46	P6.0/WG1#	67	NC
5	P5.0/ALE/ADV#	26	P3.5/AD5 /PBUS.5	47	P1.3/RXD1	68	P2.2/EPA1 /PROG#
6	V_{PP}	27	P3.4/AD4 /PBUS.4	48	P1.2/TXD1	69	P2.3/COMP3
7	P5.3/RD#	28	P3.3/AD3 /PBUS.3	49	NC	70	P2.7/SCLK1# /BCLK1
8	P5.5/BHE#/WRH#	29	P3.2/AD2 /PBUS.2	50	NC	71	NC
9	NC	30	P3.1/AD1 /PBUS.1	51	P1.1/RXD0	72	NC
10	P5.2/WR#/WRL#	31	P3.0/AD0 /PBUS.0	52	P1.0/TXD0	73	P2.4/COMP0 /AINC#
11	P5.7/BUSWIDTH	32	NC	53	P0.7/ACH7 /T1DIR/PMODE.3	74	P2.5/COMP1 /PACT#
12	P4.7/AD15 /PBUS.15	33	RESET#	54	P0.6/ACH6 /T1CLK/PMODE.2	75	P2.6/COMP2 /CPVER
13	P4.6/AD14 /PBUS.14	34	NMI	55	ANGND	76	P6.7/PWM1
14	V_{CC}	35	NC	56	V_{REF}	77	P6.6/PWM0
15	P4.5/AD13 /PBUS.13	36	EA#	57	P0.5/ACH5 /PMODE.1	78	NC
16	NC	37	V_{SS}	58	P0.4/ACH4 /PMODE.0	79	NC
17	P4.4/AD12 /PBUS.12	38	NC	59	P0.3/ACH3	80	NC
18	P4.3/AD11 /PBUS.11	39	V_{CC}	60	P0.2/ACH2	81	XTAL2
19	P4.2/AD10 /PBUS.10	40	P6.5/WG3	61	P0.1/ACH1	82	XTAL1
20	P4.1/AD9/PBUS.9	41	P6.4/WG3#	62	P0.0/ACH0	83	V_{SS}
21	P4.0/AD8/PBUS.8	42	P6.3/WG2	63	NC	84	EXTINT

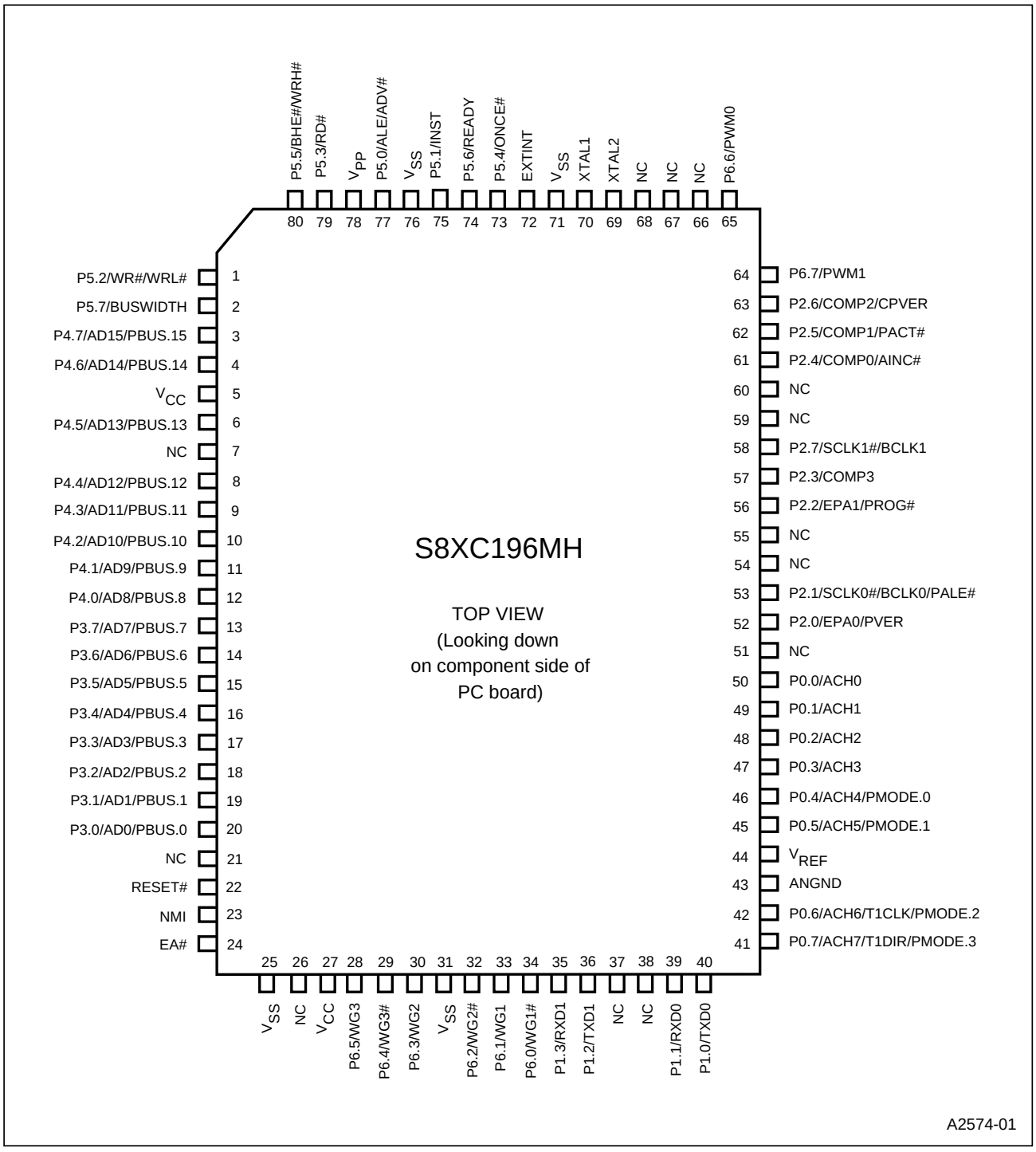


Figure 5. 8XC196MH 80-lead Shrink EIAJ/QFP Package

Table 6. 80-lead Shrink EIAJ/QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	P5.2/WR#/WRL#	21	NC	41	P0.7/ACH7/T1DIR /PMODE.3	61	P2.4/COMP0 /AINC#
2	P5.7/BUSWIDTH	22	RESET#	42	P0.6/ACH6 /T1CLK/PMODE.2	62	P2.5/COMP1 /PACT#
3	P4.7/AD15 /PBUS.15	23	NMI	43	ANGND	63	P2.6/COMP2 /CPVER
4	P4.6/AD14 /PBUS.14	24	EA#	44	V_{REF}	64	P6.7/PWM1
5	V_{CC}	25	V_{SS}	45	P0.5/ACH5 /PMODE.1	65	P6.6/PWM0
6	P4.5/AD13 /PBUS.13	26	NC	46	P0.4/ACH4 /PMODE.0	66	NC
7	NC	27	V_{CC}	47	P0.3/ACH3	67	NC
8	P4.4/AD12 /PBUS.12	28	P6.5/WG3	48	P0.2/ACH2	68	NC
9	P4.3/AD11 /PBUS.11	29	P6.4/WG3#	49	P0.1/ACH1	69	XTAL2
10	P4.2/AD10 /PBUS.10	30	P6.3/WG2	50	P0.0/ACH0	70	XTAL1
11	P4.1/AD9/PBUS.9	31	V_{SS}	51	NC	71	V_{SS}
12	P4.0/AD8/PBUS.8	32	P6.2/WG2#	52	P2.0/EPA0/PVER	72	EXTINT
13	P3.7/AD7/PBUS.7	33	P6.1/WG1	53	P2.1/SCLK0# /BCLK0/PALE#	73	P5.4/ONCE#
14	P3.6/AD6/PBUS.6	34	P6.0/WG1#	54	NC	74	P5.6/READY
15	P3.5/AD5/PBUS.5	35	P1.3/RXD1	55	NC	75	P5.1/INST
16	P3.4/AD4/PBUS.4	36	P1.2/TXD1	56	P2.2/EPA1 /PROG#	76	V_{SS}
17	P3.3/AD3/PBUS.3	37	NC	57	P2.3/COMP3	77	P5.0/ALE/ADV#
18	P3.2/AD2/PBUS.2	38	NC	58	P2.7/SCLK1# /BCLK1	78	V_{PP}
19	P3.1/AD1/PBUS.1	39	P1.1/RXD0	59	NC	79	P5.3/RD#
20	P3.0/AD0/PBUS.0	40	P1.0/TXD0	60	NC	80	P5.5/BHE#/WRH#

PIN DESCRIPTIONS

Table 7. Signal Descriptions

Signal Name	Type	Description	Multiplexed With
ACH7 ACH6 ACH5 ACH4 ACH3:0	I	**Analog Channels**. These pins are analog inputs to the A/D converter. These pins are multiplexed with the port 0 pins. While it is possible for the pins to function simultaneously as analog and digital inputs, this is not recommended because reading the port while a conversion is in process can produce unreliable conversion results. The ANGND and V_{REF} pins must be connected for the A/D converter and the multiplexed port pins to function.	P0.7/T1DIR/PMODE.3 P0.6/T1CLK/PMODE.2 P0.5/PMODE.1 P0.4/PMODE.0 P0.3:0
AD15:8 AD7:0	I/O	**Address/Data Lines**. These pins provide a multiplexed address and data bus. During the address phase of the bus cycle, address bits 0–15 are presented on the bus and can be latched using ALE or ADV#. During the data phase, 8- or 16-bit data is transferred.	P4.7:0/PBUS.15:8 P3.7:0/PBUS.7:0
ADV#	O	**Address Valid**. This active-low output signal is asserted only during external memory accesses. ADV# indicates that valid address information is available on the system address/data bus. The signal remains low while a valid bus cycle is in progress and is returned high as soon as the bus cycle completes. An external latch can use the ADV# signal to demultiplex the address from the address/data bus. Used with a decoder, ADV# can generate chip-selects for external memory.	P5.0/ALE
AINC#	I	**Auto Increment**. In slave programming mode, this active-low input signal enables the autoincrement mode. Auto increment allows reading from or writing to sequential OTPROM locations without requiring address transactions across the programming bus for each read or write.	P2.4/COMP0
ALE	O	**Address Latch Enable**. This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus. ALE differs from ADV# in that it is not returned high until a new bus cycle is to begin. An external latch can use ALE to demultiplex the address from the address/data bus.	P5.0/ADV#
ANGND	GND	**Analog Ground**. Reference ground for the A/D converter and the logic used to read port 0. ANGND must be held at nominally the same potential as V_{SS}.	—
BCLK1 BCLK0	I	**Serial Communications Baud Clock 0 and 1**. BCLK0 and 1 are alternate clock sources for the serial ports. The maximum input frequency is $F_{OSC}/4$.	P2.7/SCLK1# P2.1/SCLK0#/PALE#

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
BHE#	O	**Byte High Enable**. During 16-bit bus cycles, this active-low output signal is asserted for word reads and writes and for high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system address/data bus. BHE#, in conjunction with A0, selects the memory byte to be accessed: **BHE# A0 Byte(s) Accessed** 0 0 both bytes 0 1 high byte only 1 0 low byte only	P5.5/WRH#
BUSWIDTH	I	**Bus Width**. When enabled in the chip configuration register, this active-high input signal dynamically selects the bus width of the bus cycle in progress. When BUSWIDTH is high, a 16-bit bus cycle occurs; when BUSWIDTH is low, an 8-bit bus cycle occurs. BUSWIDTH is active during a CCR fetch.	P5.7
COMP3 COMP2 COMP1 COMP0	O	**Event Processor Array (EPA) Compare Pins**. These signals are the output of the EPA compare modules. These pins are multiplexed with other signals and may be configured as standard I/O.	P2.3 P2.6/CPVER P2.5/PACT# P2.4/AINC#
CPVER	O	**Cumulative Program Verification**. This active-high output signal indicates whether any verify errors have occurred since the device entered programming mode. CPVER remains high until a verify error occurs, at which time it is driven low. Once an error occurs, CPVER remains low until the device exits programming mode. When high, CPVER indicates that all locations have programmed correctly since the device entered programming mode.	P2.6/COMP2
EA#	I	**External Access**. This active-low input signal directs memory accesses to on-chip or off-chip memory. If EA# is low, the memory access is off-chip. If EA# is high and the memory address is within 2000H–2FFFH, the access is to on-chip ROM or OTPROM. Otherwise, an access with EA# high is to off-chip memory. EA# is sampled **only** on the rising edge of RESET#. If EA# = V_{EA} on the rising edge of RESET#, the device enters the programming mode selected by PMODE.3:0. For devices without ROM, EA# must be tied low.	—
EPA1 EPA0	I/O	**Event Processor Array (EPA) Input/Output pins**. These are the high-speed input/output pins for the EPA capture/compare modules. These pins are multiplexed with other signals and may be configured as standard I/O.	P2.2/PROG# P2.0/PVER

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
EXTINT	I	**External Interrupt**. This programmable interrupt is controlled by the WG_PROTECT register. This register controls whether the interrupt is edge triggered or sampled and whether a rising edge/high level or falling edge/low level activates the interrupt. This interrupt vectors through memory location 203CH. If the chip is in idle mode and if EXTINT is enabled, a valid EXTINT interrupt brings the chip back to normal operation, where the first action is to execute the EXTINT service routine. After completion of the service routine, execution resumes at the instruction following the one that put the chip into idle mode. In powerdown mode, a valid EXTINT interrupt causes the chip to return to normal operating mode. If EXTINT is enabled, the EXTINT service routine is executed. Otherwise, execution continues at the instruction following the IDLPD instruction that put the chip into powerdown mode.	—
INST	O	**Instruction Fetch**. This active-high output signal is valid only during external memory bus cycles. When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches.	P5.1
NMI	I	**Nonmaskable Interrupt**. In normal operating mode, a rising edge on NMI causes a vector through the NMI interrupt at location 203EH. NMI must be asserted for greater than one state time to guarantee that it is recognized. In idle mode, a rising edge on NMI brings the chip back to normal operation, where the first action is to execute the NMI service routine. After completion of the service routine, execution resumes at the instruction following the one that put the chip into idle mode. In powerdown mode, NMI causes a return to normal operating mode only if it is tied to EXTINT.	—
ONCE#	I	**On-circuit Emulation**. Holding this pin low while the RESET# signal transitions from a low to a high places the device into on-circuit emulation (ONCE) mode. ONCE mode isolates the device from other components in the system to allow the use of a clip-on emulator for system debugging. This mode puts all pins except XTAL1 and XTAL2 into a high-impedance state. To exit ONCE mode, reset the device by pulling the RESET# signal low.	P5.4

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
P0.7 P0.6 P0.5 P0.4 P0.3:0	I	**Port 0**. This is a high-impedance, input-only port. Port 0 pins should **not** be left floating. These pins may individually be used as analog inputs (ACH*x*) or digital inputs (P0.*x*). While it is possible for the pins to function simultaneously as analog and digital inputs, this is not recommended because reading port 0 while a conversion is in process can produce unreliable conversion results. ANGND and V_{REF} must be connected for port 0 and the A/D converter to function.	ACH7/T1DIR/PMODE.3 ACH6/T1CLK/PMODE.2 ACH5/PMODE.1 ACH4/PMODE.0 ACH3:0
P1.3 P1.2 P1.1 P1.0	I	**Port 1**. This is a 4-bit, bidirectional, standard I/O port that is multiplexed with individually selectable special-function signals. (Used as PBUS.15:12 in Auto-programming Mode.)	RXD1 TXD1 RXD0 TXD0
P2.7 P2.6 P2.5 P2.4 P2.3 P2.2 P2.1 P2.0	I/O	**Port 2**. This is an 8-bit, bidirectional, standard I/O port that is multiplexed with individually selectable special-function signals. P2.6 is multiplexed with a special test mode function. To prevent accidental entry into test modes, always configure P2.6 as an output.	SCLK1#/BCLK1 COMP2/CPVER COMP1/PACT# COMP0/AINC# COMP3 EPA1/PROG# SCLK0#/BCLK0/PALE# EPA0/PVER
P3.7:0	I/O	**Port 3**. This is an 8-bit, bidirectional, memory-mapped I/O port with open-drain outputs. The pins are shared with the multiplexed address/data bus, which has complementary drivers. In programming modes, port 3 serves as the low byte of the programming bus (PBUS).	AD7:0/PBUS.7:0
P4.7:0	I/O	**Port 4**. This is an 8-bit, bidirectional, memory-mapped I/O port with open-drain outputs. The pins are shared with the multiplexed address/data bus, which has complementary drivers. In programming modes, port 4 serves as the high byte of the programming bus (PBUS).	AD15:8/PBUS.15:8
P5.7 P5.6 P5.5 P5.4 P5.3 P5.2 P5.1 P5.0	I/O	**Port 5**. This is an 8-bit, bidirectional, standard I/O port that is multiplexed with individually selectable control signals. Because P5.4 is multiplexed with the ONCE# function, always configure it as an output to prevent accidental entry into ONCE mode.	BUSWIDTH READY BHE#/WRH# ONCE# RD# WR#/WRL# INST ALE/ADV#

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
P6.7 P6.6 P6.5 P6.4 P6.3 P6.2 P6.1 P6.0	O	**Port 6**. This is an 8-bit output port that is multiplexed with the special functions of the waveform generator and PWM peripherals. The WG_OUT register configures the pins, establishes the output polarity, and controls whether changes to the outputs are synchronized with an event or take effect immediately.	PWM1 PWM0 WG3 WG3# WG2 WG2# WG1 WG1#
PACT#	O	**Programming Active**. In auto-programming mode, PACT# low indicates that programming activity is occurring.	P2.5/COMP1
PALE#	I	**Programming ALE**. In slave programming mode, this active-low input indicates that ports 3 and 4 contain a command/address. When PALE# is asserted, data and commands on ports 3 and 4 are read into the device.	P2.1/SCLK0#/BCLK0
PBUS.15:8 PBUS.7:0	I/O	**Programming Bus**. In programming modes, used as a bidirectional port with open-drain outputs to pass commands, addresses, and data to or from the device. Used as a regular system bus to access external memory during auto-programming mode. When using slave programming mode, the PBUS is used in open-drain I/O port mode (not as a system bus). In slave programming mode, you must add external pull-up resistors to read data from the device during the dump word routine.	P4.7:0/AD15:8 P3.7:0/AD7:0
PMODE.3 PMODE.2 PMODE.1 PMODE.0	I	**Programming Mode Select**. Determines the OTPROM programming algorithm that is to be performed. PMODE is sampled after a device reset when EA# = V_{EA} and must be stable while the device is operating.	P0.7/ACH7/T1DIR P0.6/ACH6/T1CLK P0.5/ACH5 P0.4/ACH4
PROG#	I	**Programming Start**. This active-low input is valid only in slave programming mode. The rising edge of PROG# latches data on the PBUS and begins programming. The falling edge of PROG# ends programming.	P2.2/EPA1
PVER	O	**Program Verification**. In programming modes, this active-high output signal is asserted to indicate that the word has programmed correctly. (PVER low after the rising edge of PROG# indicates an error.)	P2.0/EPA0
PWM1:0	O	**Pulse Width Modulator Outputs**. These are PWM output pins with high-current drive capability. The duty cycle and frequency-pulse-widths are programmable.	P6.7:6
RD#	O	**Read**. Read-signal output to external memory. RD# is asserted only during external memory reads.	P5.3

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
READY	I	**Ready Input**. This active-high input signal is used to lengthen external memory cycles for slow memory by generating wait states. When READY is high, CPU operation continues in a normal manner. If READY is low, the memory controller inserts wait states until the READY signal goes high or until the number of wait states is equal to the number programmed into the chip configuration register. READY is ignored for all internal memory accesses.	P5.6
RESET#	I/O	**Reset**. Reset input to and open-drain output from the chip. A falling edge on RESET# initiates the reset process. When RESET# is first asserted, the chip turns on a pull-down transistor connected to the RESET pin for 16 state times. This function can also be activated by execution of the RST instruction. In the powerdown and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. RESET# is a level-sensitive input.	—
RXD1 RXD0	I/O	**Receive Serial Data 0 and 1**. In modes 1, 2, and 3, RXD0 and 1 are used to receive serial port data. In mode 0, they function as either inputs or open-drain outputs for data.	P1.3 P1.1
SCLK1# SCLK0#	I/O	**Synchronous Clock Pin 0 and 1**. In mode 4, these are the bidirectional, shift clock signals that synchronize the serial data transfer. Data is transferred 8 bits at a time with the LSB first. The DIR bit (SP_CON*x*.7) controls the direction of SCLK*x* signal. DIR = 0 The internal shift clock is output on SCLK*x*. DIR = 1 An external shift clock is input on SCLK*x*.	P2.7/BCLK1 P2.1/BCLK0
T1CLK	I	**External Clock**. External clock for timer 1. Timer 1 increments (or decrements) on both rising and falling edges of T1CLK. Also used in conjunction with T1DIR for quadrature counting mode.	P0.6/ACH6/PMODE.2
T1DIR	I	**Timer 1 External Direction**. External direction (up/down) for timer 1. Timer 1 increments when T1DIR is high and decrements when it is low. Also used in conjunction with T1CLK for quadrature counting mode.	P0.7/ACH7/PMODE.3
TXD1 TXD0	O	**Transmit Serial Data 0 and 1**. In serial I/O modes 1, 2, and 3, TXD0 and 1 are used to transmit serial port data. In mode 0, they are used as the serial clock output.	P1.2 P1.0
V_{CC}	PWR	**Digital Supply Voltage**. Connect each V_{CC} pin to the digital supply voltage.	—
V_{PP}	PWR	**Programming Voltage**. Set to 12.5 V when programming the on-chip OTPROM. Also the timing pin for the “return from power-down” circuit.	—

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
V_{REF}	PWR	**Reference Voltage for the A/D Converter**. V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. V_{REF} must be connected for the A/D and port 0 to function.	—
V_{SS}	GND	**Digital Circuit Ground** (0 volts). Connect each V_{SS} pin to ground.	—
WG3 WG2 WG1	O	**Waveform Generator Phase 1—3 Positive Outputs**. 3-phase output signals used in motion-control applications.	P6.5 P6.3 P6.1
WG3# WG2# WG1#	O	**Waveform Generator Phase 1—3 Negative Outputs**. Complementary 3-phase output signals used in motion-control applications.	P6.4 P6.2 P6.0
WR#	O	**Write**. This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes.	P5.2/WRL#
WRH#	O	**Write High**. During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations.	P5.5/BHE#
WRL#	O	**Write Low**. During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes. During 8-bit bus cycles, WRL# is asserted for all write operations.	P5.2/WR#
XTAL1	I	**Clock/Oscillator Input**. Input to the on-chip oscillator inverter and the internal clock generator. Also provides the clock input for the serial I/O baud-rate generator, timers, and PWM unit. If an external oscillator is used, connect the external clock input signal to XTAL1 and ensure that the XTAL1 V_{IH} specification is met.	—
XTAL2	O	**Oscillator Output**. Output of the on-chip oscillator inverter. When using the on-chip oscillator, connect XTAL2 to an external crystal or resonator. When using an external clock source, let XTAL2 float.	—

ELECTRICAL CHARACTERISTICS

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... – 65°C to + 150°C
Ambient Temperature
under Bias..... – 40°C to + 85°C
Voltage from V_{PP} or EA# to
V_{SS} or ANGND (Note 1) ..... – 0.5 V to + 13.0 V
Voltage with respect to
V_{SS} or ANGND (Note 1) ..... – 0.5 V to + 7.0 V
(This includes V_{PP} on ROM and CPU devices.)
Power Dissipation ..... 1.5 W
(based on package heat transfer limitations, not device power consumption)

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias) .....– 40°C to + 85°C
V_{CC} (Digital Supply Voltage) ..... 4.50 V to 5.50 V
V_{REF} (Analog Supply Voltage) ..... 4.50 V to 5.50 V
F_{OSC} (Oscillator Frequency) (Note 2) ..... 8 MHz to 16 MHz

NOTES:
1. ANGND and V_{SS} should be at nominally the same potential.
2. Testing is performed down to 8 MHz, although the device is static by design and will typically operate below 1 Hz.

DC CHARACTERISTICS

Table 8. DC Characteristics over Specified Operating Conditions

Symbol	Parameter	Min	Typ (4)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (standard inputs (1))	– 0.5		0.3 V_{CC}	V	
V_{IL1}	Input Low Voltage (RESET#, ports 3, 4, and 5)	– 0.5		0.8	V	
V_{IH}	Input High Voltage (standard inputs (1))	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (RESET#, ports 3, 4, and 5)	0.2 V_{CC} + 1.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (RESET#, ports 1, 2, 5, P6.6, P6.7, and XTAL2)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OL1}	Output Low Voltage (ports 3, 4)			1.0	V	I_{OL} = 7 mA
V_{OL2}	Output Low Voltage (P6.5:0)			0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (output pins and I/O configured as push/pull outputs)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = – 200 µA I_{OH} = – 3.2 mA I_{OH} = – 7.0 mA
$V_{TH+} – V_{TH–}$	Hysteresis voltage width on RESET# pin	0.2			V	
I_{LI}	Input Leakage Current (standard inputs (1))			± 10	µA	$V_{SS} < V_{IN} < V_{CC}$ – 0.3V
I_{LI1}	Input Leakage Current (port 0 – A/D inputs)			± 3	µA	$V_{SS} < V_{IN} < V_{REF}$
I_{IH}	Input High Current (NMI)			300	µA	V_{IN} = 0.7 V_{CC}
I_{IL}	Input Low Current (port 2, except P2.6)			– 70	µA	V_{IN} = 0.3 V_{CC}

NOTES:
1. Standard input pins include XTAL1, EA#, and Ports 1 and 2 when configured as inputs.
2. Maximum current that an external device must sink to ensure test mode entry.
3. Violating these specifications during reset may cause the device to enter test modes.
4. Typical values are based on a limited number of samples and are not guaranteed. Operating conditions for typical values are room temperature and $V_{REF} = V_{CC} = 5.5$ V.
5. Testing is performed down to 8 MHz, although the device is static by design and will typically operate below 1 Hz.
6. All voltages are referenced relative to V_{SS}. When used, V_{SS} refers to the device pin.
7. Table 9 lists the total current limits during normal (non-transient conditions). The total current listed is the sum of the pins listed for each specification value.

Table 8. DC Characteristics over Specified Operating Conditions (Continued)

Symbol	Parameter	Min	Typ (4)	Max	Units	Test Conditions
I_{IL1}	Input Low Current (P5.4 and P2.6 during reset) (2)			– 10	mA	V_{IN} = 0.8 V
I_{IL2}	Input Low Current (ports 3, 4, and 5, except P5.4)			– 300	µA	V_{IN} = 0.8 V
I_{IL3}	Input Low Current (port 1)			– 300	µA	V_{IN} = 0.3 V_{CC}
I_{OH}	Output High Current (P5.4 and P2.6 during reset) (3)	– 0.2			mA	0.7 V_{CC}
I_{OH1}	Output High Current (P6.5:0 during reset)	– 6		– 40	µA	0.7 V_{CC}
I_{CC}	V_{CC} Supply Current		50	70	mA	XTAL1 = 16 MHz V_{CC} = 5.5 V V_{PP} = 5.5 V V_{REF} = 5.5 V
I_{REF}	A/D Reference Supply Current		2	5	mA	
I_{IDLE}	Idle Mode Current		15	30	mA	
I_{PD}	Powerdown Mode Current (4)		5	50	µA	
R_{RST}	Reset Pull-up Resistor	6		65	kΩ	
C_S	Pin Capacitance (any pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:
1. Standard input pins include XTAL1, EA#, and Ports 1 and 2 when configured as inputs.
2. Maximum current that an external device must sink to ensure test mode entry.
3. Violating these specifications during reset may cause the device to enter test modes.
4. Typical values are based on a limited number of samples and are not guaranteed. Operating conditions for typical values are room temperature and V_{REF} = V_{CC} = 5.5 V.
5. Testing is performed down to 8 MHz, although the device is static by design and will typically operate below 1 Hz.
6. All voltages are referenced relative to V_{SS}. When used, V_{SS} refers to the device pin.
7. Table 9 lists the total current limits during normal (non-transient conditions). The total current listed is the sum of the pins listed for each specification value.

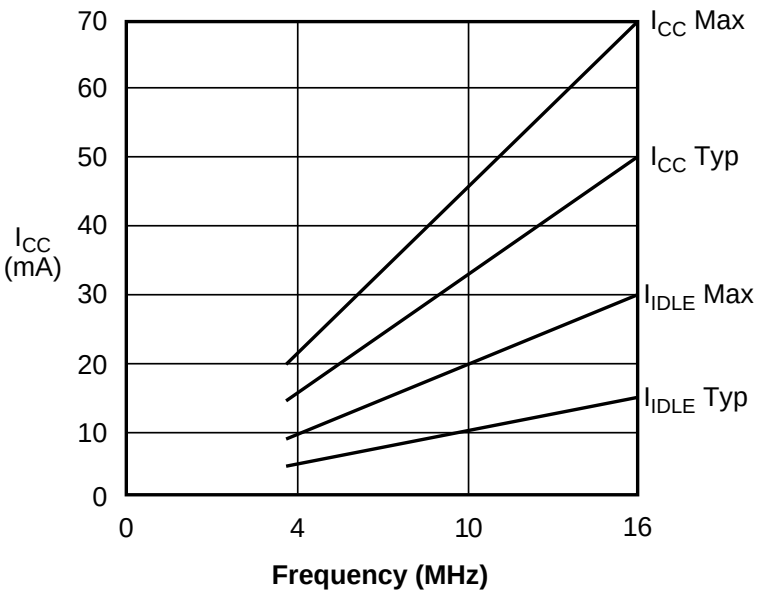


Table 9. Total Current Limits During Normal (Non-transient) Conditions

Signal Names	Maximum I_{OL} Limits	Maximum I_{OH} Limits
Port 1	25 mA	– 25 mA
Port 2, P6.6, P6.7	40 mA	– 40 mA
Port 3	40 mA	– 30 mA
Port 4	40 mA	– 30 mA
Port 5	40 mA	– 30 mA
P6.5:0	40 mA	– 30 mA

Figure 6. I_{CC}, I_{IDLE} versus Frequency

EXPLANATION OF AC SYMBOLS

Each symbol consists of two pairs of letters prefixed by "T" (for time). The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points. For example, T_{RHDZ} is the time between signal R (RD#) condition H (high) and signal D (Input Data) condition Z (floating). Table 10 defines the signal and condition codes.

Table 10. AC Timing Symbol Definitions

Signals				Conditions	
A	Address	P	PROG#	H	High
B	BHE#	Q	Data Out	L	Low
D	Data In	R	RD#	V	Valid
G	BUSWIDTH	V	PVER	X	No Longer Valid
I	T1DIR/AINC#	W	WR#/WRH#/WRL#	Z	Floating
K	T1CLK	X	XTAL1		
L	ALE/ADV#/PALE#	Y	READY		

AC CHARACTERISTICS (OVER SPECIFIED OPERATION CONDITIONS)

Table 11 defines the AC timing specifications that the external memory system must meet and those that the 8XC196MH will provide.

Table 11. AC Timing Definitions (1)

Symbol	Parameter	Min	Max	Units	Notes
F_{OSC}	Frequency on XTAL1	8	16	MHz	4
T_{OSC}	$1/F_{OSC}$	62.5	125	ns	
The External Memory System Must Meet These Specifications					
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 75$	ns	
T_{LLYV}	ALE/ADV# Low to READY Setup		$T_{OSC} - 70$	ns	
T_{YLYH}	Non READY Time	No Upper Limit		ns	
T_{LLYX}	READY Hold after ALE/ADV# Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	2
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2T_{OSC} - 75$	ns	
T_{LLGV}	ALE/ADV# Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns	

NOTES:
1. Test Conditions: Capacitive load on all pins = 100 pF, rise and fall times = 10 ns, F_{OSC} = 16 MHz.
2. Exceeding the maximum specification causes additional wait states.
3. If wait states are used, add $2T_{OSC} \times n$, where n = number of wait states.
4. Testing is performed down to 8 MHz, although the device is static by design and will typically operate below 1 Hz.
5. Assuming back-to-back bus cycles.
6. 8-bit bus only.

Table 11. AC Timing Definitions (1) (Continued)

Symbol	Parameter	Min	Max	Units	Notes
The External Memory System Must Meet These Specifications (Continued)					
T_{LLGX}	BUSWIDTH Hold after ALE/ADV# Low	T_{OSC}		ns	
T_{LHDV}	ALE/ADV# High to Input Data Valid		$3T_{OSC} – 55$	ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} – 55$	ns	3
T_{RLDV}	RD# Active to Input Data Valid		$T_{OSC} – 30$	ns	3
T_{RHDZ}	End of RD# to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after RD# Inactive	0		ns	
The 8XC196MH will Meet These Specifications					
T_{XHLH}	XTAL1 Rising Edge to ALE Rising	20	110	ns	
T_{XHLL}	XTAL1 Rising Edge to ALE Falling	20	110	ns	
T_{LHLH}	ALE/ADV# Cycle Time	$4T_{OSC}$		ns	3
T_{LHLL}	ALE/ADV# High Period	$T_{OSC} – 10$	$T_{OSC} + 10$	ns	
T_{AVLH}	Address Valid to ALE/ADV# High	$T_{OSC} – 17$		ns	
T_{AVLL}	Address Valid to ALE/ADV# Low	$T_{OSC} – 17$		ns	
T_{LLAX}	Address Hold after ALE/ADV# Low	$T_{OSC} – 40$		ns	
T_{LLRL}	ALE/ADV# Low to RD# Low	$T_{OSC} – 30$		ns	
T_{RLRH}	RD# Low Period	$T_{OSC} – 5$	$T_{OSC} + 25$	ns	3
T_{RHLH}	RD# High to ALE/ADV# High	T_{OSC}	$T_{OSC} + 25$	ns	5
T_{RLAZ}	RD# Low to Address Float		5	ns	
T_{LLWL}	ALE/ADV# Low to WR# Low	$T_{OSC} – 10$		ns	
T_{QVWH}	Data Valid before WR# High	$T_{OSC} – 23$		ns	
T_{WLWH}	WR# Low Period	$T_{OSC} – 30$		ns	3
T_{WHQX}	Data Hold after WR# High	$T_{OSC} – 25$		ns	
T_{WHLH}	WR# High to ALE/ADV# High	$T_{OSC} – 10$	$T_{OSC} + 15$	ns	5
T_{WHBX}	BHE#, INST Hold after WR# High	$T_{OSC} – 10$		ns	
T_{WHAX}	A15:8 Hold after WR# High	$T_{OSC} – 30$		ns	6
T_{RHBX}	BHE#, INST Hold after RD# High	$T_{OSC} – 10$		ns	
T_{RHAX}	A15:8 Hold after RD# High	$T_{OSC} – 30$		ns	6

NOTES:
1. Test Conditions: Capacitive load on all pins = 100 pF, rise and fall times = 10 ns, F_{OSC} = 16 MHz.
2. Exceeding the maximum specification causes additional wait states.
3. If wait states are used, add $2T_{OSC} \times n$, where n = number of wait states.
4. Testing is performed down to 8 MHz, although the device is static by design and will typically operate below 1 Hz.
5. Assuming back-to-back bus cycles.
6. 8-bit bus only.

SYSTEM BUS TIMINGS

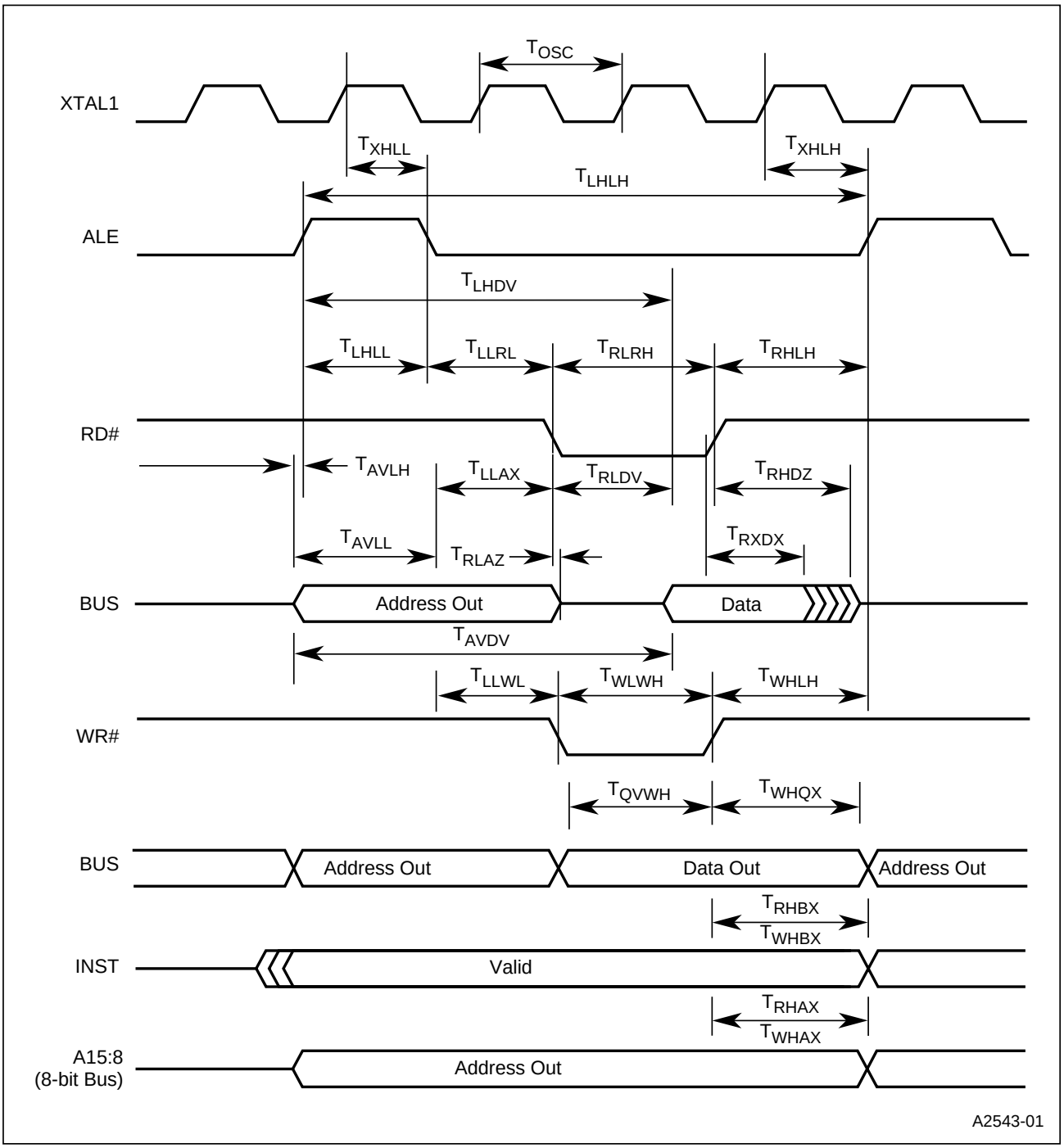


Figure 7. System Bus Timing Diagram

READY TIMING (ONE WAIT STATE)

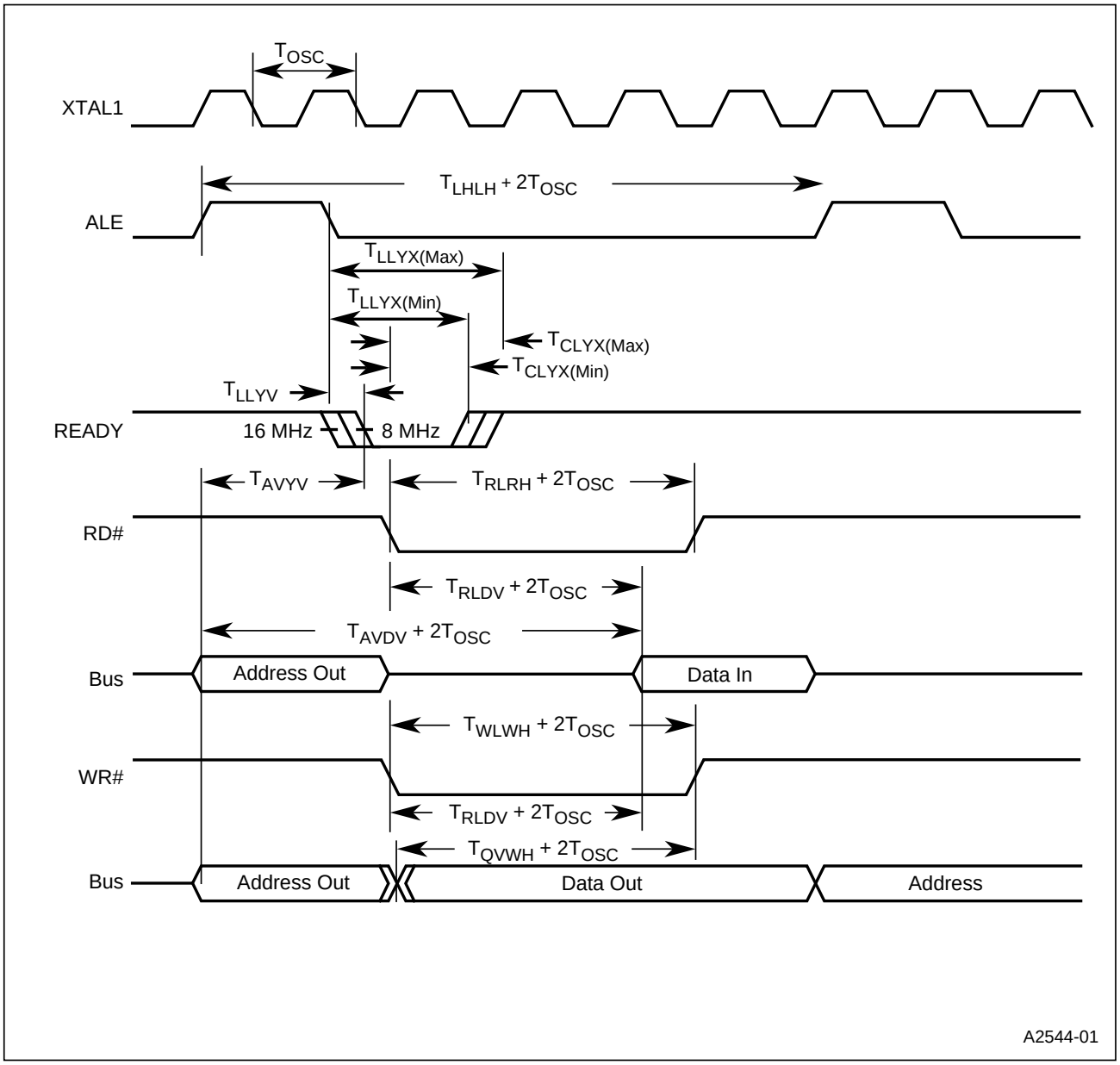


Figure 8. READY Timing Diagram (One Wait State)

BUSWIDTH TIMING

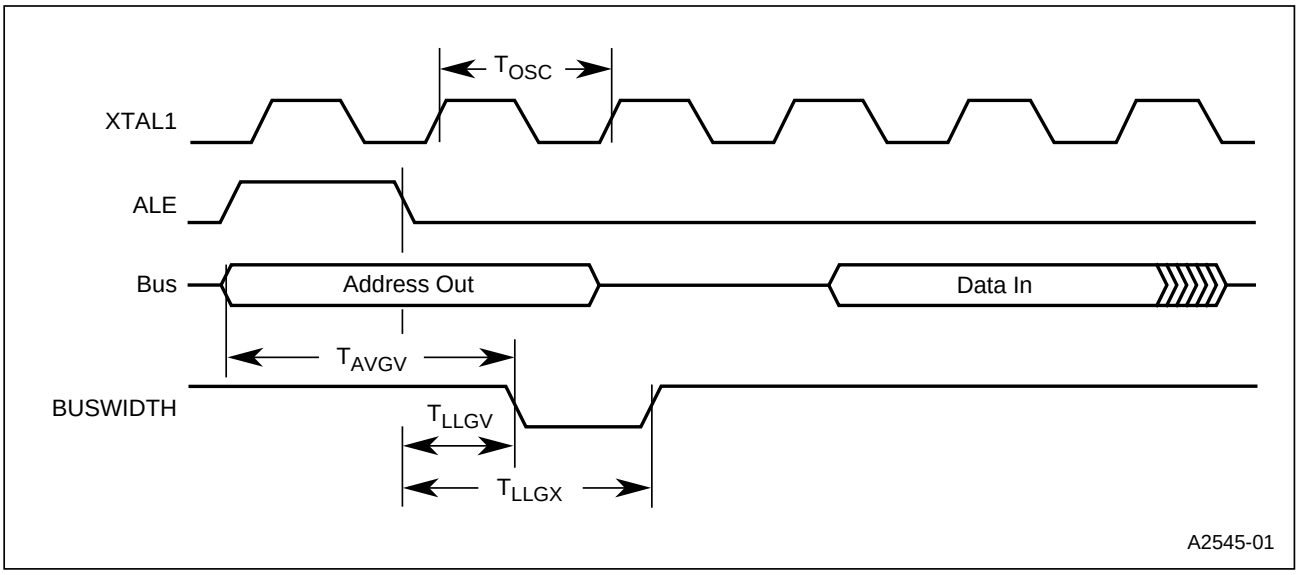


Figure 9. BUSWIDTH Timing Diagram

EXTERNAL CLOCK DRIVE

Table 12. External Clock Drive Timing

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	62.5	125	ns
T_{XHXX}	High Time	22		ns
T_{XLXX}	Low Time	22		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

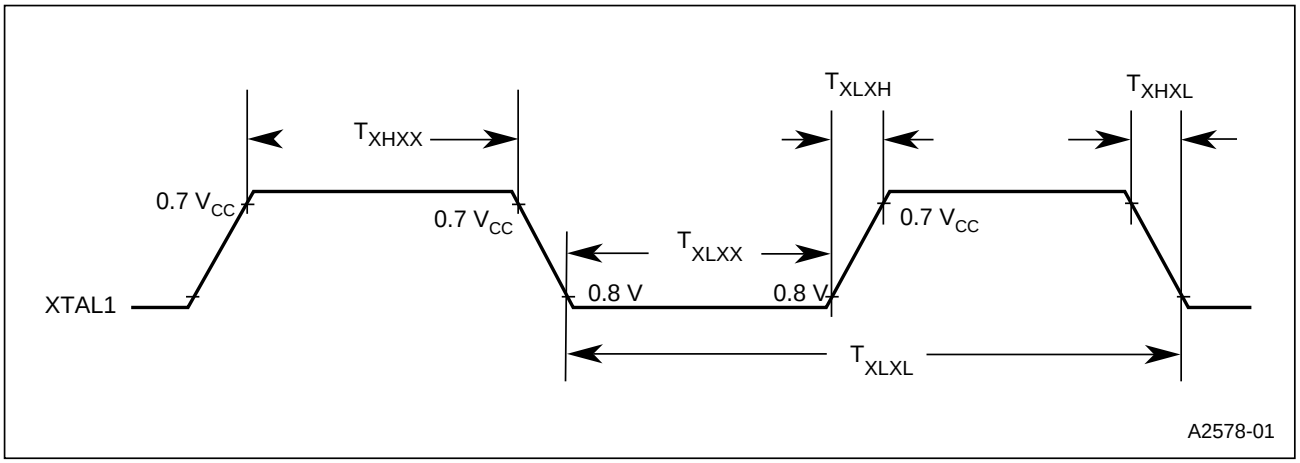


Figure 10. External Clock Drive Waveforms

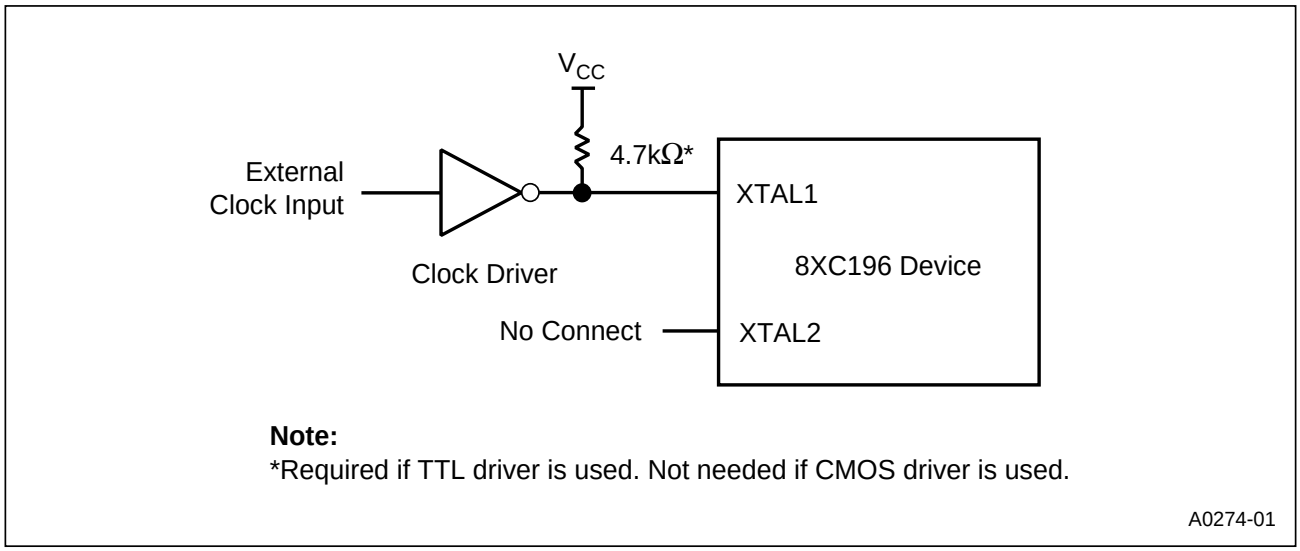
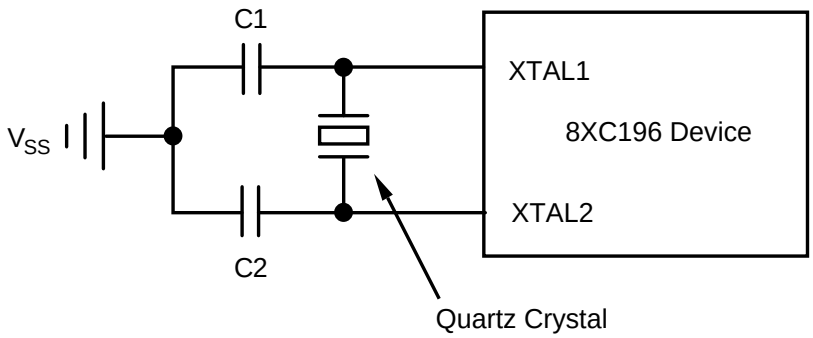


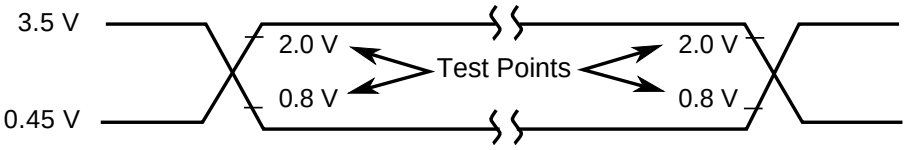
Figure 11. External Clock Connections



Note:
Keep oscillator components close to the chip and use short, direct traces to XTAL1, XTAL2, and V_{ss}. When using crystals, C1=C2≈20pF. When using ceramic resonators, consult the manufacturer for recommended oscillator circuitry.

A0273-01

Figure 12. External Crystal Connections



AC testing inputs are driven at 3.5 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

A2120-02

Figure 13. AC Testing Input, Output Waveforms

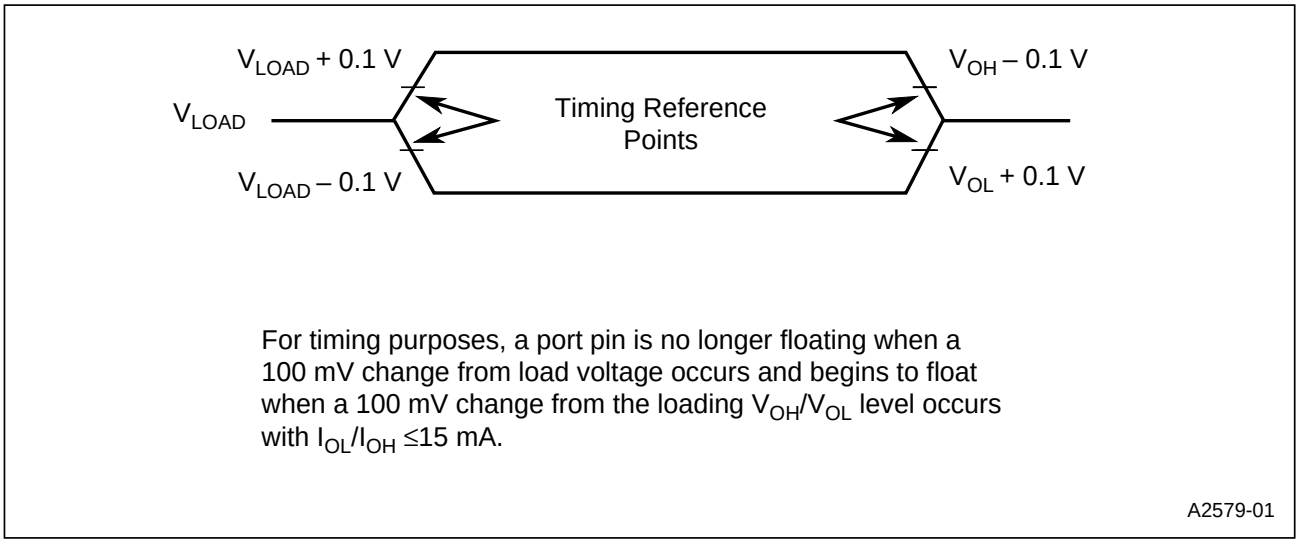


Figure 14. Float Waveforms

AC CHARACTERISTICS — SERIAL PORT, SHIFT REGISTER MODE

Table 13. Serial Port Timing — Shift Register Mode (Mode 0)

Symbol	Parameter	Min	Max	Units	Notes
T_{XLXL}	Serial Port Clock Period (Baud-rate*n* ≥ 8002H) (Baud-rate*n* = 8001H)	 $6T_{OSC}$ $4T_{OSC}$		 ns ns	 1, 2
T_{XLXH}	Serial Port Clock Low Period (Baud-rate*n* ≥ 8002H) (Baud-rate*n* = 8001H)	 $4T_{OSC}$ – 50 $2T_{OSC}$ – 50	 $4T_{OSC}$ + 50 $2T_{OSC}$ + 50	 ns ns	 1, 2
T_{QVXH}	Output Data Setup to Clock High	$2T_{OSC}$ – 50		ns	
T_{XHQX}	Output Data Hold after Clock High	$2T_{OSC}$ – 50		ns	
T_{XHQV}	Next Output Data Valid after Clock High		$2T_{OSC}$ + 50	ns	
T_{DVXH}	Input Data Setup to Clock High	T_{OSC} + 50		ns	
T_{XHDX}	Input Data Hold after Clock High	0		ns	
T_{XHQZ}	Last Clock High to Output Float		T_{OSC}	ns	

NOTES:
1. *n* for Baud-rate*n* signifies Serial Port 0 or 1.
2. Maximum Serial Port Mode 0 reception is with Baud-rate*n* ≥ 8002H.

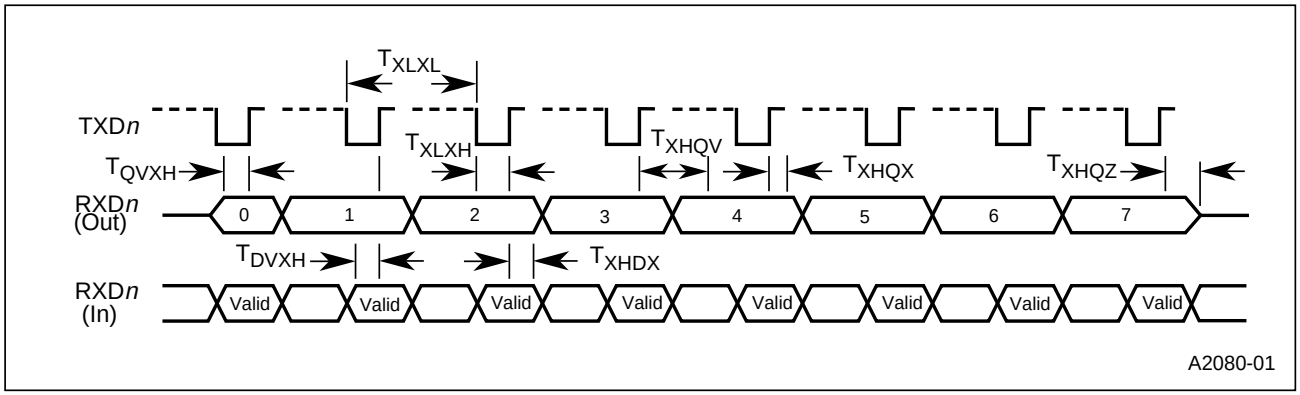


Figure 15. Serial Port Waveform — Shift Register Mode (Mode 0)

Table 14. Serial Port Timing — Mode 4

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (DIR=0)	$16T_{OSC}$	$131072T_{OSC}$	ns
T_{XLXX}	Serial Port Clock Low Period (DIR=0/1)	$(T_{XLXL}/2) – 30$		ns
T_{XHXX}	Serial Port Clock High Period (DIR=0/1)	$(T_{XLXL}/2) – 30$		ns
T_{XLXL}	Serial Port Clock Period (DIR=1)	$16T_{OSC}$		ns
T_{XHXL}	Serial Clock Falling Time (DIR=1)	0	20	ns
T_{XLXH}	Serial Clock Rising Time (DIR=1)	0	20	ns
T_{XLQV}	Clock Low to Output Data Setup		$7.5T_{OSC} – 50$	ns
T_{XLQX}	Output Data Hold after Clock Low	0		ns
T_{XHQX}	Last Output Data Hold after Clock High (DIR=1)	$13.7T_{OSC}$		ns
T_{DVXX}	Input Data Setup to Clock Low Invalid	0		ns
T_{XHDH}	Input Data Hold after Clock High	$6T_{OSC}$		ns

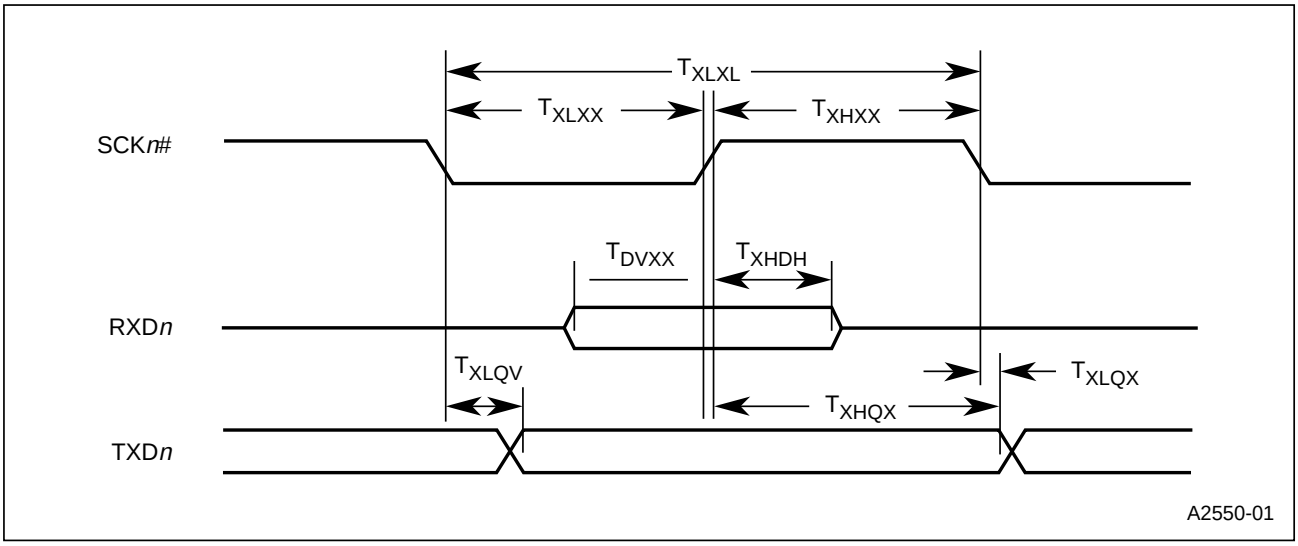


Figure 16. Serial Port Waveform — Mode 4

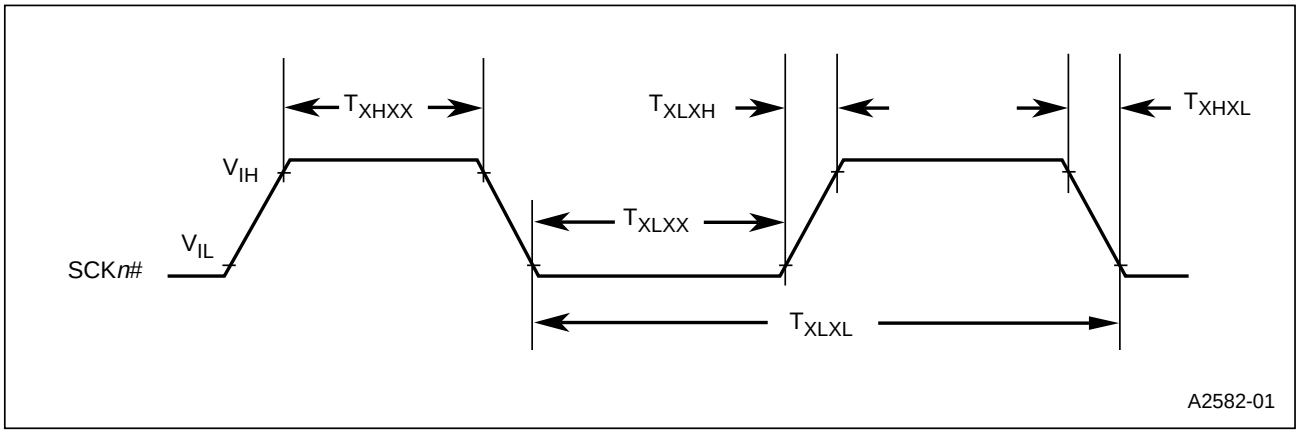


Figure 17. Serial Port Waveform — Clock Drive (DIR = 1)

BAUD-RATE CLOCK DRIVE TABLE

Table 15. Baud Rate Clock Drive

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Baud Rate Clock Period		$4T_{OSC}$	ns
T_{XHXX}	Baud Rate Clock High Time	$2T_{OSC} - 30$		ns
T_{XLXX}	Baud Rate Clock Low Time	$2T_{OSC} - 30$		ns
T_{XLXH}	Baud Rate Clock Rise Time		20	ns
T_{XHXL}	Baud Rate Clock Fall Time		20	ns

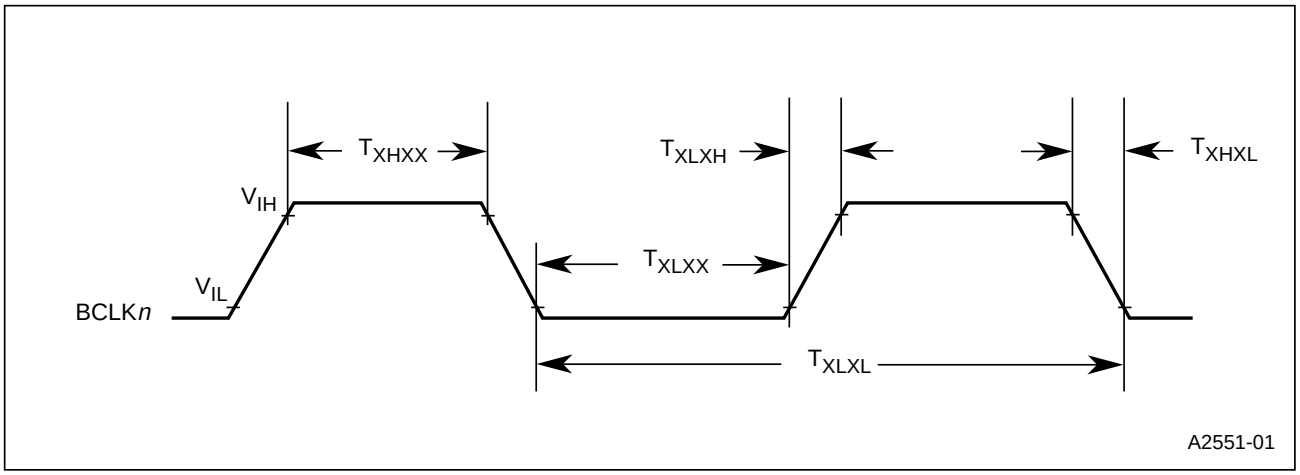


Figure 18. Baud-Rate Clock Drive Waveforms

A/D SAMPLE AND CONVERSION TIMES

Two parameters, sample time and conversion time, control the time required for an A/D conversion. The sample time is the length of time that the analog input voltage is actually connected to the sample capacitor. If this time is too short, the sample capacitor will not charge completely. If the sample time is too long, the input voltage may change and cause conversion errors. The conversion time is the length of time required to convert the analog input voltage stored on the sample capacitor to a digital value. The conversion time must be long enough for the comparator and circuitry to settle and resolve the voltage. Excessively long conversion times allow the sample capacitor to discharge, degrading accuracy.

The AD_TIME register programs the A/D sample and conversion times. Use the T_{SAM} and T_{CONV} specifications in Tables 16 and 18 to determine appropriate values for SAM and CONV; otherwise, erroneous conversion results may occur.

Use the following formulas to determine the SAM and CONV values:

$$SAM = \frac{T_{SAM} \times F_{OSC} - 2}{8}$$

$$CONV = \left[\frac{T_{CONV} \times F_{OSC} - 3}{2 \times B}\right] - 1$$

where:

SAM = 1 to 7
CONV = 2 to 31
T_{SAM} is the sample time, in µsec (Tables 16 and 18)
T_{CONV} is the conversion time, in µsec (Tables 16 and 18)
F_{OSC} is the XTAL1 frequency, in MHz
B is the number of bits to be converted (8 or 10)

When the SAM and CONV values are known, write them to the AD_TIME register. Do not write to this register while a conversion is in progress; the results are unpredictable.

AC CHARACTERISTICS — A/D CONVERTER

Table 16. 10-bit A/D Operating Conditions (1)

Symbol	Description	Min	Max	Units	Notes
T_A	Ambient Temperature	– 40	+ 85	°C	
V_{CC}	Digital Supply Voltage	4.50	5.50	V	
V_{REF}	Analog Supply Voltage	4.50	5.50	V	2
T_{SAM}	Sample Time	1.0		µs	3
T_{CONV}	Conversion Time	10.0	20.0	µs	3
F_{OSC}	Oscillator Frequency	8	16	MHz	

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than + 0.5 V because V_{REF} supplies both the resistor ladder and the analog portion of the converter and input port pins.
3. Program the AD_TIME register to meet the T_{SAM} and T_{CONV} specifications.

Table 17. 10-bit Mode A/D Characteristics Over Specified Operating Conditions (1)

Parameter	Typical (3)	Min	Max	Units (2)	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	± 3	LSBs	
Full-scale Error	0.25 ± 0.5			LSBs	
Zero Offset Error	0.25 ± 0.5			LSBs	
Nonlinearity	1.0 ± 2.0		± 3	LSBs	
Differential Nonlinearity		– 0.75	+ 0.75	LSBs	
Channel-to-channel Matching	± 0.1	0	± 1	LSBs	
Repeatability	± 0.25	0		LSBs	

NOTES:
1. Testing is performed with V_{REF} = 5.12 V and F_{OSC} = 16 MHz.
2. An *LSB*, as used here, has a value of approximately 5 mV.
3. Typical values are based on a limited number of samples and are not guaranteed. Operating conditions for typical values are room temperature and $V_{REF} = V_{CC}$ = 5.5 V.
4. DC to 100 KHz.
5. Multiplexer break-before-make guaranteed.
6. Resistance from device pin, through internal multiplexer, to sample capacitor.
7. These values may be exceeded if the pin current is limited to ± 2mA.
8. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
9. All conversions were performed with processor in idle mode.

Table 17. 10-bit Mode A/D Characteristics Over Specified Operating Conditions (1) (Continued)

Parameter	Typical (3)	Min	Max	Units (2)	Notes
Temperature Coefficients: Offset Full-scale Differential Nonlinearity	 0.009 0.009 0.009			 LSB/C LSB/C LSB/C	
Off-isolation		– 60		dB	4, 5
Feedthrough	– 60			dB	4
V_{CC} Power Supply Rejection	– 60			dB	6
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		ANGND – 0.5	V_{REF} + 0.5	V	7, 8
Sampling Capacitor	3			pF	
DC Input Leakage	± 1.0	0	± 3	µA	

NOTES:
1. Testing is performed with V_{REF} = 5.12 V and F_{OSC} = 16 MHz.
2. An *LSB*, as used here, has a value of approximately 5 mV.
3. Typical values are based on a limited number of samples and are not guaranteed. Operating conditions for typical values are room temperature and $V_{REF} = V_{CC}$ = 5.5 V.
4. DC to 100 KHz.
5. Multiplexer break-before-make guaranteed.
6. Resistance from device pin, through internal multiplexer, to sample capacitor.
7. These values may be exceeded if the pin current is limited to ± 2mA.
8. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
9. All conversions were performed with processor in idle mode.

Table 18. 8-bit A/D Operating Conditions (1)

Symbol	Description	Min	Max	Units	Notes
T_A	Ambient Temperature	– 40	+ 85	°C	
v_{CC}	Digital Supply Voltage	4.50	5.50	V	
v_{REF}	Analog Supply Voltage	4.50	5.50	V	2
T_{SAM}	Sample Time	1.0		µs	3
T_{CONV}	Conversion Time	7.0	20.0	µs	3
F_{OSC}	Oscillator Frequency	8	16	MHz	

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than + 0.5 V because V_{REF} supplies both the resistor ladder and the analog portion of the converter and input port pins.
3. Program the AD_TIME register to meet the T_{SAM} and T_{CONV} specifications.

Table 19. 8-bit Mode A/D Characteristics Over Specified Operating Conditions (1)

Parameter	Typical (3)	Min	Max	Units (2)	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	± 1	LSBs	
Full-scale Error	± 0.5			LSBs	
Zero Offset Error	± 0.5			LSBs	
Nonlinearity		0	± 1	LSBs	
Differential Nonlinearity		– 0.5	+ 0.5	LSBs	
Channel-to-channel Matching		0	± 1	LSBs	
Repeatability	± 0.25	0		LSBs	
Temperature Coefficients: Offset Full-scale Differential Nonlinearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		– 60		dB	4, 5
Feedthrough	– 60			dB	4
V_{CC} Power Supply Rejection	– 60			dB	4
Input Series Resistance		750	1.2K	Ω	6
Voltage on Analog Input Pin		ANGND – 0.5	V_{REF} + 0.5	V	7, 8
Sampling Capacitor	3			pF	
DC Input Leakage	± 1	0	± 3	µA	

NOTES:
1. Testing is performed with V_{REF} = 5.12 V and F_{OSC} = 16 MHz.
2. An *LSB*, as used here, has a value of approximately 20 mV.
3. Typical values are based on a limited number of samples and are not guaranteed. Operating conditions for typical values are room temperature and $V_{REF} = V_{CC}$ = 5.5 V.
4. DC to 100 KHz.
5. Multiplexer break-before-make guaranteed.
6. Resistance from device pin, through internal multiplexer, to sample capacitor.
7. These values may be exceeded if the pin current is limited to ± 2mA.
8. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
9. All conversions were performed with processor in idle mode.

OTPROM SPECIFICATIONS

Table 20. Programming Operating Conditions

Symbol	Description	Min	Max	Units	Notes
T_A	Ambient Temperature	20	30	°C	
V_{CC}	Supply Voltage During Programming	4.50	5.50	V	3
V_{REF}	Reference Supply Voltage During Programming	4.50	5.50	V	3
V_{PP}	Programming Voltage	12.25	12.75	V	2
V_{EA}	EA Pin Voltage	12.25	12.75	V	2
F_{OSC}	Oscillator Frequency During Auto and Slave Mode Programming Oscillator Frequency During Run-Time Programming	6 6	8 12	MHz MHz	

NOTES:
1. V_{CC} and V_{REF} should be at nominally the same voltage during programming.
2. If V_{PP} and V_{EA} exceed the maximum specification, the device may be damaged.
3. V_{SS} and ANGND should be at nominally the same potential (0 volts).
4. Load capacitance during auto and slave mode programming = 150 pF.

Table 21. AC OTPROM Programming Characteristics

Symbol	Description	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	PALE# Pulse Width	50		T_{OSC}
T_{PLPH}	PROG# Pulse Width (1)	50		T_{OSC}
T_{PHLL}	PROG# High to Next PALE# Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	PROG# High to Next PROG# Low	220		T_{OSC}
T_{LHPL}	PALE# High to PROG# Low	220		T_{OSC}
T_{PLDV}	PROG# Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	RESET# High to First PALE# Low	1100		T_{OSC}
T_{PHIL}	PROG# High to AINC# Low	0		T_{OSC}
T_{ILIH}	AINC# Pulse Width	240		T_{OSC}

NOTE:
1. This specification is for Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm explained in the User's Manual.

Table 21. AC OTPROM Programming Characteristics (Continued)

Symbol	Description	Min	Max	Units
T_{ILVH}	PVER Hold after AINC# Low	50		T_{OSC}
T_{ILPL}	AINC# Low to PROG# Low	170		T_{OSC}
T_{PHVL}	PROG# High to PVER Valid		220	T_{OSC}

NOTE:
1. This specification is for Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm explained in the User's Manual.

Table 22. DC OTPROM Programming Characteristics

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (when programming)		100	mA

NOTE: Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabiliized. Otherwise, the device may be damaged.

OTPROM PROGRAMMING WAVEFORMS

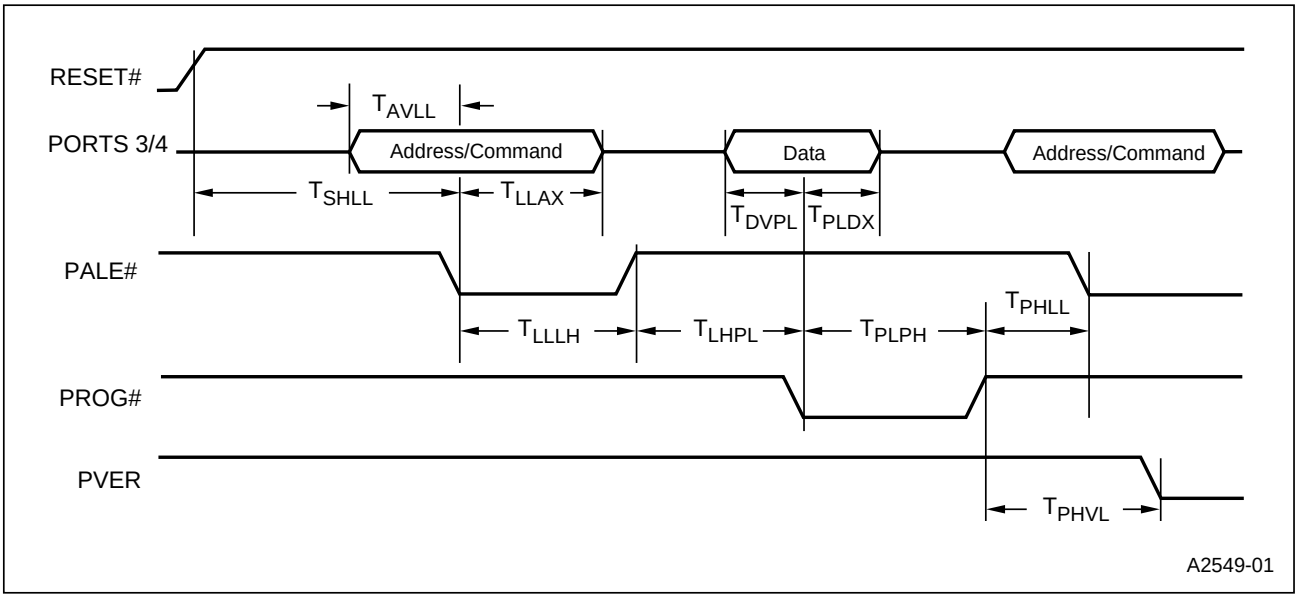


Figure 19. Slave Programming Mode Data Program Mode with Single Program Pulse

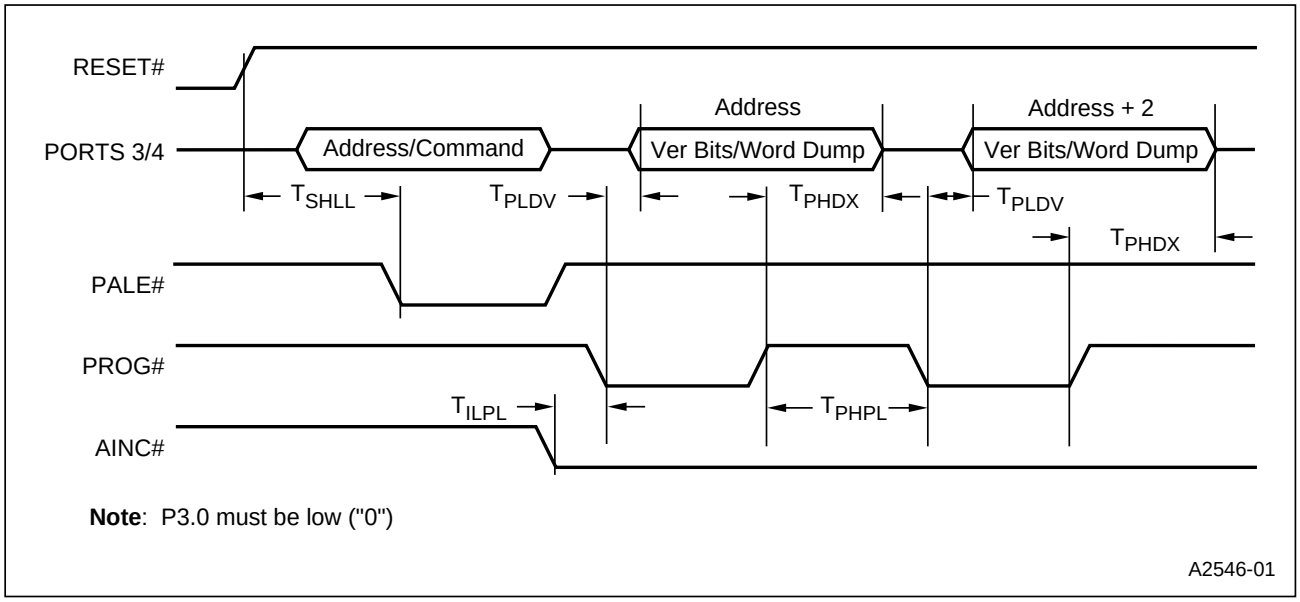


Figure 20. Slave Programming Mode in Word Dump with Autoincrement Timing

SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTOINCREMENT

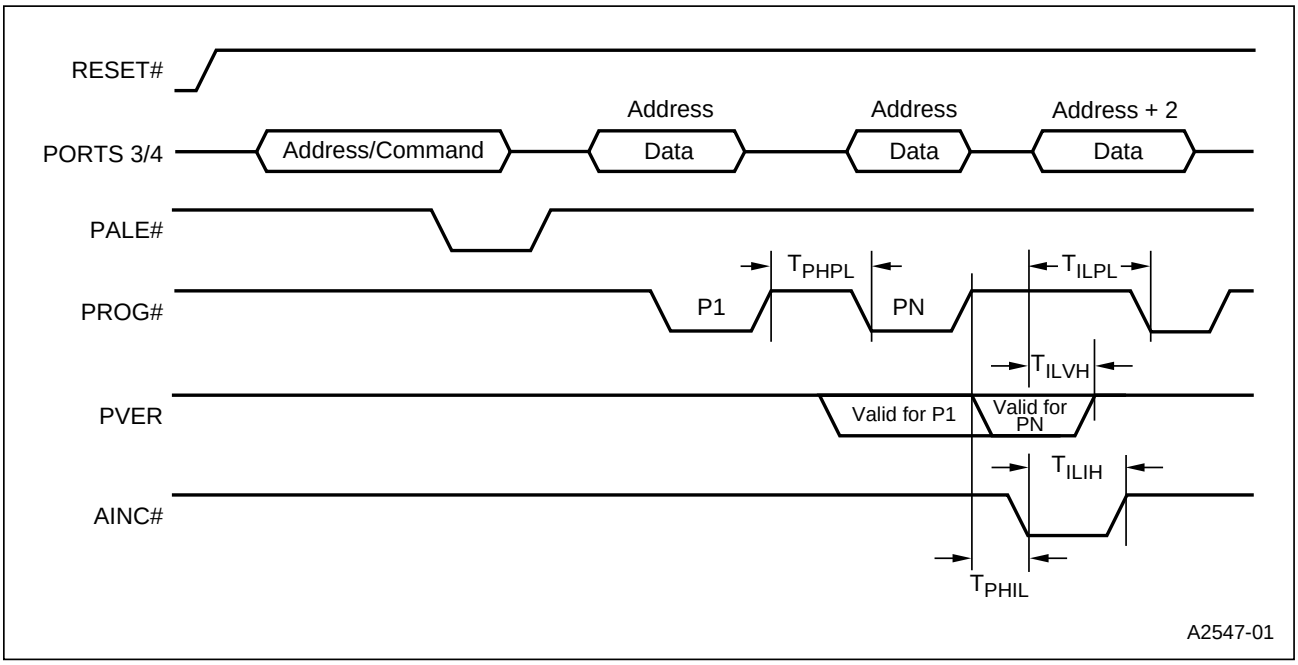


Figure 21. Slave Programming Mode in Data Program with Repeated Program Pulse and Autoincrement

8XC196MC/MD TO 8XC196MH DESIGN CONSIDERATIONS

The 8XC196MH is not pin compatible with the 8XC196MC or the 8XC196MD. Be aware that signal multiplexing sometimes differs between the 8XC196MH and the 8XC196MC/MD. For example, P2.7 is multiplexed with COMP3 on the 8XC196MC/MD and with SCLK1# and BCLK1 on the 8XC196MH.

DATA SHEET REVISION HISTORY

This is the initial publication of this data sheet (272543-001). Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.