2-Series, 3-Series, and 4-Series Li-Ion Battery Pack Manager

Check for Samples: bq30z50-R1, bq30z55-R1

FEATURES

- **Fully Integrated 2-Series, 3-Series, and 4-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection**
- **High Side N-CH Protection FET Drive**
- **Integrated Pre-Charge FET**
- **Integrated Cell Balancing While Charging or At Rest**
- **SBS v1.1 Interface**
- **Low Power Modes**
  - **Low Power: < 180 µA**
  - **Sleep < 76 µA**
- **Complete Set of Advanced Protections:**
  - **Internal Cell Short**
  - **Cell Imbalance**
  - **Cell Voltage**
  - **Over Current**
  - **Temperature**
  - **FET Protection**
- **Sophisticated Charge Algorithms**
  - **JEITA**
  - **Enhanced Charging**
  - **Adaptive Charging**
  - **Cell Balancing While Charging or at Rest**
- **Diagnostic Lifetime Data Monitor**
- **PF Snapshot and Black Box Recorder**
- **SHA-1 Authentication**
- **Small Package: TSSOP**

APPLICATIONS

- **Notebook/Netbook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The bq30z5x-R1 device is a fully integrated gas gauge and analog monitoring single-package solution that provides protection and monitoring with authentication for 2-series, 3-series, and 4-series cell Li-Ion battery packs.

One of the most advanced devices of its kind on the market, the bq30z5x-R1 device incorporates sophisticated algorithms that provide cell balancing while charging or at rest.

The device communicates via an SBS v1.1 interface, providing high accuracy cell parameter reporting and control of battery pack operation.

An optimum balance of quick response hardware-based protection along with intelligent CPU control provides an ideal pack solution. The device provides flexible user-programmable settings of critical system parameters, such as voltage, current, temperature, and cell imbalance, among other conditions.

The bq30z5x-R1 device has advanced charge algorithms, including JEITA support, enhanced cell charging, and adaptive charging compensating charge losses, enabling faster charging. In addition, the bq30z5x-R1 device can monitor critical parameters over the life of the battery pack, enabling tracking of usage conditions.

The advanced snapshot and black box functionality provide critical information for analysis of returned battery packs.

SHA-1 authentication with secure memory for authentication keys enables identification for genuine battery packs beyond doubt.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PART NUMBER	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING INFORMATION(1)	
					TUBE(2)	TAPE AND REEL(3)
–40°C to 85°C	bq30z50-R1	TSSOP–38	DBT	bq30z50-R1	bq30z50-R1DBT	bq30z50-R1DBTR
	bq30z55-R1	TSSOP–30	DBT	bq30z55-R1	bq30z55-R1DBT	bq30z55-R1DBTR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of the document, or see the TI website at www.ti.com.
(2) A single tube quantity is 50 units.
(3) A single reel quantity is 2000 units.

THERMAL INFORMATION

THERMAL METRIC(1)		bq30z50 TSSOP and QFN 38 PINS	bq30z55 TSSOP and QFN 30 PINS	UNITS
$\theta_{JA, High K}$	Junction-to-ambient thermal resistance(2)	64.2	73.1	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	16.5	17.5	
θ_{JB}	Junction-to-board thermal resistance (4)	31.2	34.5	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.3	0.3	
ψ_{JB}	Junction-to-board characterization parameter (6)	26.9	30.3	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

TYPICAL IMPLEMENTATION

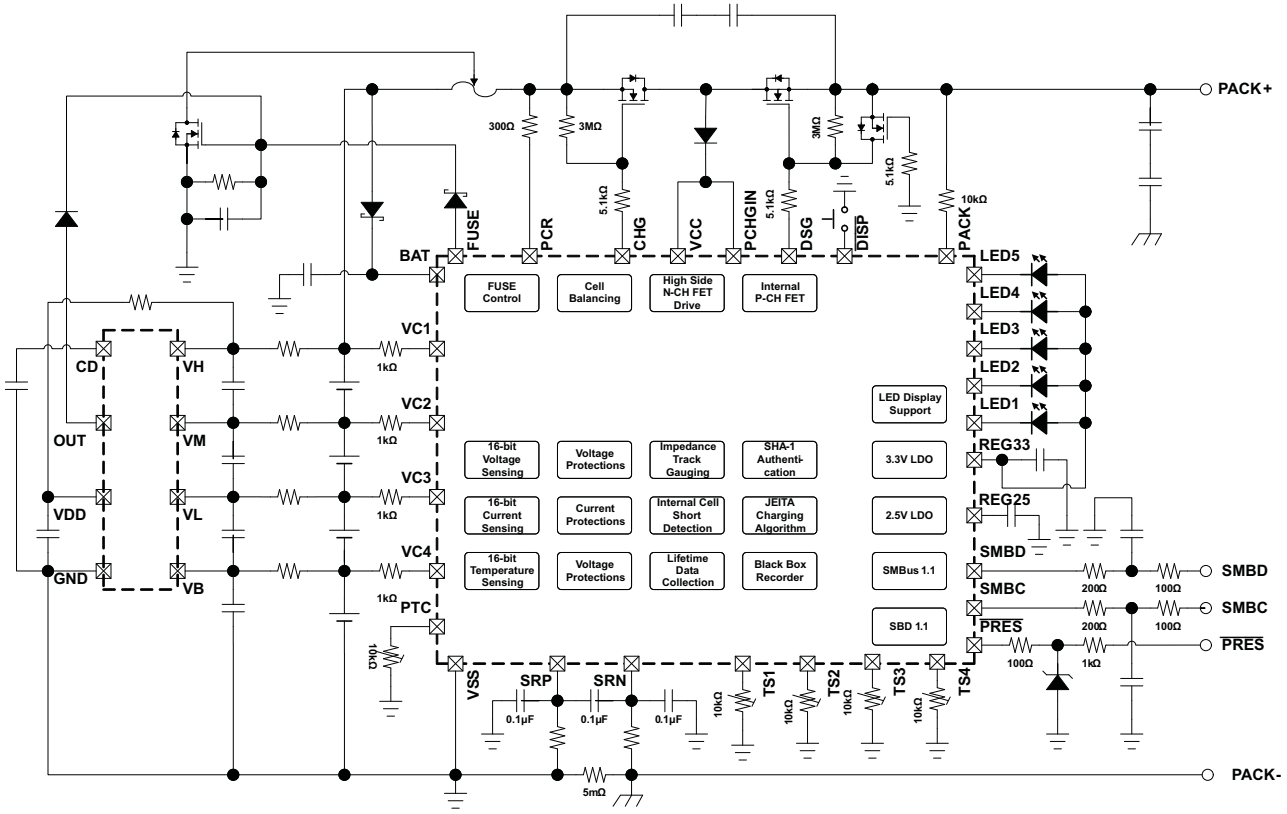


Figure 1. bq30z50-R1 Implementation

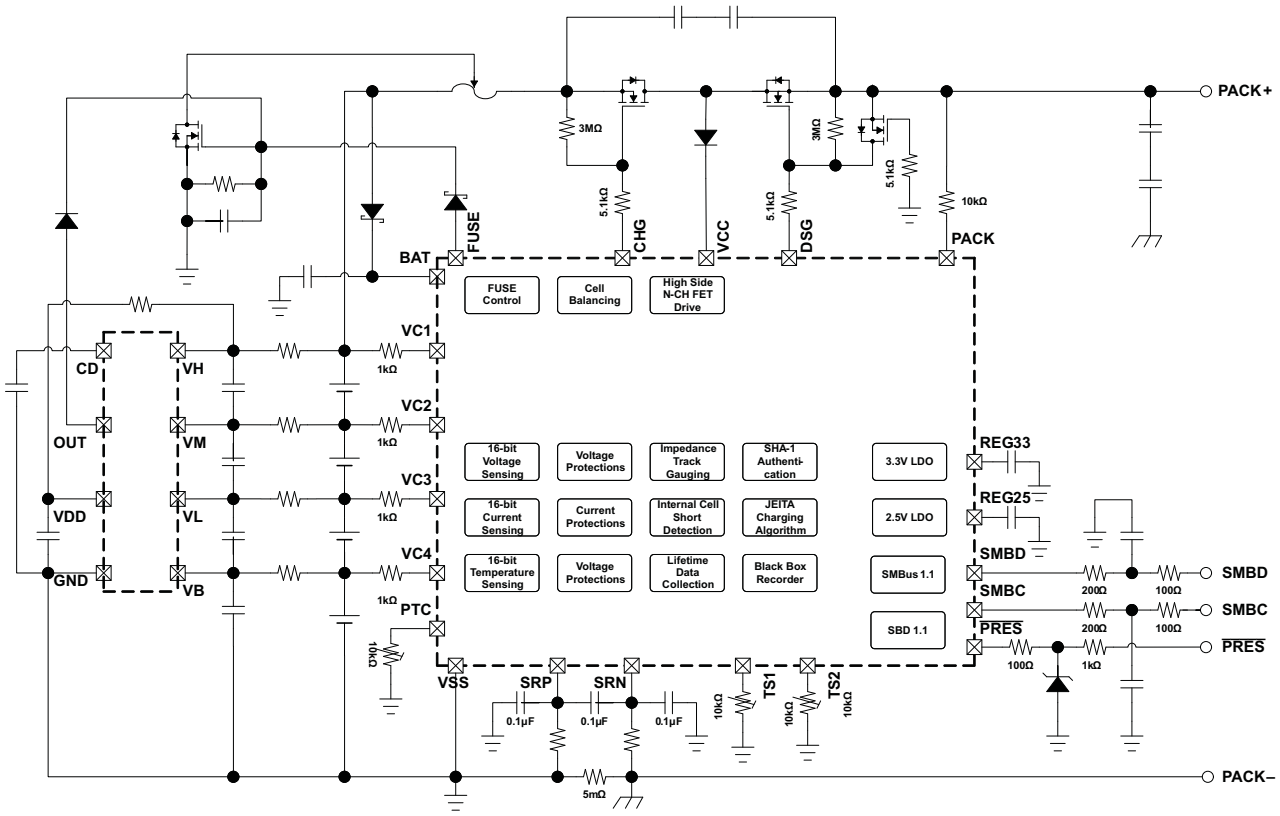


Figure 2. bq30z55-R1 Implementation

TERMINAL FUNCTIONS

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	bq30z50-R1-DBT	bq30z55-R1-DBT		
CHG	1	1	O	Discharge N-FET gate drive
PCR	2	—	O	Pre-Charge Circuit output
BAT	3	2	P	Alternate power source
VC1	4	3	I	Sense input for positive voltage of top most cell in stack and cell balancing input for top most cell in stack
VC2	5	4	I	Sense input for positive voltage of third lowest cell in stack and cell balancing input for third lowest cell in stack
VC3	6	5	I	Sense input for positive voltage of second lowest cell in stack and cell balancing input for second lowest cell in stack
VC4	7	6	I	Sense input for positive voltage of lowest cell in stack and cell balancing input for lowest cell in stack
VSS	8	7	P	Device ground
VSS	9	—	P	Device ground
TS1	10	8	AI	Temperature sensor 1 thermistor input
SRP	11	9	AI	Differential Coulomb counter input
TS2	15	11	AI	Temperature sensor 2 thermistor input
SRN	13	10	AI	Differential Coulomb counter input
TS3	14	—	AI	Temperature sensor 3 thermistor input
TS4	12	—	AI	Temperature sensor 4 thermistor input
$\overline{\text{PRES}}$	18	12	I	Host system present input
SMBD	17	13	I/OD	SBS 1.1 data line
NC	18	14	—	Not connected, connect to VSS
SMBC	19	15	I/OD	SBS 1.1 clock line
$\overline{\text{DISP}}$	20	—	I	Display active input
NC	21	16,17,18,19,20	—	Not connected
LED5	22	—	O	LED display constant current sink
LED4	23	—	O	LED display constant current sink
LED3	24	—	O	LED display constant current sink
LED2	25	—	O	LED display constant current sink
LED1	26	—	O	LED display constant current sink
RBI	27	21	P	RAM backup
REG25	28	22	P	2.5-V regulator output
VSS	29	23	P	Device ground
VSS	30	—	P	Device ground
REG33	31	24	P	3.3-V regulator output
PTC	32	25	—	Test pin connect to VSS
FUSE	33	26	O	Fuse drive
PCHGIN	34	—	I	Pre-Charge circuit input
VCC	35	27	P	Power supply voltage
GPOD	36	28	I/OD	High voltage general purpose I/O
PACK	37	29	P	Alternate power source
DSG	38	30	O	Charge N-FET gate drive

PIN-OUT DIAGRAMS

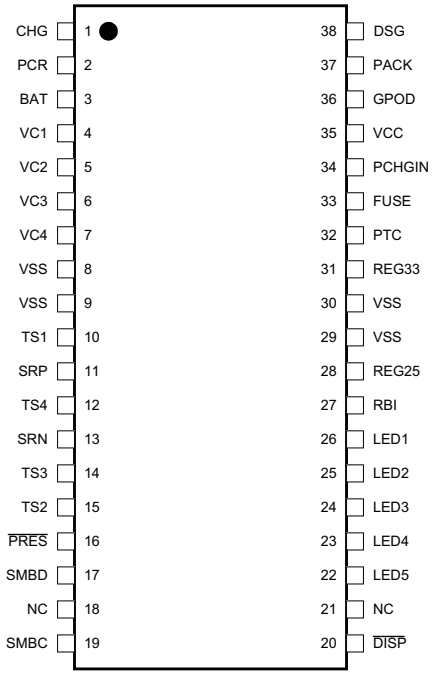


Figure 3. bq30z50-R1 Pin-Out Diagram

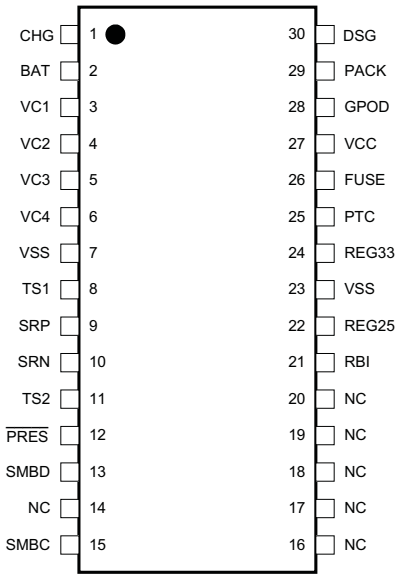


Figure 4. bq30z55-R1 Pin-Out Diagram

PIN EQUIVALENT DIAGRAMS

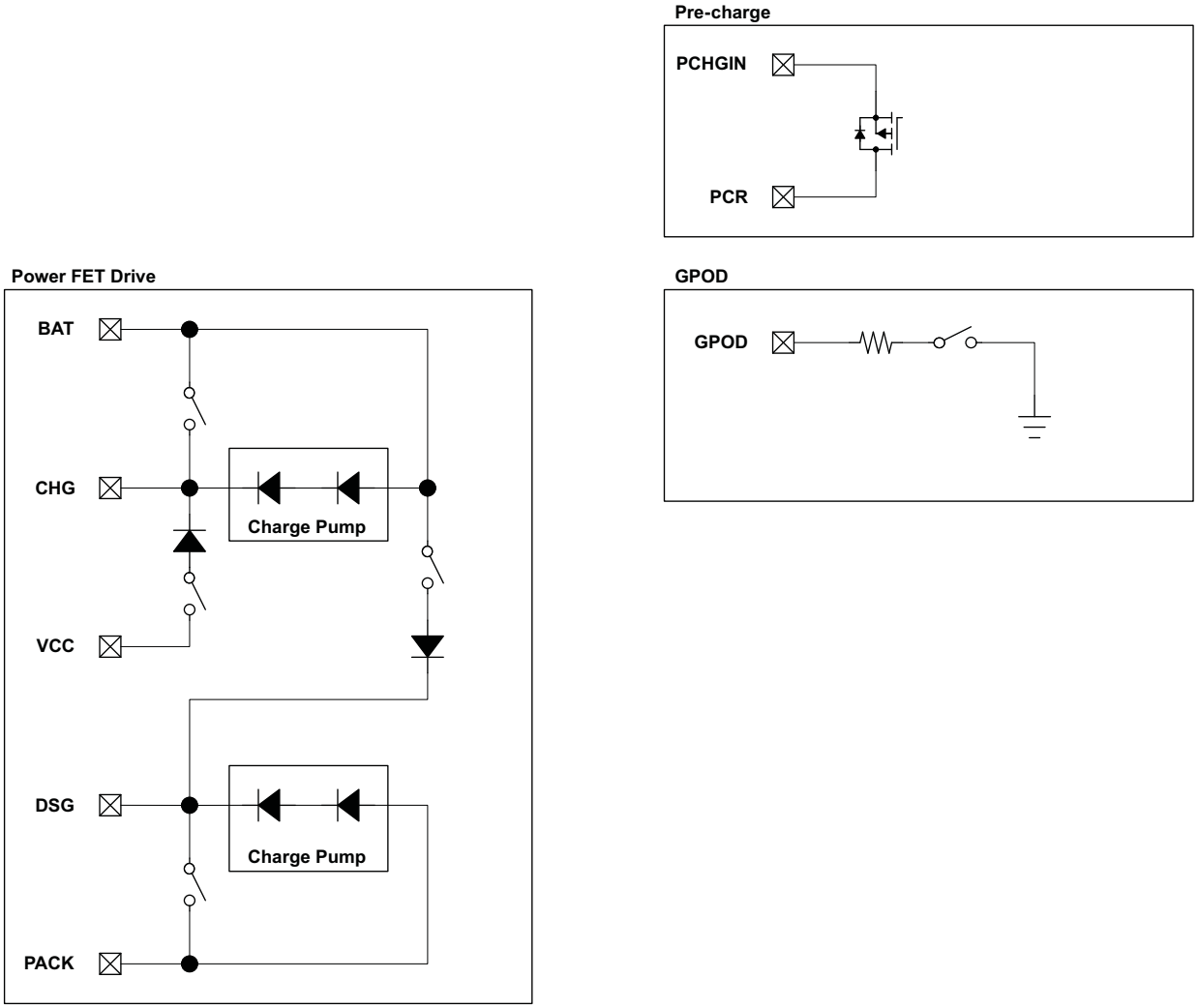


Figure 5. Pin Equivalent Diagram 1

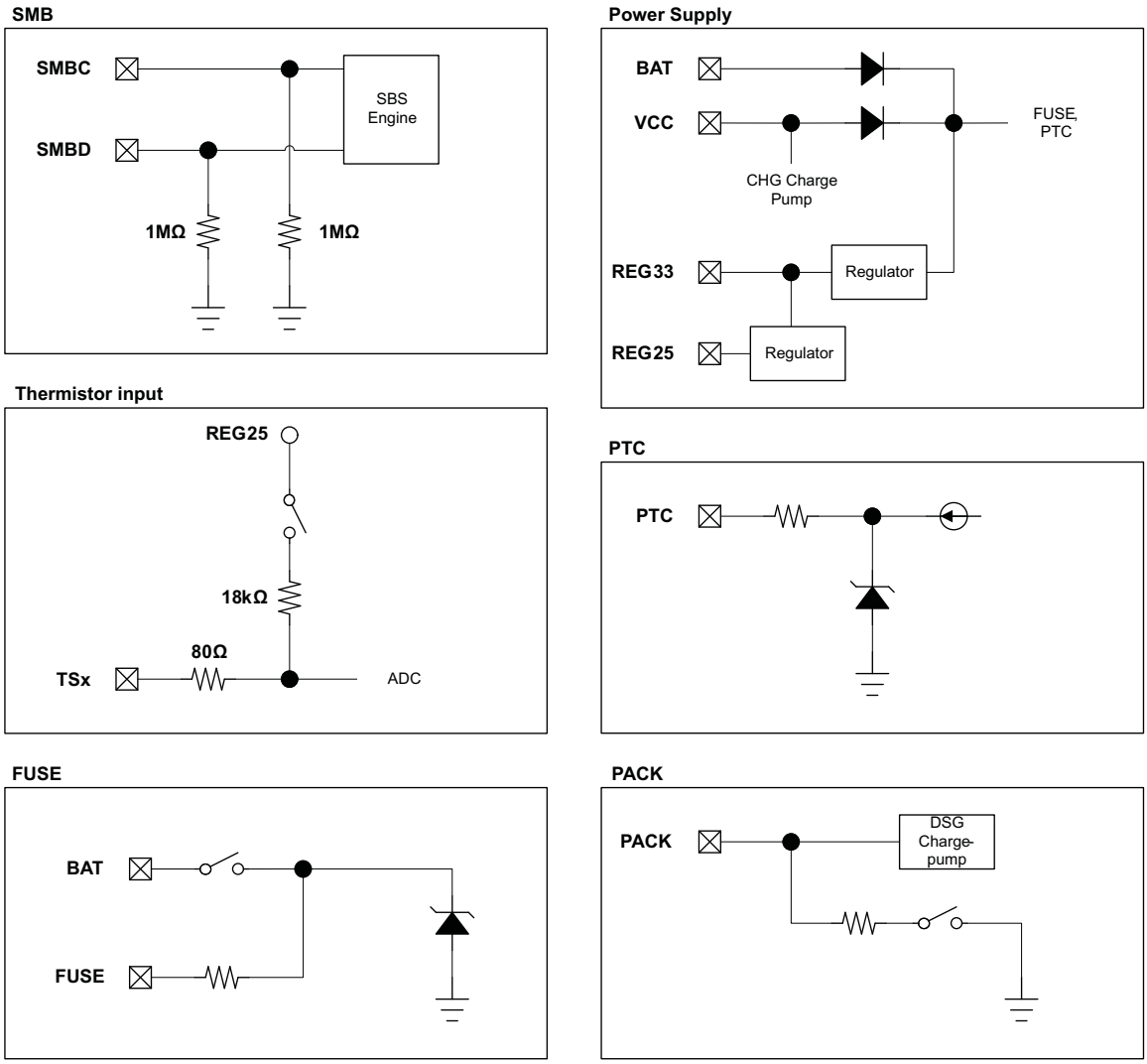


Figure 6. Pin Equivalent Diagram 2

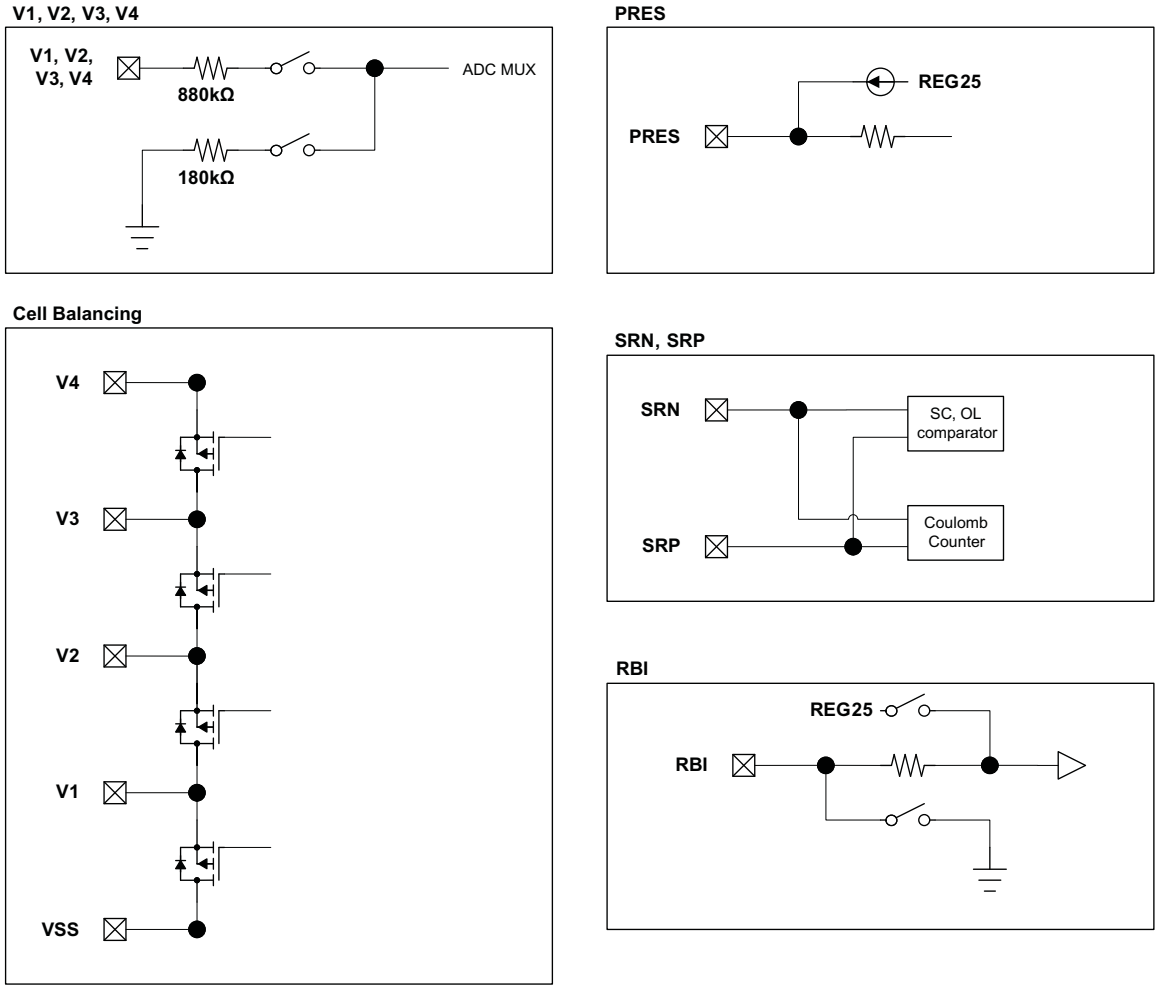


Figure 7. Pin Equivalent Diagram 3

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

DESCRIPTION	PINS	VALUE
Supply voltage range, V_{MAX}	VCC, PCHGIN, PCR, PTC, PACK w.r.t. Vss	–0.3 V to 34 V
Input voltage range, V_{IN}	VC1, BAT	V_{VC2} – 0.3 V to V_{VC2} + 8.5 or 34 V, whichever is lower
	VC2	V_{VC3} – 0.3 V to V_{VC3} + 8.5 V
	VC3	V_{VC4} – 0.3 V to V_{VC4} + 8.5 V
	VC4	V_{SRP}– 0.3 V to V_{SRP} + 8.5 V
	SRP, SRN	–0.3 V to 0.3 V
	LED1, LED2, LED3, LED4, LED5, SMBC, SMBD	V_{SS} – 0.3 V to 6.0 V
	$\overline{DISP}$, TS1, TS2, TS3, TS4, $\overline{PRES}$	–0.3 V to V_{REG25} + 0.3 V
Output voltage range, V_O	DSG	–0.3 V to V_{PACK} + 20 V or V_{SS} + 34 V, whichever is lower
	CHG	–0.3 V to V_{BAT} + 20 V or V_{SS}+ 34 V, whichever is lower
	GPOD, FUSE	–0.3 V to 34 V
	RBI, REG25	–0.3 V to 2.75 V
	REG33	–0.3 V to 5.0 V
Maximum VSS current, I_{SS}		50 mA
Current for cell balancing, I_{CB}		10 mA
ESD Rating	HBM, VCx Only	1 kV
Functional Temperature, T_{FUNC}		–40 to 110 °C
Storage temperature range, T_{STG}		–65 to 150 °C
Lead temperature (soldering, 10 s), T_{SOLDER}		300 °C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Typical values stated where T_A = 25 ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40 ºC to 85 ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage	VCC, PACK, PCHGIN, PCR			25	V
	BAT	3.8		V_{VC2} + 5.0	
$V_{STARTUP}$	Start up voltage at PACK	3.0		5.5	V
V_{IN} Input voltage range	VC1, BAT	V_{VC2}		V_{VC2} + 5.0	V
	VC2	V_{VC3}		V_{VC3} + 5.0	
	VC3	V_{VC4}		V_{VC4} + 5.0	
	VC4	V_{SRP}		V_{SRP} + 5.0	
	VCn – VC(n+1), (n=1, 2, 3, 4)	0		5.0	
	PACK			25	
	PTC	0		2	V
	SRP to SRN	–0.2		0.2	V
C_{REG33} External 3.3-V REG capacitor		1			µF
C_{REG25} External 2.5-V REG capacitor		1			µF
T_{OPR} Operating temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS: Supply Current

Typical values stated where TA = 25 ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40 ºC to 85 ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Normal	CHG on, DSG on, no Flash write		410		µA
	Sleep	CHG off, DSG on, no SBS Communication		129		µA
		CHG off, DSG off, no SBS Communication		83		µA
	Shutdown				1	µA

ELECTRICAL CHARACTERISTICS: Power On Reset (POR)

Typical values stated where TA = 25 ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40 ºC to 85 ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT-}	Negative-going voltage input	At REG25	1.9	2.0	2.1	V
V_{HYS}	POR Hysteresis	At REG25	65	125	165	mV

ELECTRICAL CHARACTERISTICS: WAKE FROM SLEEP

Typical values stated where TA = 25 ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40 ºC to 85 ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE}	V_{WAKE} Threshold	V_{WAKE} = 1.2 mV	0.2	1.2	2.0	mV
		V_{WAKE} = 2.4 mV	0.4	2.4	3.6	
		V_{WAKE} = 5 mV	2.0	5.0	6.8	
		V_{WAKE} = 10 mV	5.3	10	13	
V_{WAKE_TCO}	Temperature drift of VWAKE accuracy			0.5		%/°C
t_{WAKE}	Time from application of current and wake of bq30z5x-R1			0.2	1	ms

ELECTRICAL CHARACTERISTICS: RBI RAM Backup

Typical values stated where TA = 25 ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40 ºC to 85 ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RBI)}$	RBI data-retention input current	VRB > V(RB)MIN, VCC < VIT		20	1100	nA
		VRB > V(RB)MIN, VCC < VIT, T_A = 0 °C to 70 °C			500	
$V_{(RBI)}$	RBI data-retention voltage		1			V

ELECTRICAL CHARACTERISTICS: 3.3-V Regulator

Typical values stated where TA = 25 ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40 ºC to 85 ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG33}	Regulator output voltage	3.8 V < VCC or BAT ≤ 5 V, I_{CC} ≤4 mA	2.4		3.5	V
		5 V < VCC or BAT ≤ 6.8 V, I_{CC} ≤13 mA	3.1	3.3	3.5	V
		6.8 V < VCC or BAT ≤ 20 V, I_{CC} ≤ 30 mA	3.1	3.3	3.5	V
I_{REG33}	Regulator Output Current		2			mA
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature	VCC or BAT = 14.4 V, IREG33 = 2 mA		0.2		%

ELECTRICAL CHARACTERISTICS: 3.3-V Regulator (continued)

Typical values stated where TA = 25 ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40 ºC to 85 ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{(VDDLINE)}$	Line regulation	VCC or BAT = 14.4 V, IREG33 = 2 mA		1	13	mV
$\Delta V_{(VDDLOAD)}$	Load regulation	VCC or BAT = 14.4 V, IREG33 = 2 mA		5	18	mV
$I_{(REG33MAX)}$	Current limit	VCC or BAT = 14.4 V, REG33 = 3 V			70	mA
		VCC or BAT = 14.4 V, REG33 = 0 V			33	

ELECTRICAL CHARACTERISTICS: 2.5-V Regulator

Typical values stated where T_A = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG25}	Regulator output voltage	I_{REG25} = 10 mA	2.35	2.5	2.55	V
I_{REG25}	Regulator Output Current		3			mA
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature	VCC or BAT = 14.4 V, IREG25 = 2 mA		0.25		%
$\Delta V_{(VDDLINE)}$	Line regulation	VCC or BAT = 14.4 V, IREG25 = 2 mA		1	4	mV
$\Delta V_{(VDDLOAD)}$	Load regulation	VCC or BAT = 14.4 V, IREG25 = 2 mA		20	40	mV
$I_{(REG33MAX)}$	Current limit	VCC or BAT = 14.4 V, REG25 = 2.3 V			65	mA
		VCC or BAT = 14.4 V, REG25 = 0 V			23	

ELECTRICAL CHARACTERISTICS: $\overline{DISP}$, $\overline{PRES}$, SMBD, SMBC

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where TA = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input	$\overline{DISP}$, $\overline{PRES}$, SMBD, SMBC	2.0			V
V_{IL}	Low-level input	$\overline{DISP}$, $\overline{PRES}$, SMBD, SMBC, IL = –0.5 mA			0.8	V
V_{OL}	Low-level output voltage	SMBD, SMBC, IL = 7 mA			0.4	V
C_{IN}	Input capacitance	$\overline{DISP}$, $\overline{PRES}$, SMBD, SMBC		5		pF
I_{LKG}	Input leakage current	$\overline{DISP}$, $\overline{PRES}$, SMBD, SMBC			1	µA
I_{WPU}	Weak Pull Up Current	$\overline{PRES}$, V_{OH} = V_{REG25} – 0.5 V	60		120	µA
$I_{(\overline{DISP})}$	$\overline{DISP}$ source currents	$\overline{DISP}$ active, $\overline{DISP}$ = V_{REG25} – 0.6 V	–3			mA
$I_{LKG(\overline{DISP})}$	$\overline{DISP}$ leakage current	$\overline{DISP}$ inactive	–0.22		0.22	µA
$R_{PD(SMBx)}$	SMBC, SMBD Pull-Down	T_A = –40 ˚C to 100 ˚C	550	775	1000	kΩ

ELECTRICAL CHARACTERISTICS: CHG, DSG FET Drive

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON)}$	Output voltage, charge, and discharge FETs on	$V_{O(FETONDSG)} = V_{(DSG)} – V_{PACK}$, VGS connect 10 MΩ, VCC 3.8 V to 8.4 V	8.0	9.7	12	V
		$V_{O(FETONDSG)} = V_{(DSG)} – V_{PACK}$, VGS connect 10 MΩ, VCC > 8.4 V	9.0	11	12	V
		$V_{O(FETONCHG)} = V_{(CHG)} – V_{BAT}$, V_{GS} connect 10 MΩ, VCC 3.8 V to 8.4 V	8.0	9.7	12	V
		$V_{O(FETONCHG)} = V_{(CHG)} – V_{BAT}$, V_{GS} connect 10 MΩ, VCC > 8.4 V	9.0	11	12	V
$V_{(FETOFF)}$	Output voltage, charge and discharge FETs off	$VO_{(FETOFFDSG)} = V_{(DSG)} – V_{PACK}$	–0.4		0.4	V
		$V_{O(FETOFFCHG)} = V_{(CHG)} –$ VBAT	–0.4		0.4	V
t_r	Rise time	C_L = 4700 pF R_G= 5.1 kΩ VCC <8.4 V_{DSG}: V_{BAT} to V_{BAT} + 4 V, V_{CHG}: V_{PACK} to V_{PACK} + 4 V		800	1400	µs
		C_L = 4700 pF R_G= 5.1 kΩ VCC >8.4 V_{DSG}: V_{BAT} to V_{BAT}+4 V, V_{CHG}: V_{PACK} to V_{PACK} + 4 V		200	500	µs
t_f	Fall time	C_L = 4700 pF R_G= 5.1 kΩ V_{DSG}: V_{BAT}+ $V_{O(FETONDSG)}$ to V_{BAT} + 1 V V_{CHG}: V_{PACK} + $V_{O(FETONCHG)}$ to V_{PACK} + 1 V		80	200	µs

ELECTRICAL CHARACTERISTICS: GPOD

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where TA = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PU_GPOD}	GPOD Pull Up Voltage				V_{CC}	V
V_{OL_GPOD}	GPOD Output Voltage Low	I_{OL} = 1 mA	0.3			V

ELECTRICAL CHARACTERISTICS: FUSE

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where TA = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(FUSE)}$	High Level FUSE Output	VCC = 3.8 V to 9 V	2.4		8.5	V
		VCC = 9 V to 25 V	7	8	9	V
$V_{IH(FUSE)}$			2.8			V
	Weak pull up current in off state	Ensured by design. Not production tested.		100		nA
$t_{R(FUSE)}$	FUSE Output Rise Time	C_L = 1 nF, VCC = 9 V to 25V, $V_{OH(FUSE)}$ = 0 V to 5 V		5	20	µs
$Z_{O(FUSE)}$	FUSE Output Impedance			2	5	kΩ

ELECTRICAL CHARACTERISTICS: PTC Thermistor Support

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PTC}	PTC	V_{PTC} = 0 to 2 V,				
		T_A = –40 °C to 110 °C	1.3	2	2.7	MΩ
$I_{O(PTC)}$	PTC	V_{PTC} = 0 to 2 V				
		T_A = –40 °C to 110 °C	–450	–370	–230	nA
t_{PTC}	PTC Blanking Delay	T_A = –40 °C to 110 °C	60	80	110	ms

ELECTRICAL CHARACTERISTICS: LED5, LED4, LED3, LED2, LED1

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where TA = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
I_{OL}	Low-level output current	VOL = 0.4 V, 3-mA setting	2.5	3.5	4.5	mA
		VOL = 0.4 V, 4-mA setting	3.0	4.5	6.0	mA
		VOL = 0.4 V, 5-mA setting	3.5	5.5	7.5	mA
I_{LEDx}	Current matching between LEDx			0.1		mA

ELECTRICAL CHARACTERISTICS: COULOMB COUNTER

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	SRP – SRN	–0.20		0.25	V
	Conversion time	Single conversion		250		ms
	Resolution (no missing codes)		16			bits
	Effective resolution	Single conversion, signed	15			bits
	Offset error	Post Calibrated		10		µV
	Offset error drift			0.3	0.5	µV/°C
	Full-scale error		–0.8%	0.2%	0.8%	
	Full-scale error drift				150	PPM/°C
	Effective input resistance		2.5			MΩ

ELECTRICAL CHARACTERISTICS: VC1, VC2, VC3, VC4

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	VC4 – VC3, VC3 – VC2, VC2 – VC1, VC1 – VSS	–0.20		8	V
	Conversion time	Single conversion		32		ms
	Resolution (no missing codes)		16			bits
	Effective resolution	Single conversion, signed	15			bits
$R_{(BAL)}$	$R_{DS(ON)}$ for internal FET at V_{DS} > 2 V	V_{DS} = VC4 – VC3, VC3 – VC2, VC2 – VC1, VC1 – VSS	200	310	430	Ω
	$R_{DS(ON)}$ for internal FET at V_{DS} > 4 V	V_{DS} = VC4 – VC3, VC3 – VC2, VC2 – VC1, VC1 – VSS	60	125	230	Ω

ELECTRICAL CHARACTERISTICS: TS1, TS2, TS3, TS4

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R	Internal Pull Up Resistor		16.5	17.5	19.0	KΩ
R_{DRIFT}	Internal Pull Up Resistor Drift From 25 °C				200	PPM/°C
R_{PAD}	Internal Pin Pad resistance			84		Ω
V_{IN}	Input voltage range	TS1 – VSS, TS2 – VSS, TS3 – VSS, TS4 – VSS	–0.20		$0.8\times V_{REG25}$	V
	Conversion Time			16		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution		11	12		Bits

ELECTRICAL CHARACTERISTICS: Internal Temperature Sensor

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$	Temperature sensor voltage		–1.9	–2.0	–2.1	mV/°C
	Conversion Time			16		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution		11	12		Bits

ELECTRICAL CHARACTERISTICS: Internal Thermal Shutdown

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{MAX1}	Maximum PCHG temperature		110		150	°C
T_{MAX2}	Maximum REG33 temperature		125		175	
$T_{RECOVER}$	Recovery hysteresis temperature			10		°C
$t_{PROTECT}$	Protection time			5		µs

ELECTRICAL CHARACTERISTICS: High Frequency Oscillator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency of CPU Clock			4.194		MHz
$f_{(EIO)}$	Frequency error(1)(2)	T_A = –20 °C to 70 °C	–2%	±0.25%	2%	
		T_A = –40 °C to 85 °C	–3%	±0.25%	3%	
$t_{(SXO)}$	Start-up time(3)	T_A = –25 °C to 85 °C		3	6	ms

(1) The frequency error is measured from 4.194 MHz.
(2) The frequency drift is included and measured from the trimmed frequency at V_{REG25} = 2.5 V, T_A = 25°C.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3% when the device is already powered.

ELECTRICAL CHARACTERISTICS: Low Frequency Oscillator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		kHz

ELECTRICAL CHARACTERISTICS: Low Frequency Oscillator (continued)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LEIO)}$	Frequency error(1)(2)	T_A = –20 °C to 70 °C	–1.5%	±0.25%	1.5%	
		T_A = –40 °C to 85 °C	–2.5%	±0.25%	2.5%	
$t_{(LSXO)}$	Start-up time(3)	T_A = –25 °C to 85 °C			100	µs

(1) The frequency drift is included and measured from the trimmed frequency at VCC = 2.5 V, T_A = 25 °C.
(2) The frequency error is measured from 32.768 kHz.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3 %.

ELECTRICAL CHARACTERISTICS: Internal Voltage Reference

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal Reference Voltage		1.215	1.225	1.230	V
V_{REF_DRIFT}	Internal Reference Voltage Drift	T_A = –25 °C to 85 °C		±80		PPM/°C
		T_A = 0 °C to 60 °C		±50		PPM/°C

ELECTRICAL CHARACTERISTICS: Flash

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write-cycles	Data Flash	20k			Cycles
		Instruction Flash	1k			Cycles
$I_{CC(PROG\_DF)}$	Data Flash-write supply current	T_A = –40°C to 85°C		3	4	mA
$I_{CC(ERASE\_DF)}$	Data Flash-erase supply current	T_A = –40°C to 85°C		3	18	mA

(1) Assured by design. Not production tested.

ELECTRICAL CHARACTERISTICS: OCD Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OCD)}$	OCD detection threshold voltage range, typical	RSNS = 0	50		200	mV
		RSNS = 1	25		100	mV
$\Delta V_{(OCDT)}$	OCD detection threshold voltage program step	RSNS = 0		10		mV
		RSNS = 1		5		mV
$V_{(OFFSET)}$	OCD offset		–10		10	mV
$V_{(Scale\_Err)}$	OCD scale error		–10		10	%
$t_{(OCDD)}$	Overcurrent in Discharge Delay		1		31	ms
$t_{(OCDD\_STEP)}$	OCDD Step options			2		ms
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Overcurrent and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCD1 Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SDC1)}$	SCD1 detection threshold voltage range, typical	RSNS = 0	100		450	mV
		RSNS = 1	50		225	mV
$\Delta V_{(SCD1T)}$	SCD1 detection threshold voltage program step	RSNS = 0		50		mV
		RSNS = 1		25		mV
$V_{(OFFSET)}$	SCD1 offset		–10		10	mV
$V_{(Scale\_Err)}$	SCD1 scale error		–10		10	%
$t_{(SCD1D)}$	Short Circuit in Discharge Delay	AFE.STATE_CNTL[SCDDx2] = 0	0		915	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		1830	µs
$t_{(SCD1D\_STEP)}$	SCD1D Step options	AFE.STATE_CNTL[SCDDx2] = 0		61		µs
		AFE.STATE_CNTL[SCDDx2] = 1		122		µs
$t_{(DETECT)}$	Current fault detect time	VSRP-SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Overcurrent and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCD2 Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SDC2)}$	SCD2 detection threshold voltage range, typical	RSNS = 0	100		450	mV
		RSNS = 1	50		225	mV
$\Delta V_{(SCD2T)}$	SCD2 detection threshold voltage program step	RSNS = 0		50		mV
		RSNS = 1		25		mV
$V_{(OFFSET)}$	SCD2 offset		–10		10	mV
$V_{(Scale\_Err)}$	SCD2 scale error		–10		10	%
$t_{(SCD1D)}$	Short Circuit in Discharge Delay	AFE.STATE_CNTL[SCDDx2] = 0	0		458	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		915	µs
$t_{(SCD2D\_STEP)}$	SCD2D Step options	AFE.STATE_CNTL[SCDDx2] = 0		30.5		µs
		AFE.STATE_CNTL[SCDDx2] = 1		61		µs
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Overcurrent and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCC Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCCT)}$	SCC detection threshold voltage range, typical	RSNS = 0	–100		–300	mV
		RSNS = 1	–50		–225	mV
$\Delta V_{(SCCDT)}$	SCC detection threshold voltage program step	RSNS = 0		–50		mV
		RSNS = 1		–25		mV

ELECTRICAL CHARACTERISTICS: SCC Current Protection (continued)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OFFSET)}$	SCC offset		–10		10	mV
$V_{(Scale\_Err)}$	SCC scale error		–10		10	%
$t_{(SCCD)}$	Short Circuit in Charge Delay		0		915	ms
$t_{(SCCD\_STEP)}$	SCCD Step options			61		ms
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Overcurrent and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SBS Timing Characteristics

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start		4.0			µs
$t_{SU:STA}$	Repeated start setup time		4.7			µs
$t_{SU:STO}$	Stop setup time		4.0			µs
$t_{HD:DAT}$	Data hold time		300			ns
$t_{SU:DAT}$	Data setup time		250			ns
$t_{TIMEOUT}$	Error signal/detect	See (1)	25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period	See (2)			Disabled	
t_{HIGH}	Clock high period	See (2)	4.0		50	µs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time	See (3)			25	ms
$t_{LOW:MEXT}$	Cumulative clock low master extend time	See (4)			10	ms
t_F	Clock/data fall time	See (5)			300	ns
t_R	Clock/data rise time	See (6)			1000	ns

(1) The bq30z5x-R1 times out when any clock low exceeds $t_{TIMEOUT}$.
(2) t_{HIGH}, Max, is the minimum bus idle time. SMBC = 1 for t > 50 µs causes reset of any transaction involving bq30z5x-R1 that is in progress. This specification is valid when the THIGH_VAL = 0. If THIGH_VAL = 1 then the value of THIGH is set by THIGH_1,2 and the timeout is not SMBus standard.
(3) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) Rise time tR = V_{ILMAX} – 0.15) to (V_{IHMIN} + 0.15)
(6) Fall time tF = 0.9 V_{DD} to (V_{ILMAX} – 0.15)

ELECTRICAL CHARACTERISTICS: SBS XL Timing Characteristics

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMBXL}	SMBus XL operating frequency	Slave mode	40		400	kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start		4.0			µs

ELECTRICAL CHARACTERISTICS: SBS XL Timing Characteristics (continued)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU:STA}$	Repeated start setup time		4.7			µs
$t_{SU:STO}$	Stop setup time		4.0			µs
$t_{TIMEOUT}$	Error signal/detect	See (1)	5		20	ms
t_{LOW}	Clock low period				20	µs
t_{HIGH}	Clock high period	See (2)			20	µs

(1) The bq30z5x-R1 times out when any clock low exceeds $t_{TIMEOUT}$.
(2) t_{HIGH}, Max, is the minimum bus idle time.

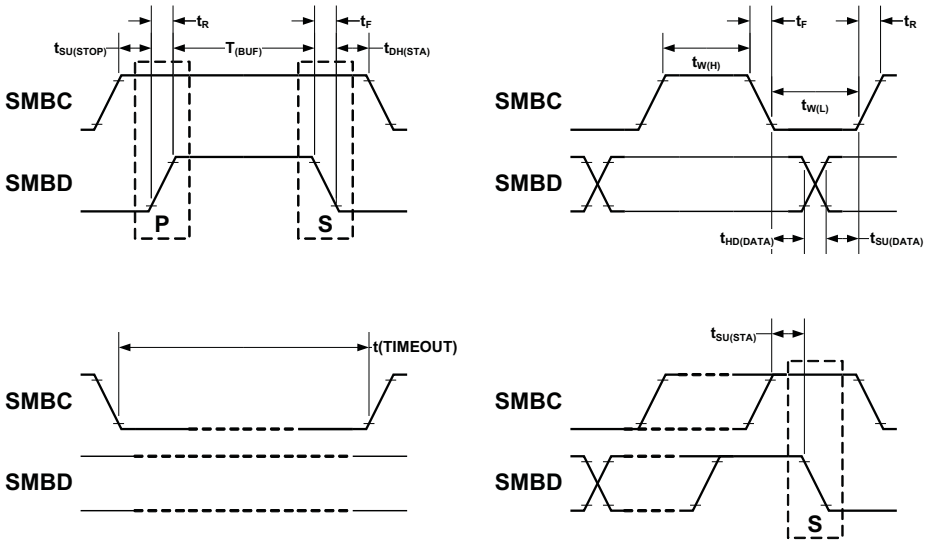


Figure 8. SMBus Timing Diagram

FEATURE SET

Protections Safety Features

The bq30z50-R1 supports a wide range of battery and system protection features that can easily be configured. The Protections safety features include:

- Cell Undervoltage Protection
- Cell Undervoltage I*R Compensated Protection
- Cell Overvoltage Protection
- Overcurrent in Charge Protection 1 and 2
- Overcurrent in Discharge Protection 1 and 2
- Overload in Discharge Protection
- Short Circuit in Charge Protection
- Short Circuit in Discharge Protection 1 and 2
- Over Temperature in Charge Protection
- Over Temperature in Discharge Protection
- Over Temperature FET protection
- SBS Host Watchdog Protection
- Pre Charge Timeout Protection
- Fast Charge Timeout Protection
- Over Charge Protection
- Over ChargingCurrent() Protection
- Over ChargingVoltage() Protection

Permanent Fail Safety Features

The Permanent Fail features of the bq30z50-R1 can be used to indicate more serious faults via the SAFE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. Upon a Permanent Fail event triggers critical system information is written to non volatile memory to simplify failure analysis. In addition the black box stores the sequence of safety events also into non volatile memory to simplify failure analysis. The Permanent Fail protection features include:

- Cell Undervoltage
- Cell Overvoltage
- Copper Deposition
- Over Temperature Cell
- Over Temperature FET
- QMAX Imbalance
- Cell Balancing
- Capacity Degradation
- Impedance
- Voltage Imbalance at Rest
- Voltage Imbalance Active
- Charge FET
- Discharge FET
- Thermistor
- Chemical FUSE
- AFE Register
- AFE Communication
- 2nd-Level Protection
- PTC
- Instruction Flash

- Open Cell Tab Connection
- Data Flash

Charge Control Features

The bq30z50-R1 charge control features include:

- Supports JEITA temperature ranges T1, T2, T3, T4, T5, T6. Reports charging voltage and charging current according to the active temperature range.
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges, and allows for varying the charging current according to the cell voltage.
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts.
- Determines the chemical state of charge of each battery cell using Impedance Track™ and can reduce the charge difference of the battery cells in fully charged state of the battery pack gradually using cell balancing algorithm during rest and charging. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms.

Gas Gauging

The bq30z50-R1 uses the Impedance Track™ Technology to measure and calculate the available charge in battery cells. The achievable accuracy is better than 1% error over the lifetime of the battery and there is no full charge discharge learning cycle required. See the *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application report (SLUA364B) for further details.

Lifetime Data Logging Features

The bq30z50-R1 offers extended lifetime data logging where important measurements are stored for warranty and analysis purposes. The data monitored includes *lifetime*:

- Maximum cell voltage cell0, cell1, cell2, cell3
- Minimum cell voltage cell0, cell1, cell2, cell3
- Maximum cell voltage delta
- Maximum charge current
- Maximum discharge current
- Maximum average discharge current
- Maximum average discharge power
- Maximum cell temperature
- Minimum cell temperature
- Maximum cell temperature delta
- Maximum device temperature
- Minimum device temperature
- Maximum FET temperature
- Total accumulated safety events and last safety event in term of charging cycle
- Total accumulated charging events and charging events
- Total accumulated gauging events and gauging events
- Total accumulated cell balancing time cell0, cell1, cell2, cell3
- Total device f/w runtime
- Accumulated runtime in JEITA under temperature range
- Accumulated runtime in JEITA low temperature range
- Accumulated runtime in JEITA standard temperature range
- Accumulated runtime in JEITA recommended temperature range

- Accumulated runtime in JEITA high temperature range
- Accumulated runtime in JEITA over temperature range

Authentication

- The bq30z50-R1 supports authentication by the host using SHA-1.
- SHA-1 authentication by the gas gauge is required for unsealing and full access.

Power Modes

The bq30z50-R1 supports three power modes to reduce power consumption:

- In Normal Mode, the bq30z50-R1 performs measurements, calculations, protection decisions, and data updates in 0.25-s intervals. Between these intervals, the bq30z50-R1 is in a reduced power stage.
- In Sleep Mode, the bq30z50-R1 performs measurements, calculations, protection decisions, and data update in adjustable time intervals. Between these intervals, the bq30z50-R1 is in a reduced power stage. The bq30z50-R1 has a wake function that enables exit from Sleep mode when current flow or failure is detected.
- In Shutdown Mode, the bq30z50-R1 is completely disabled.
- In Ship Mode, the bq30z50-R1 enters a low-power mode with no voltage, current, and temperature measurements, the FETs are turned off, and the MCU is in a halt state. The device will wake up on SMBus communication detection.

Configuration

System Present Operation

The bq30z50-R1 checks the $\overline{\text{PRES}}$ pin periodically (1s). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the bq30z50-R1 detects this as system present.

BATTERY PARAMETER MEASUREMENTS

Charge and Discharge Counting

The bq30z50-R1 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from –0.25 V to 0.25 V. The bq30z50-R1 detects charge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is negative. The bq30z50-R1 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nVh.

Voltage

The bq30z50-R1 updates the individual series cell voltages at 0.25-s intervals. The internal ADC of the bq30z50-R1 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track™ gas-gauging.

Current

The bq30z50-R1 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5 mΩ to 20 mΩ typ. sense resistor.

Auto Calibration

The bq30z50-R1 provides an auto-calibration feature to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The bq30z50-R1 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s.

Temperature

The bq30z50-R1 has an internal temperature sensor and inputs for four external temperature sensors. All five temperature sensor options are individually enabled and configured for cell or FET temperature. Two configurable thermistor models are provided to allow the monitoring of cell temperature in addition to FET temperature which may be of a higher temperature type.

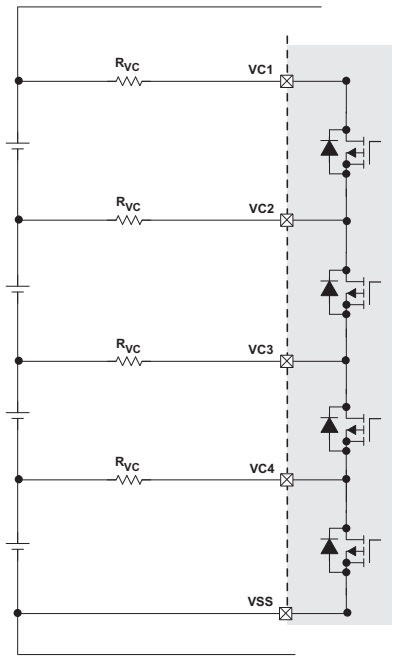
CELL BALANCING

The device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device internal bypass is used up to 10 mA can be bypassed and multiple cells can be bypassed at the same time. Higher cell balance current can be achieved by using external cell balancing circuit. In external cell balancing mode only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge need to be bypassed to balance the capacity of all cells.

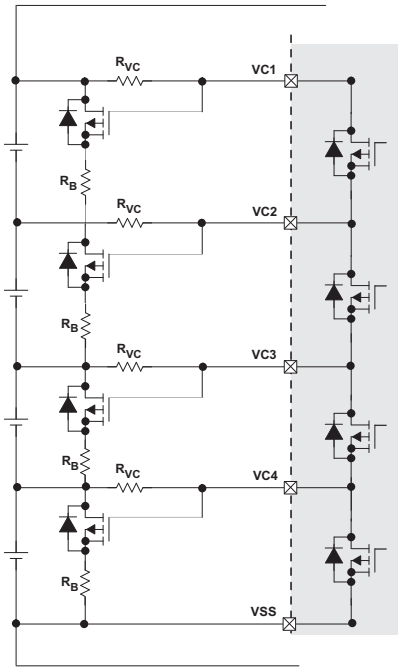
Internal Cell Balancing

When internal cell balancing is configured, the cell balance current is defined by the external resistor R_{VC} at the VCx input.



External Cell Balancing

When internal cell balancing is configured, the cell balance current is defined by R_B. Only one cell at a time can be balanced.



bq30z50-R1 Application Schematic

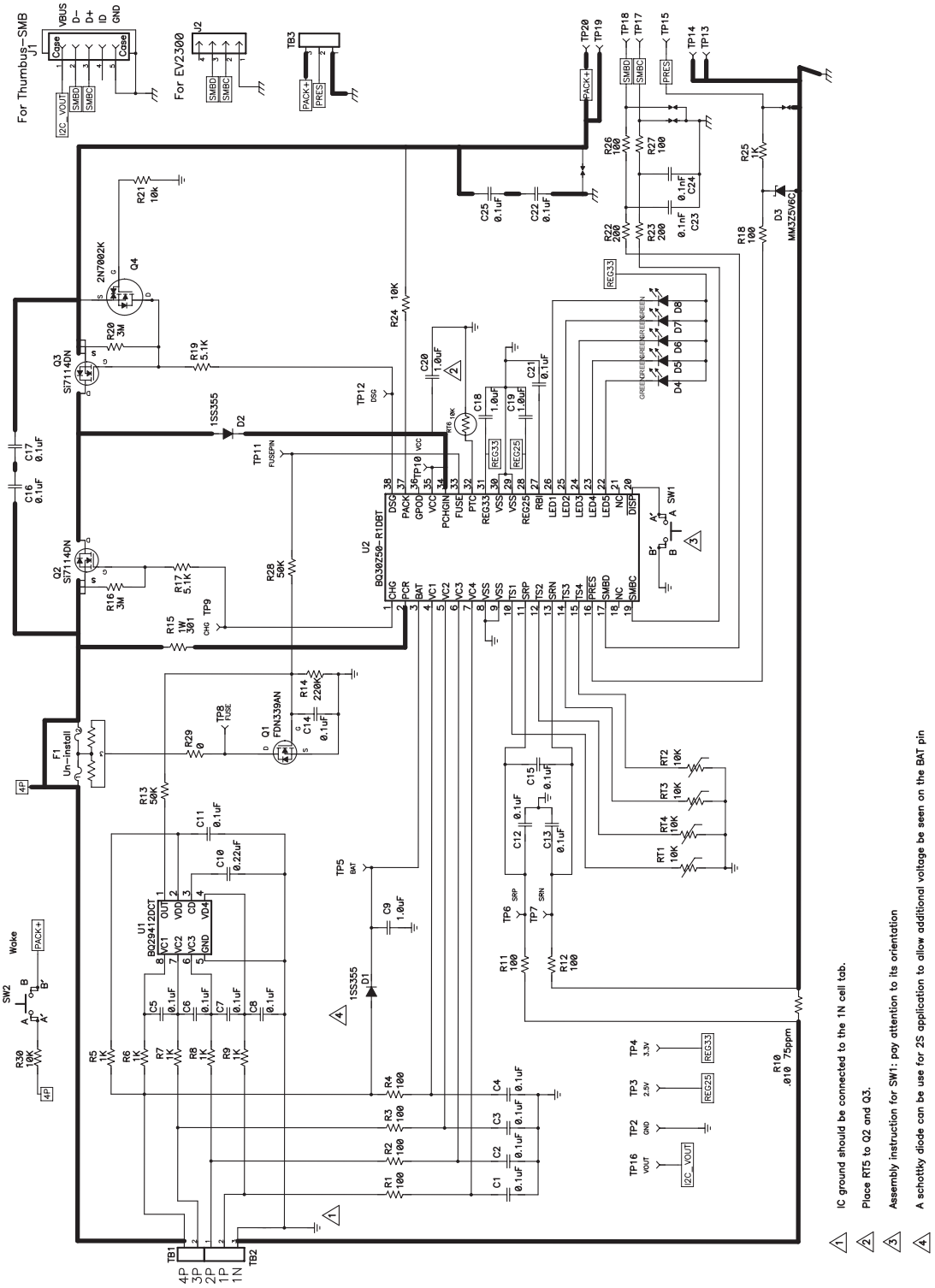


Figure 9. bq30z50_R1 Schematic

bq30z55-R1 Application Schematic

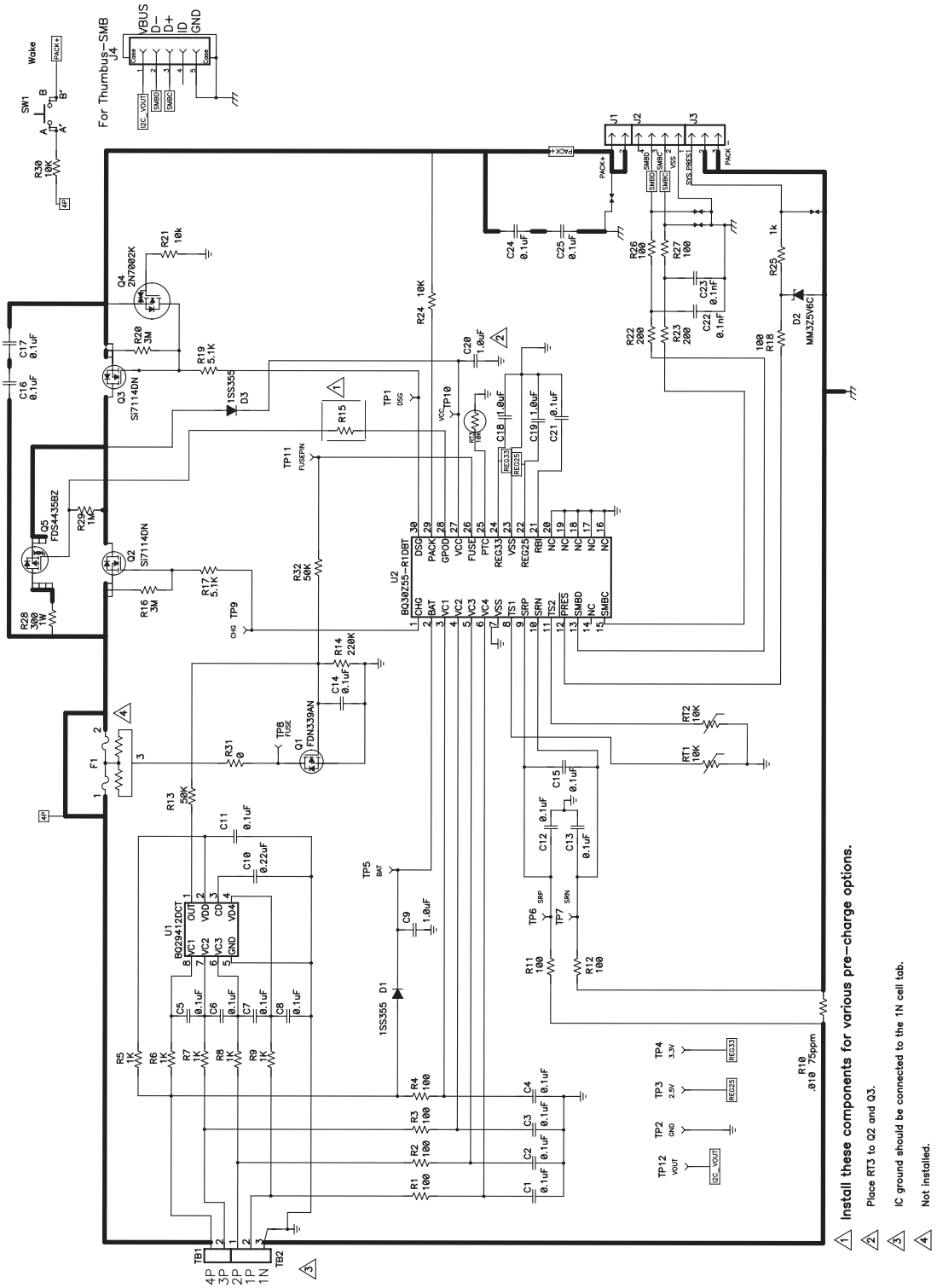
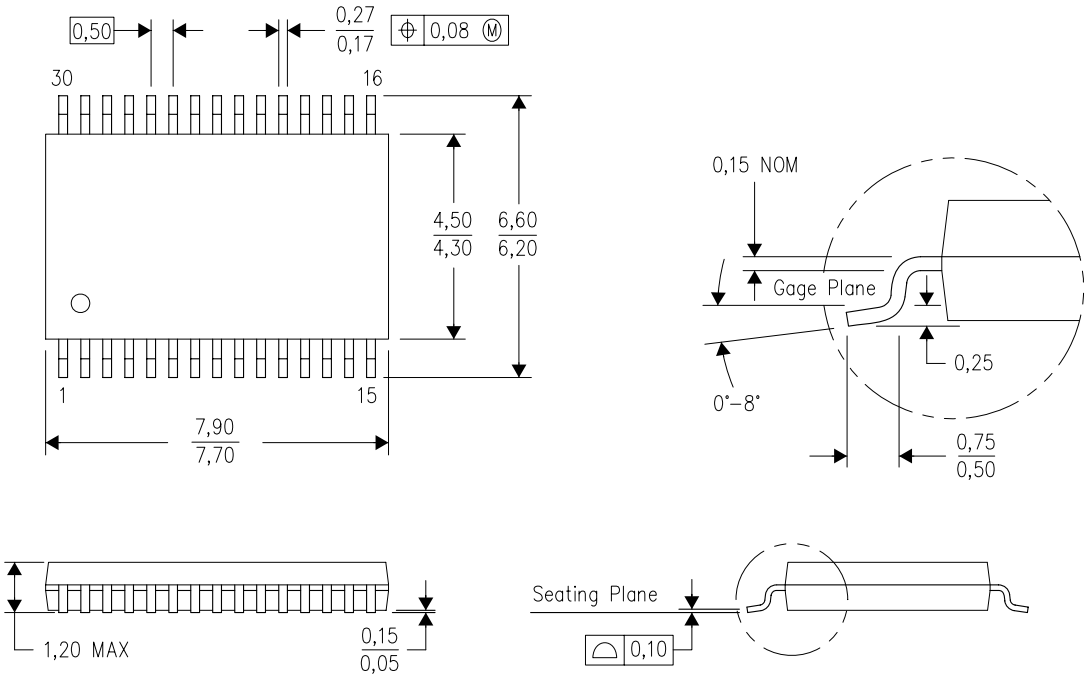


Figure 10. bq30z55-R1 Schematic

DBT (R–PDSO–G30) PLASTIC SMALL OUTLINE



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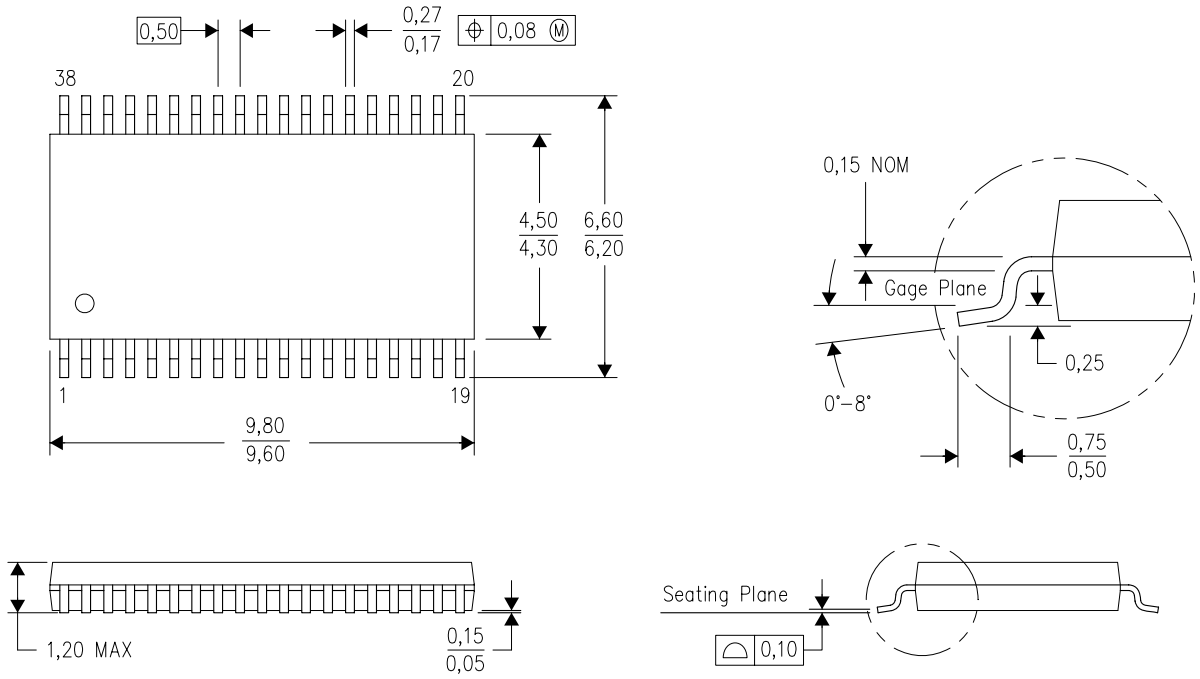
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE



4073252-6/I 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ30Z55DBT-R1	PREVIEW	TSSOP	DBT	30		TBD	Call TI	Call TI	
BQ30Z55DBTR-R1	PREVIEW	TSSOP	DBT	30		TBD	Call TI	Call TI	

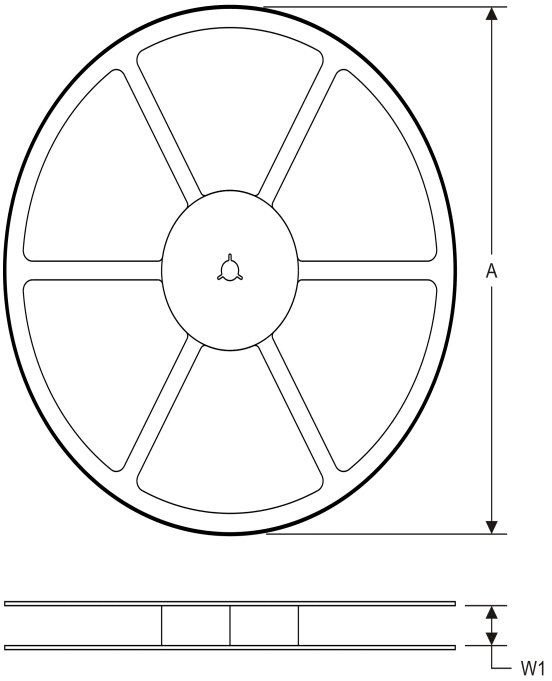
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

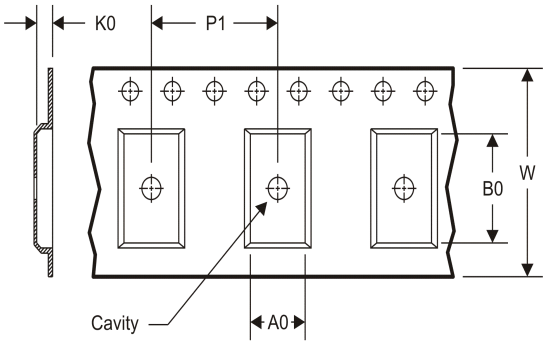
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



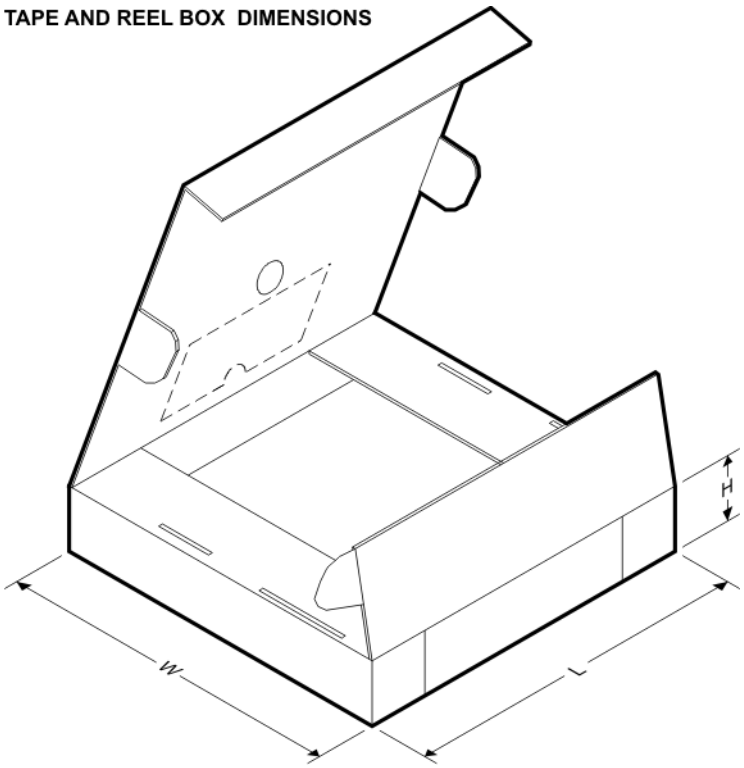
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ30Z50DBTR	TSSOP	DBT	38	0	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ30Z50DBTR	TSSOP	DBT	38	0	346.0	346.0	33.0

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