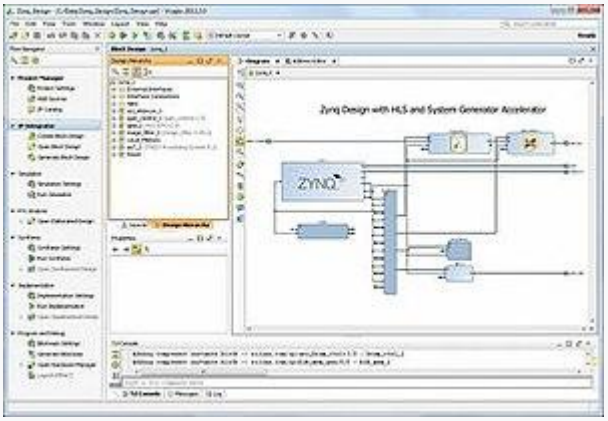
Xilinx Vivado

Vivado Design Suite



Xilinx Vivado Design Suite 2014.2 with Block Design panel (center) and project navigation tree (left)

Developer(s)	Xilinx
Stable release	2018.3[1] / December 10, 2018; 3 months ago[2]
Written in	C++
Operating system	Microsoft Windows, Linux
Available in	English
Type	EDA
License	Shareware
Website	www.xilinx.com/products/design-tools/vivado.html

Vivado Design Suite is a software suite produced by Xilinx for synthesis and analysis of HDL designs, superseding Xilinx ISE with additional features for system on a chip development and high-level synthesis.[3][4][5][6]Vivado represents a ground-up rewrite and re-thinking of the entire design flow (compared to ISE), and has been described by reviewers as "well conceived, tightly integrated, blazing fast, scalable, maintainable, and intuitive".[7][8][9]

Unlike ISE which relied on ModelSim for simulation,[10][11] the Vivado System Edition includes an in-built logic simulator.[12] Vivado also introduces high-level synthesis, with a toolchain that converts C code into programmable logic.[5] Vivado has been described as a "state-of-the-art comprehensive EDA tool with all the latest bells and whistles in terms of data model, integration, algorithms, and performance".[13]

Replacing the 15 year old ISE with Vivado Design Suite took 1000 person-years and cost US $200 million.[14]

Features

Vivado enables developers to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. Vivado is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors.

Vivado was introduced in April 2012,[3] and is an integrated design environment (IDE) with system-to-IC level tools built on a shared scalable data model and a common debug environment. Vivado includes electronic system level (ESL) design tools for synthesizing and verifying C-based algorithmic IP; standards based packaging of both algorithmic and RTL IP for reuse; standards based IP stitching and systems integration of all types of system building blocks; and the verification of blocks and systems.[15] A free version WebPACK Edition of Vivado provides designers with a limited version of the design environment.[16]

Components

The **Vivado High-Level Synthesis** compiler enables C, C++ and SystemC programs to be directly targeted into Xilinx devices without the need to manually create RTL.[17][18][19] Vivado HLS is widely reviewed to increase developer productivity, and is confirmed to support C++ classes, templates, functions and operator overloading.[20][18] Vivado 2014.1 introduced support for automatically converting OpenCL kernels to IP for Xilinx devices.[21][18] OpenCL kernels are programs that execute across various CPU, GPU and FPGA platforms.[18][21]

The **Vivado Simulator** is a component of the Vivado Design Suite. It is a compiled-language simulator that supports mixed-language, TCL scripts, encrypted IP and enhanced verification.

The **Vivado IP Integrator** allows engineers to quickly integrate and configure IP from the large Xilinx IP library. The Integrator is also tuned for MathWorks Simulinkdesigns built with Xilinx's System Generator and Vivado High-Level Synthesis.[22]

The **Vivado TCL Store** is a scripting system for developing addons to Vivado, and can be used to add to and modify Vivado's capabilities.[21] TCL stands for Tool Command Language, and is the scripting language on which Vivado itself is based.[21] All of Vivado's underlying functions can be invoked and controlled via TCL scripts.[21]

Device Support

As of 2018, Xilinx recommends Vivado Design Suite for new designs with Ultrascale, Ultrascale+, Virtex-7, Kintex-7, Artix-7, and Zynq-7000.[23]

Vivado supports newer high capacity devices, and speeds the design of programmable logic and I/O.[24] Vivado provides faster integration and implementation for programmable systems into devices with 3D stacked silicon interconnect technology, ARM processing systems, analog mixed signal (AMS), and many semiconductor intellectual property (IP) cores.[25]

Vivado is targeted at Xilinx's larger FPGAs, and is slowly replacing Xilinx ISE as their mainline tool chain. As of 2014, Vivado covers Xilinx's mid-scale and large FPGAs, and ISE covered the mid-scale and smaller FPGAs and all CPLDs.

V·T·E	Programmable logic		[hide]
Concepts	ASIC · SoC · FPGA (Logic block) · CPLD · EPLD · PLA · PAL · GAL · PSoC · Reconfigurable computing (Xputer) · Soft microprocessor · Circuit underutilization · High-level synthesis · Hardware acceleration		
Languages	Verilog (A · AMS) · VHDL (AMS · VITAL) · SystemVerilog (DPI) · SystemC · AHDL · Handel-C · PSL · UPF · PALASM · ABEL · CUPL · OpenVera · C to HDL · Flow to HDL · MyHDL · JHDL · ELLA		
Companies	Accellera · Actel · Achronix · AMD · Aldec · Atmel · Cadence · Cypress · Duolog · Forte · Intel (Altera) · Lattice · National · Mentor Graphics · Microsemi · Signetics · Synopsys (Magma · Virage Logic) · Texas Instruments · Tabula · Xilinx		
Products	Hardware	iCE · Stratix · Virtex	
	Software	Altera Quartus · Xilinx ISE · **Xilinx Vivado** · ModelSim · VTR · Simulators	
	IP	Proprietary	ARC · ARM Cortex-M · LEON · LatticeMico8 · MicroBlaze · PicoBlaze · Nios · Nios II
		Open-source	JOP · LatticeMico32 · OpenCores · OpenRISC (1200) · RISC-V · Zet