1. INTRODUCTION

1.1 DESCRIPTION

The TIM9904A four-phase clock generator/driver is a 20-pin dual-in-line package peripheral device designed for use with the Texas Instruments TMS 9900 microprocessor family and other microprocessors. The TIM9904A internal oscillator is controlled by a fundamental crystal or an external oscillator. The TIM9904A is fabricated using low-power Schottky technology and is available in both plastic and ceramic packages.

1.2 KEY FEATURES

- Clock generator/driver for the TMS 9900 or other microprocessors
- MOS and TTL four-phase outputs
- Self-contained oscillator crystal-controlled
- External oscillator can be used
- Clock D-type flip-flop with Schmitt-trigger input for reset signal synchronization
- Standard 20-pin plastic and ceramic packages

2. ARCHITECTURE

The TIM9904A clock generator/driver (Figure 1) comprises an oscillator, a divide-by-four counter with gating to generate four clock phases, high-level (12-volt) output drivers, low-level (5-volt) complementary output drivers, a D-type flip-flop controlled by an external signal, and a $\phi 3$ clock. The four high-level clock phases provide clock inputs to a TMS 9900 (or other) microprocessor. The four complementary TTL-level clocks can be used to time memory or other logic functions in a TMS 9900 computer system. The D-type flip-flop can be used, for example, to provide a reset signal to a TMS 9900, timed by $\phi 3$, on receipt of and input to the FFD input from power turn-on or a manual switch closure. Other applications are possible. A safety feature incorporated in the ϕ outputs causes the ϕ outputs to go low if an open occurs in the V_{CC} supply common to TIM9904A and TMS 9900, thus protecting the TMS 9900.

The frequency of the internal oscillator is established by a quartz crystal. The LC circuit connected to the tank inputs selects the desired crystal frequency. An external oscillator may be used, if desired.

3. DEVICE OPERATION

Connected to a TMS 9900 as shown in Figure 2, the TIM9904A oscillator operates with a quartz fundamental crystal and an LC circuit connected to the tank terminal. For operation of the TMS 9900 microprocessor at 3 MHz, the frequency reference requires a fundamental frequency of 12 MHz (4 X 3 MHz). The quartz crystal used as a frequency reference should be designed for series-mode operation with a resistance between 20 and 75 ohms and capable of a minimum of 6 mW power dissipation. Typical frequency tolerance is +/− 0.005 percent. For 4 MHz operation, a 16 MHz fundamental crystal is used. For best results, the LC circuit connected across the tank terminals should be tuned to the fundamental crystal frequency. The crystal and tank circuit should be physically located as close as possible to the TIM9904A. When an internal oscillator is used, OSCIN should be connected to V_{CC} through a resistor (4.7 kilohm nominal), and an LC tank circuit must be connected to the tank inputs.

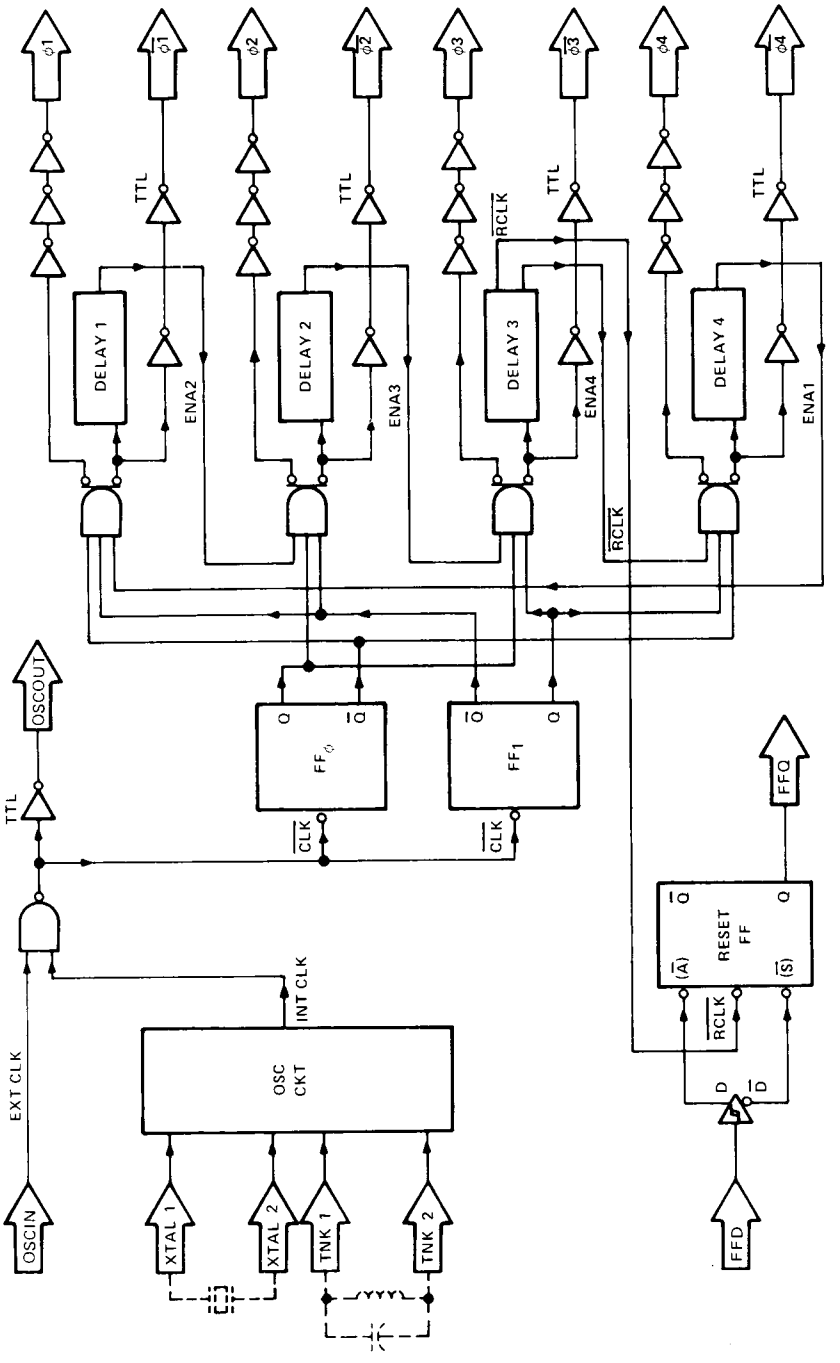


FIGURE 1 – TIM9904A BLOCK DIAGRAM

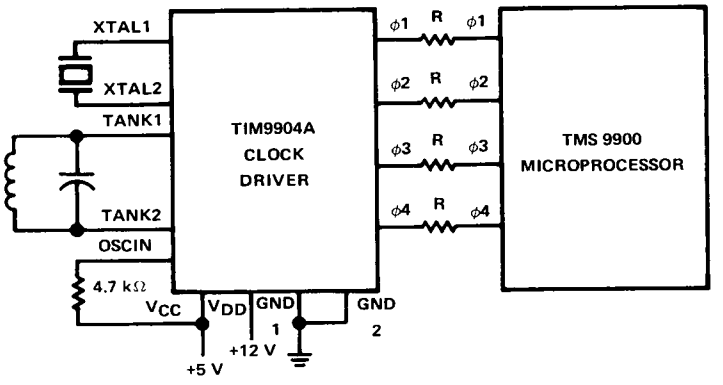


FIGURE 2 – TIM9904A CRYSTAL-CONTROLLED OPERATION

Resistors between the TIM9904A $\phi1$, $\phi2$, $\phi3$, $\phi4$, outputs and the corresponding clock input terminals of the TMS 9900 should be 16 ohms +/–20 percent (see Figure 2). The purpose of the resistors is to minimize overshoot and undershoot. The required resistance value is dependent on circuit layout; clock signal interconnections should be as short as possible.

An external oscillator can be used by connecting the crystal terminals to V_{CC} and a 130 ohm (+/–10 percent) resistor between the tank pins. The external oscillator must have a frequency four times the desired output clock frequency with a minimum of 25 percent and a maximum of 50 percent duty cycle. (See Figure 3)

The output clocks are generated from the rising edge of the OSCIN signal such that a varying pulse width will not affect the pulse width (and duty cycle) of the $\phi1$ - $\phi4$ outputs.

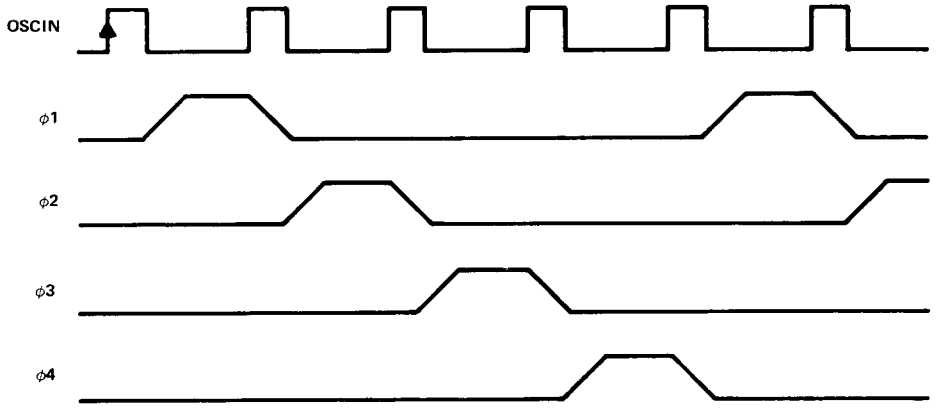


FIGURE 3 – EXTERNAL OSCILLATOR TIMING FOR USE WITH TIM9904A

The D-type flip-flop associated with TIM9904A pins FFD and FFQ provides a power-on reset and a manual reset to the TMS 9900 as shown in Figure 4. A Schmitt-trigger circuit driving the D input generates a fast-rising wave form when the input voltage rises to a specific value. At power turn-on, voltage across the 0.1 μF capacitor in Figure 4 will rise towards V_{CC}. This circuit provides a delay that resets the TMS 9900 at any time. The TMS 9900 HOLD signal could alternatively be actuated by FFD.

The ground terminals GND1 and GND2 are normally connected together and to system ground.

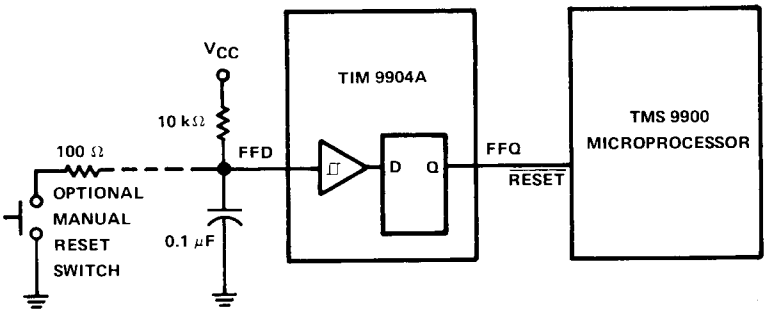


FIGURE 4 – POWER-ON RESET

4. DEVICE APPLICATION

4.1 MODES OF OPERATION

The TIM9904A may be used in one of the following modes to provide clocking for the TMS 9900 or other microprocessor:

- Fundamental operation – fundamental crystal with tank circuit
- Externally-controlled operation – internal oscillator disabled; TTL input signal determines frequency.

4.1.1 Fundamental Operation

If a crystal is available with a fundamental frequency four times the required frequency, the TANK1 and TANK2 inputs are connected to each other through a tank circuit as shown in Figure 5. The PRESET/OSCIN input is held at high level.

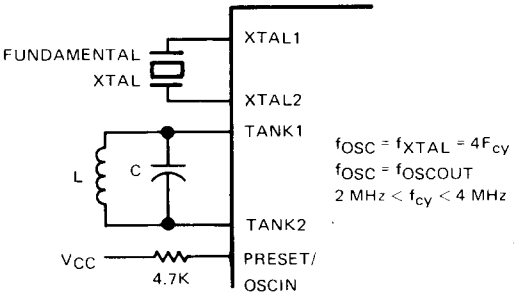


FIGURE 5 – FUNDAMENTAL FREQUENCY CRYSTAL OPERATION

4.1.2 Externally Controlled Operation

If a TTL signal is available with the appropriate frequency and waveform, it may be connected to the PRESET/OSCIN input of the TIM9904A with a resistor between the tank pins and connection of the crystal inputs to V_{CC}.

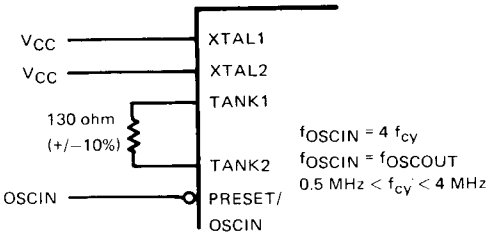


FIGURE 6 – EXTERNALLY-CONTROLLED OPERATION

4.2 COMPONENT SELECTION

The criteria for selecting the values of the discrete components used with the TIM9904A are discussed in this section.

4.2.1 Crystal

The following crystal specifications are suggested:

- Series resonant, 20-75 ohm series resistance 6 mW maximum power dissipation.
- FXTAL = 4 fcy
- For fcy = 3 MHz, specify 12 MHz fundamental.
- For fcy = 4 MHz, specify 16 MHz fundamental.
- Suggested stability: 0.005 percent from 0°C to 70°C.

4.2.2 Tank Circuit

The tank circuit should have a resonant frequency at the fundamental frequency of the crystal.

The resonant frequency is determined by the equation:

$$fosc = \frac{1}{2\pi\sqrt{LC_T}}$$

Because the value of the capacitance is in the picofarad range, board capacitance must be considered when selecting component values for the LC tank circuit. The board capacitance (CB) will be added to the device capacitance (CD), as shown in Figure 7.

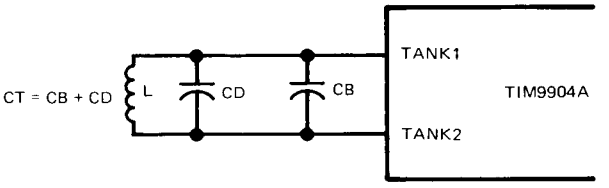


FIGURE 7 – EFFECT OF BOARD ON TANK CIRCUIT RESONANT FREQUENCY

For 16 MHz operation, the following component values may be used:

$L = 6.8\,\mu H$
$CT = 15\ pF$

It is recommended that when CB = CT, a 5 pF capacitor should be added for stability purposes.

For 12 MHz operation, the following component values may be used:

$L = 3.3\,\mu H$
$CT = 50\ pF$

4.2.3 Series Resistors

Resistors with values of 16 ohms +/–20 percent, should be installed between the $\phi 1$-$\phi 4$ outputs of the TIM9904A and the corresponding inputs of the TMS 9900. These serve three purposes:

- Reduce overshoot and ringing
- Protect the drivers from overvoltage and undervoltage signals
- Reduce device power consumption

Connect the resistors as illustrated in Figure 8.

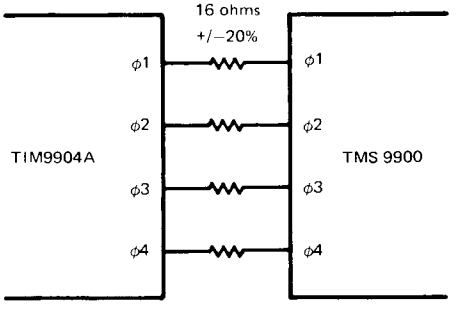


FIGURE 8 – SERIES MOS CLOCK RESISTORS

Be sure the resistor values chosen do not cause V_{IH} on the ϕ lines entering the TMS 9900 to fall below specifications.

4.2.4 Bypass Capacitors

Bypass capacitors are needed on the V_{CC} and V_{DD} lines to filter out noise caused by the device switching. The V_{DD} line is critical; the capacitor must be physically as close to the device as possible.

4.2.5 $\overline{\phi}$ TTL Outputs

Care must be exercised when designing printed circuit layouts for the $\overline{\phi}$ TTL signal. Poor layout techniques, under certain circumstances, can cause negative undershoot on high-to-low transitions on the $\overline{\phi}$ TTL output signals. This can cause damage to MOS devices, which do not have negative substrate supplies, i.e. -5 V_{BB}.

4.3 TIM 9904A TERMINAL ASSIGNMENTS

TABLE 1 – TIM9904A TERMINAL ASSIGNMENTS

SIGNATURE	PIN	I/O	DESCRIPTION
TANK 1	1	I	Tank circuit connection
TANK 2	2	I	Tank circuit connection
GND 1	3		Ground reference
FFQ	4	O	Output of D flip-flop
FFD	5	I	D-input of Schmitt-triggered flip-flop
$\overline{\phi}4$ TTL	6	O	TTL phase 4 inverted
$\overline{\phi}3$ TTL	7	O	TTL phase 3 inverted
$\phi3$	8	O	MOS phase 3
$\phi4$	9	O	MOS phase 4
GND 2	10		Ground reference
$\phi2$	11	O	MOS phase 2
$\phi1$	12	O	MOS phase 1
V_{DD}	13	I	Supply voltage: 12 V nominal
$\overline{\phi}1$ TTL	14	O	TTL phase 1 inverted
$\overline{\phi}2$ TTL	15	O	TTL phase 2 inverted
OSCOUT	16	O	Oscillator output
OSCIN	17	I	TTL external oscillator input
XTAL1	18	I	Crystal
XTAL2	19	I	Crystal
V_{CC}	20	I	Supply voltage: 5 V nominal

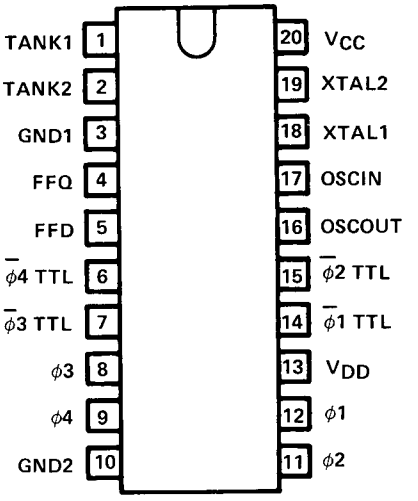


FIGURE 9 – CHIP PIN DESIGNATIONS

5. ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Supply voltage: V_{CC} (see Note 1) . . . . . 7 V
V_{DD} (see Note 1) . . . . . 13 V
Input voltage: OSCIN . . . . . 5.5 V
FFD . . . . . −0.5 V to 7 V
Operating free-air temperature range: NL, JL . . . . . 0°C to 70°C
NA, JA . . . . . −40°C to 85°C
Storage temperature range (NL, JL) . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground. Pins 3 and 10 should be connected to the same ground.

5.2 RECOMMENDED OPERATING CONDITIONS

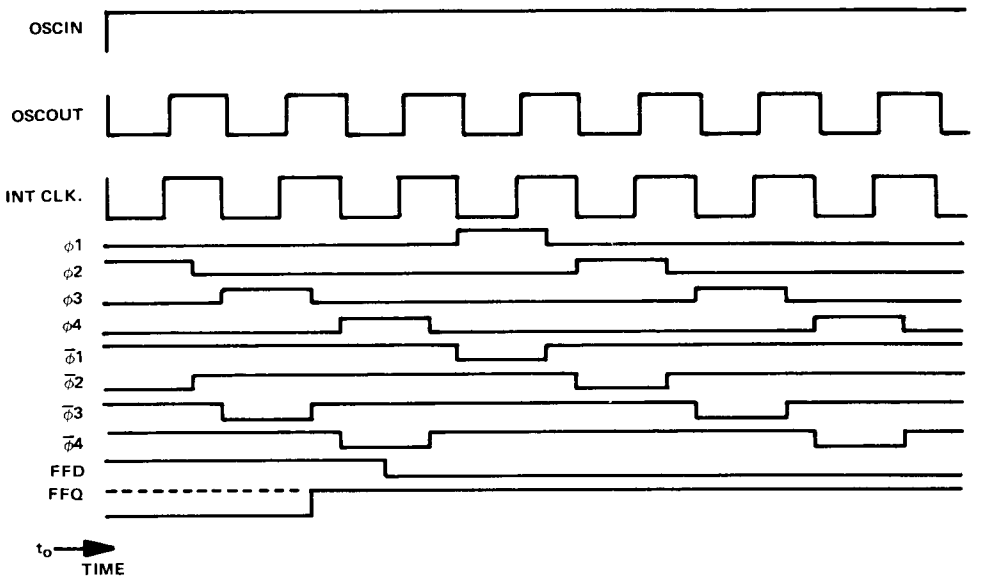
PARAMETER			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
Supply voltage, V_{DD}			11.4	12	12.6	V
High-level output current, I_{OH}	$\phi1, \phi2, \phi3, \phi4$				−100	μA
	All others				−400	
Low-level output current, I_{OL}	$\phi1, \phi2, \phi3, \phi4$				4	mA
	All others				8	
Internal oscillator frequency, f_{osc}	4 MHz			16		MHz
	3 MHz			12		
External oscillator pulse width, $t_{w(osc)}$	4 MHz		15	25		ns
	3 MHz		19	30		
Setup time, FFD input (with respect to falling edge of $\phi3$), t_{su}			70			ns
Hold time, FFD input (with respect to falling edge of $\phi3$), t_h			0			ns
Operating free-air temperature, T_A	NL, JL		0		70	°C
	NA, JA		−40		85	

5.3 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage	FFD					0.5	V
		OSCIN					0.8	
$V_{T+} - V_{T-}$	Hysteresis	FFD			0.4	0.8		V
V_{IK}	Input clamp voltage		V_{CC}=4.75 V, V_{DD}=11.4 V	I_I=18 mA			−1.5	V
V_{OH}	High-level output voltage	$\phi1, \phi2, \phi3, \phi4$	V_{CC}=4.75 V	I_{OH}=−100 μA	V_{DD}−2	V_{DD}−1,5	V_{DD}	V
		Other outputs	V_{DD}=11.4 V to 12.6 V	I_{OH}=−400 μA	2.7	3.4		
V_{OL}	Low-level output voltage	$\phi1, \phi2, \phi3, \phi4$	V_{CC}=4.75 V, V_{DD}=11.4 V	I_{OL}=4 mA		0,25	0.4	V
		Other outputs		I_{OL}=4 mA		0,25	0.4	
				I_{OL}=8 mA		0,35	0.5	
I_I	Input current at maximum input voltage	FFD	V_{CC}=5.25 V, V_{DD}=12.6 V	V_I=7 V			0,1	mA
		OSCIN		V_I=5.5 V			0.3	
I_{IH}	High-level input current	FFD	V_{CC}=5.25 V, V_{DD}=12.6 V, V_I=2.7 V				20	μA
		OSCIN					60	
I_{IL}	Low-level input current	FFD	V_{CC}=5.25 V, V_{DD}=12.6 V, V_I=0.4 V				−0.4	mA
		OSCIN					−1.6	
I_{OS}	Short circuit output current§	All except $\phi1, \phi2, \phi3, \phi4$	V_{CC}=5.25 V		−10		−100	mA
I_{CC}	Supply current from V_{CC}	0°C to 70°C	V_{CC}=5.25 V, FFD and OSCIN at GND, Output open.			65	85	mA
		−40°C to 85°C				70	105	
$I_{CC(av)}$	Supply current from V_{CC} (3 MHz)	0°C to 70°C	V_{CC}=5.25 V, V_{DD}=12.6 V, f_{out}=3 MHz			71	95	mA
		−40°C to 85°C				75	105	
$I_{CC(av)}$	Supply current from V_{CC} (4 MHz)	0°C to 70°C	V_{CC}=5.25 V, V_{DD}=12.6 V, f_{out}=4 MHz			73	95	mA
		−40°C to 85°C				80	110	
I_{DD}	Supply from V_{DD}	0°C to 70°C	V_{CC}=5.25 V, V_{DD}=12.6 V, FFD and OSCIN at GND outputs open.			14	24	mA
		−40°C to 85°C				15	25	
$I_{DD(av)}$	Supply current from V_{DD} (3 MHz)	0°C to 70°C	V_{CC}=5.25 V, V_{DD}=12.6 V, f_{out}=3 MHz			40	48	mA
		−40°C to 85°C				42	50	
$I_{DD(av)}$	Supply current from V_{DD} (4 MHz)	0°C to 70°C	V_{CC}=5.25 V, V_{DD}=12.6 V, f_{out}=4 MHz			47	52	mA
		−40°C to 85°C				47	60	

† All typical values are at V_{CC} = 5 V, V_{DD} = 12 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed 1 second. Outputs $\phi1$, $\phi2$, $\phi3$, and $\phi4$ do not have short-circuit protection.



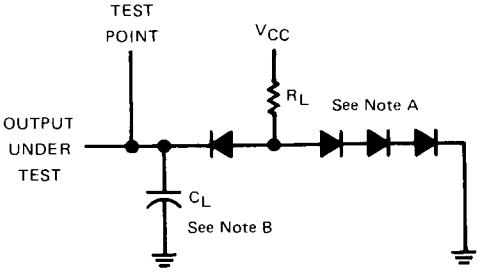
NOTE: Power-up initialization forces φ2 output to logic one first. This approach makes synchronization for testing easier.

FIGURE 10 – TYPICAL PHASE RELATIONSHIPS OF INPUTS AND OUTPUTS

5.4 SWITCHING CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{out}	Output frequency, any ϕ or $\bar{\phi}$TTL	3 MHz	Output loads: $\phi1,\phi3,\phi4$: 150 pF to GND $\phi2$: 200 pF to GND Others: R_L = 2 kΩ C_L = 15 pF	2	3	3.33	MHz
		4 MHz		2	4	4.17	
f_{out}	Output frequency, OSCOUT	3 MHz			12		MHz
		4 MHz			16		
$t_{c(\phi)}$	Cycle time, any ϕ output	3 MHz		300	333	500	ns
		4 MHz		240	250	500	
$t_{r(\phi)}$	Rise time any ϕ output			5		20	ns
$t_{f(\phi)}$	Fall time any ϕ output			5	9	20	ns
$t_{w(\phi)}$	Pulse width, any ϕ output high	3 MHz		40	60		ns
		4 MHz		30			
$t_{d(\phi1L-\phi2H)}$	Delay time, $\phi1$ low to $\phi2$ high			0	1	5	ns
$t_{d(\phi2L-\phi3H)}$	Delay time, $\phi2$ low to $\phi3$ high			0	1	5	ns
$t_{d(\phi3L-\phi4H)}$	Delay time, $\phi3$ low to $\phi4$ high			0	1	5	ns
$t_{d(\phi4L-\phi1H)}$	Delay time, $\phi4$ low to $\phi1$ high			0	1	5	ns
$t_{d(\phi1H-\phi2H)}$	Delay time, $\phi1$ high to $\phi2$ high			55	63		ns
$t_{d(\phi2H-\phi3H)}$	Delay time, $\phi2$ high to $\phi3$ high			55	63		ns
$t_{d(\phi3H-\phi4H)}$	Delay time, $\phi3$ high to $\phi4$ high			55	63		ns
$t_{d(\phi4H-\phi1H)}$	Delay time, $\phi4$ high to $\phi1$ high			55	63		ns
$t_{d(\phi H-\phi TL)}$	Delay time, ϕn high to ϕn TTL low			−20	−13	0	ns
$t_{d(\phi L-\phi TH)}$	Delay time, ϕn low to ϕn TTL high			−20	−13	−5	ns
$t_{d(\phi3L-\phi H)}$	Delay time, $\phi3$ low to FFQ output high			−18	−8	2	ns
$t_{d(\phi3L-\phi L)}$	Delay time, $\phi3$ low to FFQ output low			−10	4	10	ns
$t_{d(OSOH-\phi L)}$	OSCOUT high to any ϕ low			15	25	40	ns
$t_{w(OSO)}$	Minimum OSCOUT pulse width	3 MHz		18	30		ns
		4 MHz		14	25		

† All typical values are at V_{CC} = 5 V, V_{DD} = 12 V and T_A = 25°C.



NOTES: A. All diodes are IN916 or IN3064.
B. C_L includes probe and jig capacitance.

FIGURE 11 – LOAD CIRCUIT

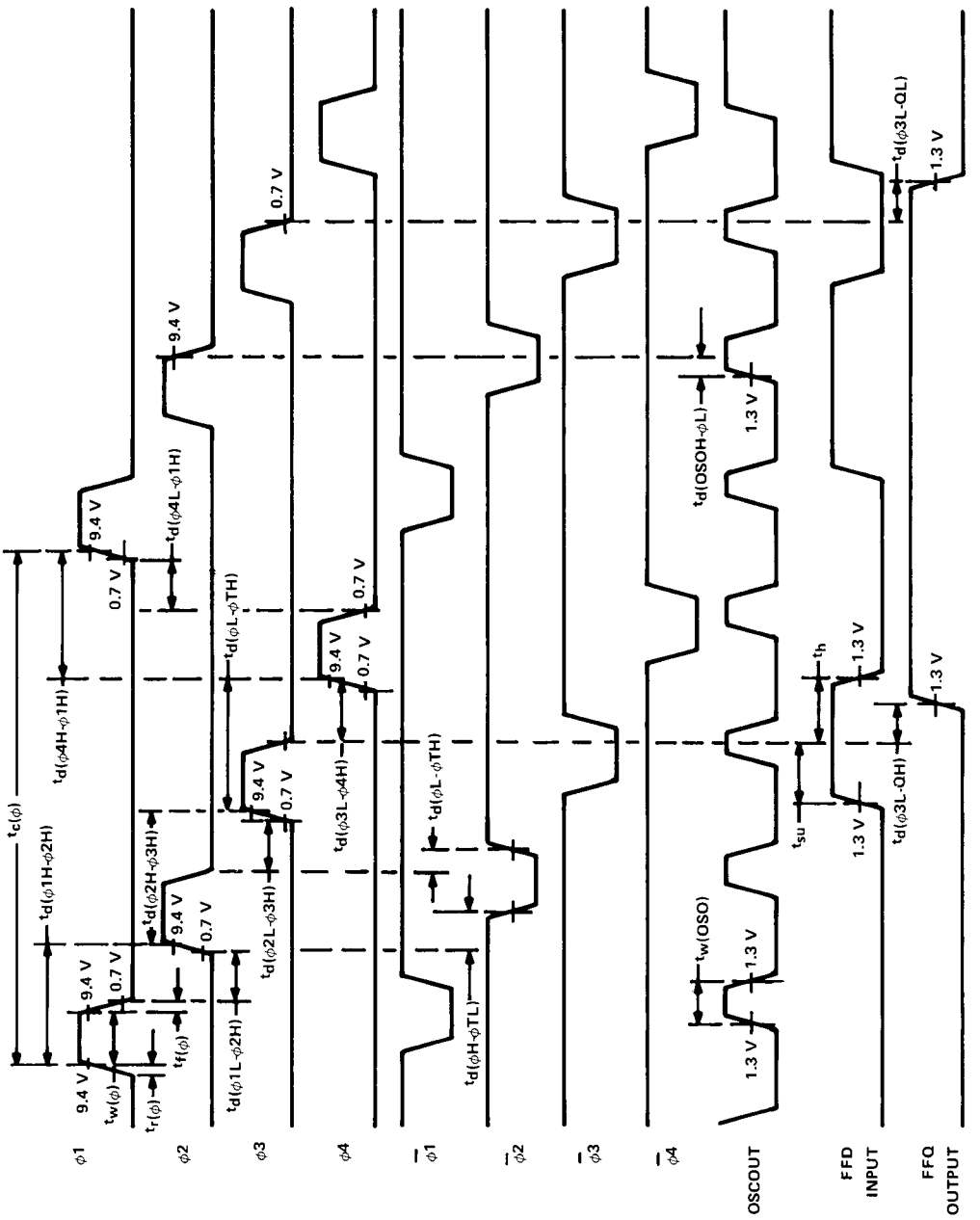
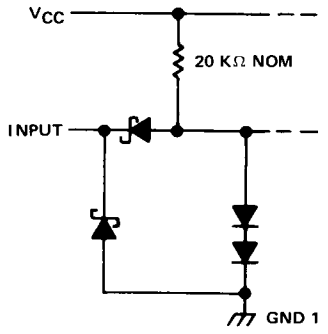


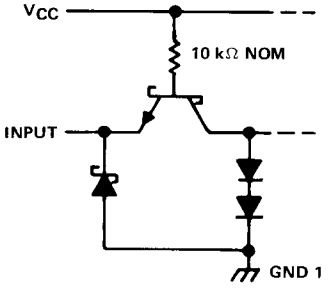
FIGURE 12 – SWITCHING CHARACTERISTICS, VOLTAGE WAVEFORMS

5.5 SCHEMATICS OF INPUTS AND OUTPUTS

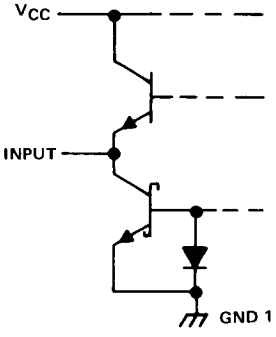
EQUIVALENT OF D INPUT



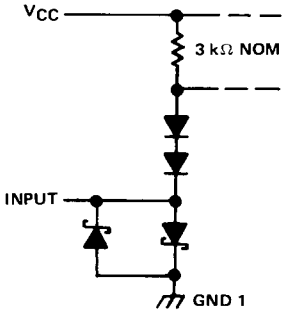
EQUIVALENT OF OSCIN INPUT



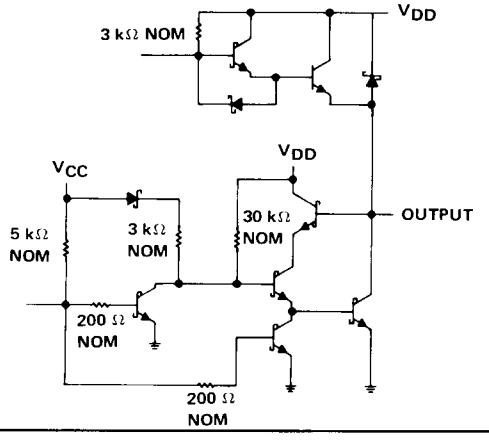
EQUIVALENT OF XTAL 1 AND XTAL 2 INPUTS



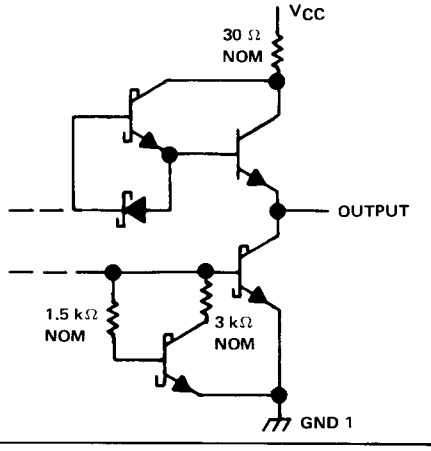
EQUIVALENT OF TANK INPUTS



TYPICAL OF $\phi1,\phi2,\phi3$ AND $\phi4$ OUTPUTS

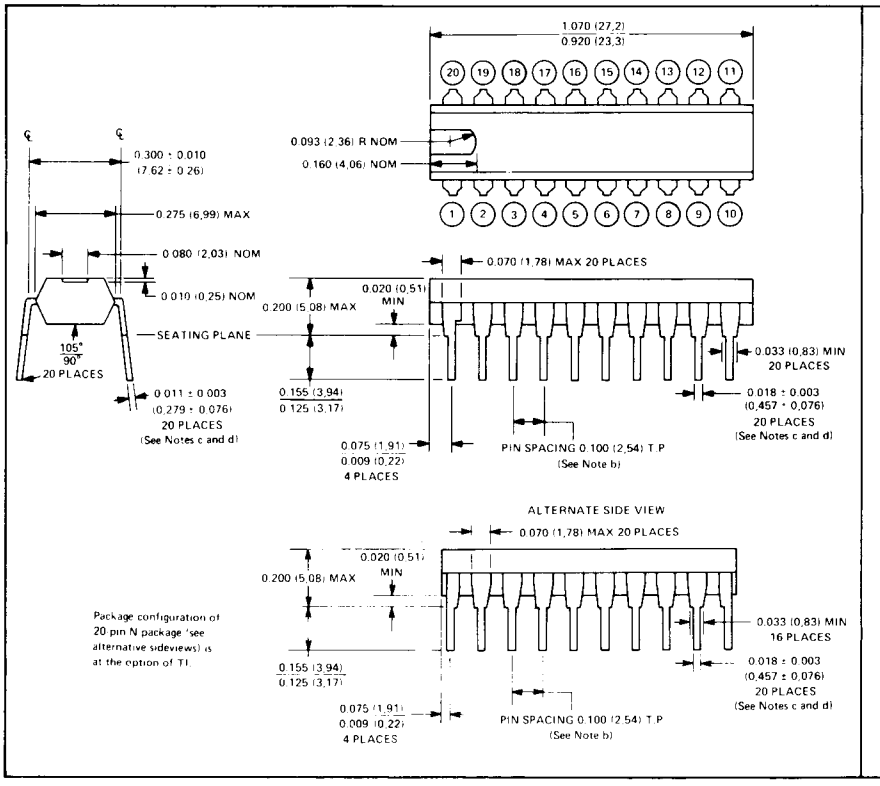


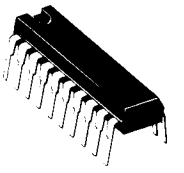
TYPICAL OF OSCOUT, Q, AND ALL ϕ TTL OUTPUTS



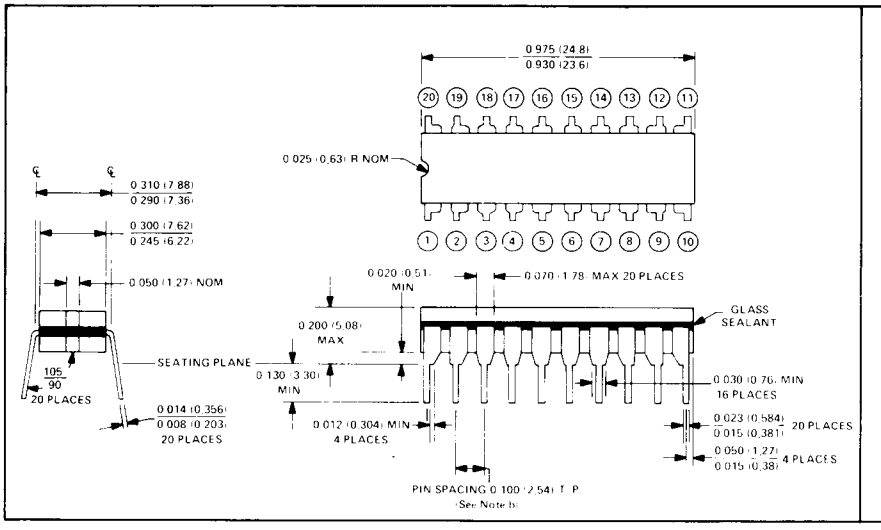
6. MECHANICAL DATA

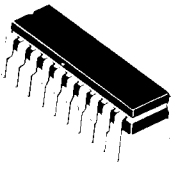
6.1 PLASTIC PACKAGE





6.2 CERAMIC PACKAGE





NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.
c. This dimension does not apply for solder dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 (0,50) above the seating plane.