1 INTRODUCTION

The TMP68HC11E9 is an advanced 8-bit microcontroller (MCU) with highly sophisticated on-chip peripheral capabilities. New design techniques were used to achieve a nominal bus speed of 2.1MHz (@Ta = −40~+85°C)*. In addition, the fully static design allows operation at frequencies down to dc, further reducing power consumption.

* : With the TMP68HC11E9, the 3MHz nominal bus speed is also guaranteed (@Ta = 0 to +70°C). The electrical specifications under 3MHz operation is similar to that of the TMP68HC11E0T-3/E1T-3. Refer to "1. Electrical Specifications" in "2.5 TMP68HC11E0T-3/E1T-3".

1.1 FEATURES

The following are some of the hardware and software highlights.

HARDWARE FEATURES

- 12K Bytes of ROM
- 512 Bytes of EEPROM
- 512 Bytes of RAM (All Saved During Standby) Relocatable to Any 4K Boundary
- Enhanced 16-Bit Timer System:
  Four Stage Programmable Prescaler
  Three Input Capture/Five Output Compare Functions or
  Four Input Capture/Four Output Compare Functions
- 8-Bit Pulse Accumulator Circuit
- Enhanced NRZ Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- Eight Channel, 8-Bit Analog-to-Digital Converter
- Real Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- Available in Plastic Shrink Dual-In-Line Packages, and Plastic Leaded chip Carrier Packages.
- Under development Quad Flat Package

SOFTWARE FEATURES

- Enhanced M6800/M6801 Instruction Set
- 16×16 Integer and Fractional Divide Features
- Bit Manipulation
- WAIT Mode
- STOP Mode

1.2 GENERAL DESCRIPTION

The high-density CMOS technology used on the TMP68HC11E9 combines smaller size and higher speeds with the low power and high noise immunity of CMOS. On-chip memory systems include 12K bytes of ROM, 512 bytes of electrically eraseable

programmable ROM (EEPROM), and 512 bytes of static RAM.

Major peripheral functions are provided on-chip. An eight channel analog-to-digital (A/D) converter is included with eight bits of resolution. An asynchronous serial communications interface (SCI) and a separate synchronous serial peripheral interface (SPI) are included. The main 16-bit free-running timer system has three input capture lines, five output compare lines, and a real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods.

Self monitoring circuitry is included on-chip to protect against system errors. A computer operating properly (COP) watchdog system protects against software failures. A clock monitor system generates a system reset in case the clock is lost or runs too slow. An illegal opcode detection circuit provides a non-maskable interrupt if an illegal opcode is detected.

Two software controlled operating modes, WAIT and STOP, are available to conserve additional power.

A block diagram of the TMP68HC11E9 is shown in Figure 1.1

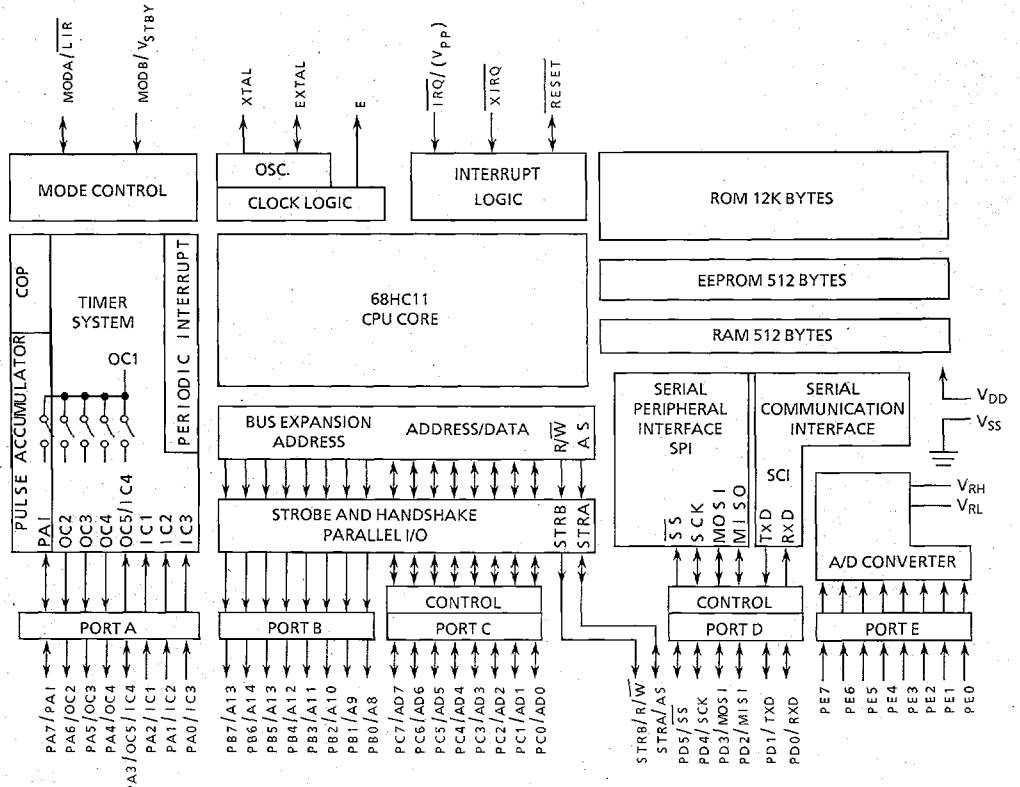

Figure 1.1 TMP68HC11E9 Block Diagram

1.3 PROGRAMMER'S MODEL

In addition to being able to execute all M6800 and M6801 instructions, the TMP68HC11E9 allows execution of 91 new opcodes. Figure 1.2 shows the seven CPU registers which are available to the programmer.

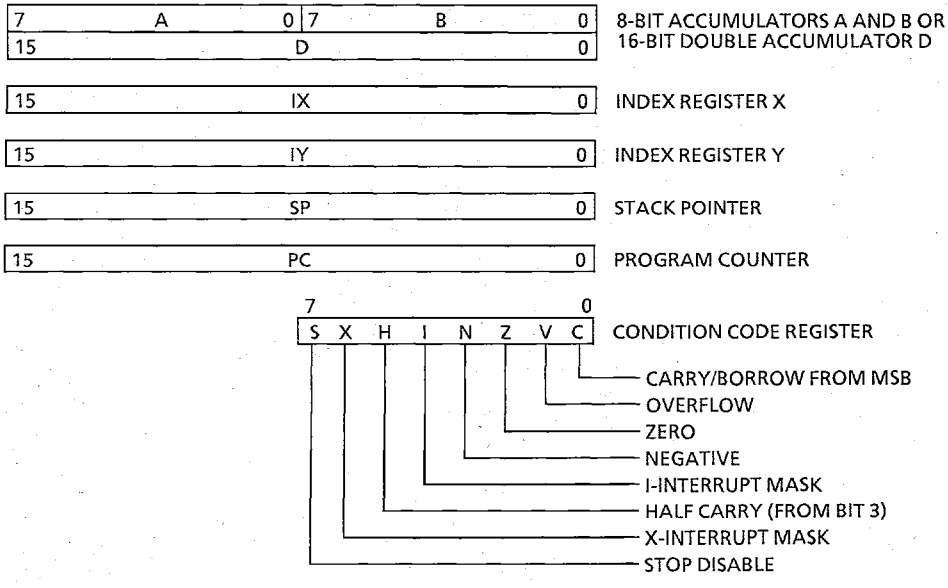

Figure 1.2 Programming Model