Introduction

The following sections are meant to give an overview about what the Qucs software can be used for and how it is used to achieve this.

Qucs is free software licensed under the General Public License (GPL). It can be downloaded from `http://qucs.sourceforge.net` and comes with the complete source code. Every user of the program is allowed and called upon (on a voluntary basis of course) to modify it for their purposes as long as changes are made public. Contact the authors to verify them and finally to incorporate it into the software.

The software is available for a variety of operating systems including

- GNU/Linux
- Windows
- FreeBSD
- MacOS
- NetBSD
- Solaris

On the homepage you'll find the source code to build and install the software. Build instructions are given. Also links for binary packages for certain distributions (e.g. Debian, SuSE, Fedora) can be found.

Once the software has been successfully installed on your system you can start it by issuing the

```
# qucs
```

command or by clicking the appropriate icon on your start menu or desktop. Qucs is a multi-lingual program. So depending on your system's language settings the Qucs graphical user interface (GUI) appears in different languages.

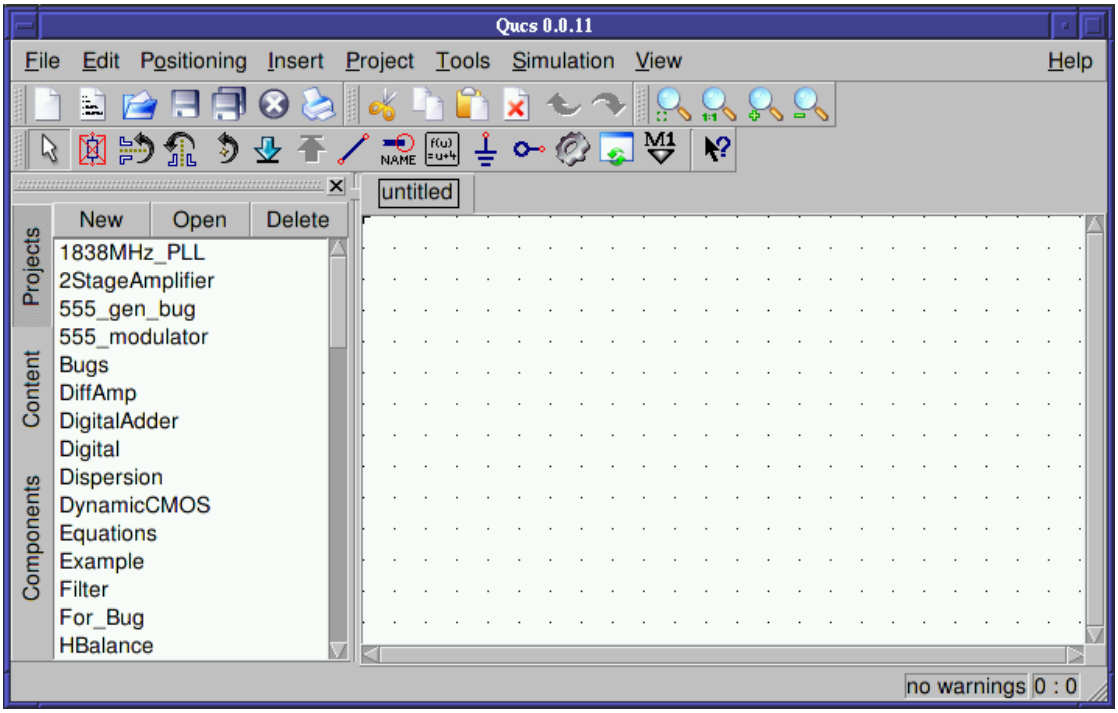

Figure 1: Qucs has been started

On the left hand side you find the **Projects** folder opened. Usually the projects folder will be empty if you use Qucs for the first time. The large area on the right hand side is the schematic area. Above you can find the menu bar and the toolbars.

In the **File** → **Application Settings** menu the user can configure the language and appearance of Qucs.

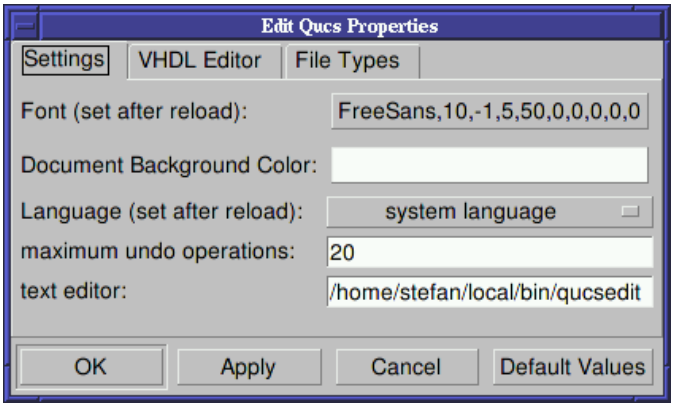

Figure 2: Application setting dialog

To take effect of the language and font settings the application must be closed either via the Ctrl + Q shortcut or the **File** → **Exit** menu entry. Then start Qucs again.

Tool suite

Qucs consists of several standalone programs interacting with each other through the GUI. There are

- the GUI itself,

  The GUI is used to create schematics, setup simulations, display simulation results, writing VHDL code, etc.

- the backend analogue simulator,

  The analogue simulator is a command line program which is run by the GUI in order to simulate the schematic which you previously setup. It takes a netlist, checks it for errors, performs the required simulation actions and finally produces a dataset.

- a simple text editor,

  The text editor is used to display netlists and simulation logging informations, also to edit files included by certain components (e.g. SPICE netlists, or Touchstone files).

- a filter synthesis application,

  The program can be used to design various types of filters.

- a transmission line calculator,

  The transmission line calculator can be used to design and analyze different types of transmission lines (e.g. microstrips, coaxial cables).

- a component library,

  The component library manager holds models for real life devices (e.g. transistors, diodes, bridges, opamps). It can be extended by the user.

- an attenuator synthesis application,

  The program can be used to design various types of passive attenuators.

- a command line conversion program

  The conversion tool is used by the GUI to import and export datasets, netlists and schematics from and to other CAD/EDA software. The supported file formats as well as usage information can be found on the manpage of **qucsconv**.

Additionally the GUI steers other EDA tools. For digital simulations (via VHDL) the program FreeHDL (see `http://www.freehdl.seul.org`) is used. And for circuit optimizations ASCO (see `http://asco.sourceforge.net`) is configured and run.

Setting up schematics

The following sections will enable the user to setup some simple schematics. For this we first create a new project named "WorkBook". Either press the **New** button above the projects folder or use the menu entry **Project** → **New Project** and enter the new project name.

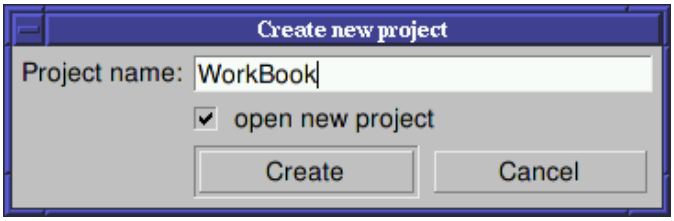

Figure 3: New project dialog

Confirm the dialog by pressing the "Create" button. When done, the project is opened and Qucs switches to the **Content** tab.

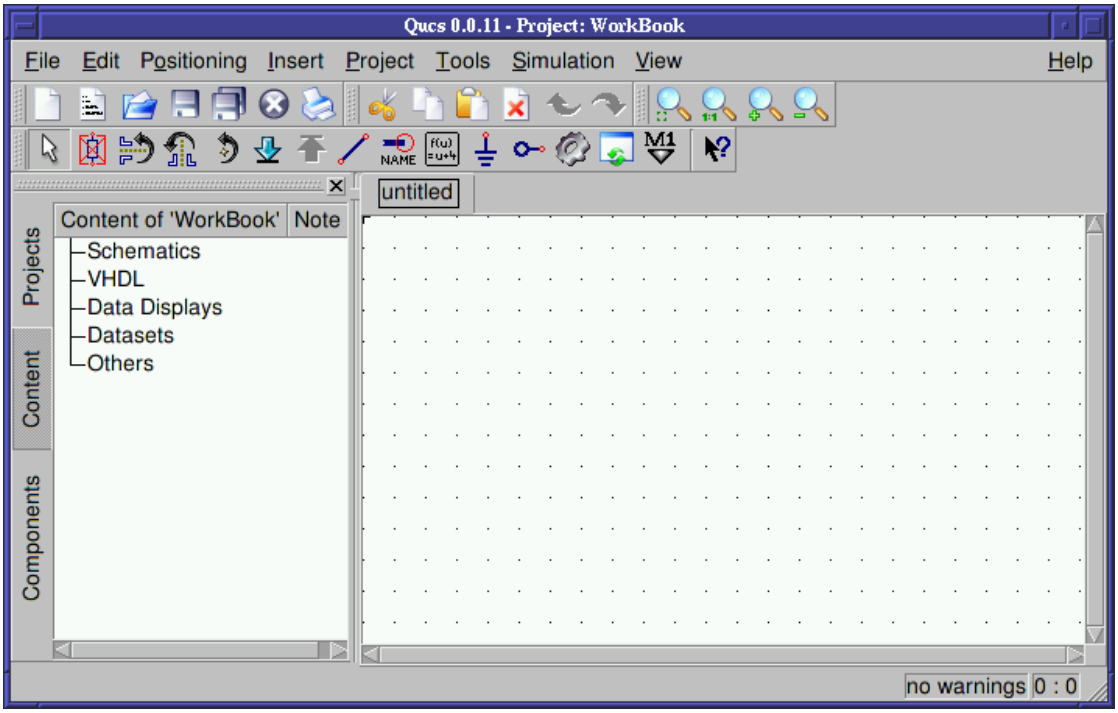

Figure 4: New empty project has been created

In the **Content** tab you will find all data related to the project. It contains your schematics, the VHDL files, data display pages, datasets as well as any other data (e.g. datasheets). On the right hand side an "untitled" and empty schematic window is displayed.

Now you can start to edit the schematic. The available components can be found in the **Components** tab.

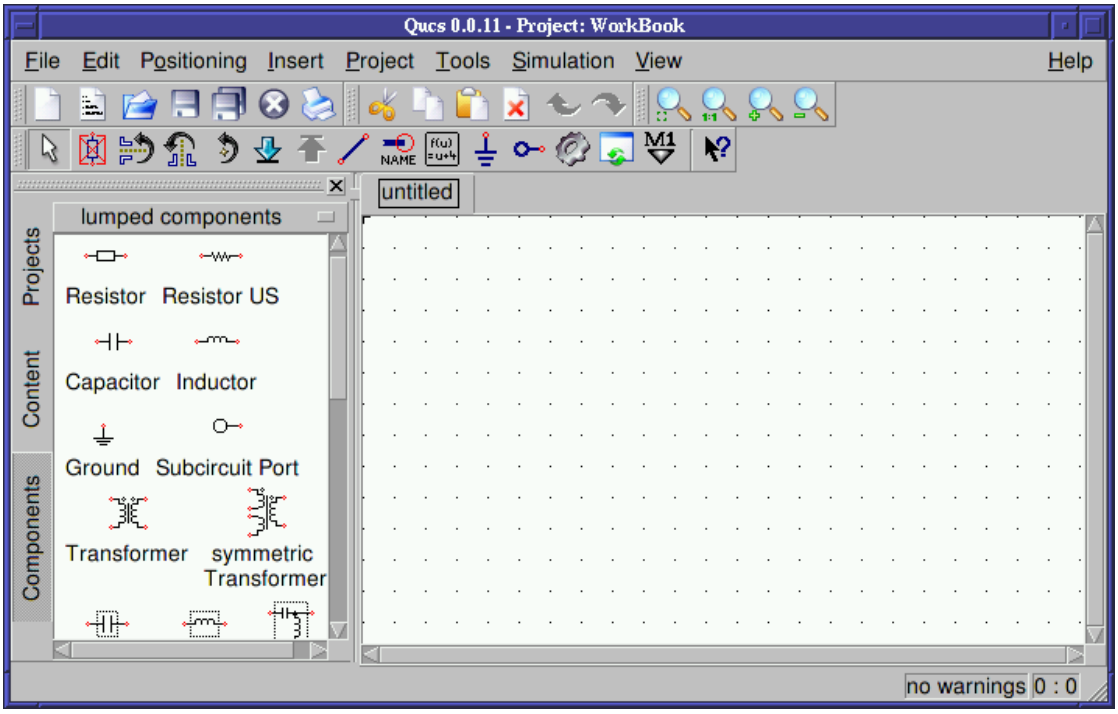

Figure 5: Components tab

In fig. 5 is shown when clicking the **Components** tab. There are lumped components (e.g. resistors, capacitors), sources (e.g. DC and AC sources), transmission lines (e.g. microstrip, coaxial cable, twisted pair), nonlinear components (e.g. ideal opamp, transistors), digital components (e.g. flip-flops), file components (e.g. Touchstone files, SPICE files), simulations (e.g. AC or DC analysis), diagrams (e.g. cartesian or polar plot) and paintings (e.g. texts, arrows, circles).

Each of the components can placed on the schematic by clicking it once, then move the mouse cursor onto the schematic and click again to put it on its final position. During the mouse move you can right click in order to rotate the component into its final position. The user can also drag-and-drop the components.

DC simulation - A voltage divider

The DC analysis is a steady state analysis. It computes the node voltage as well as branch currents of the complete circuit. The given circuit in fig. 6 is going to divide the voltage of a DC voltage source according to the resistor ratio.

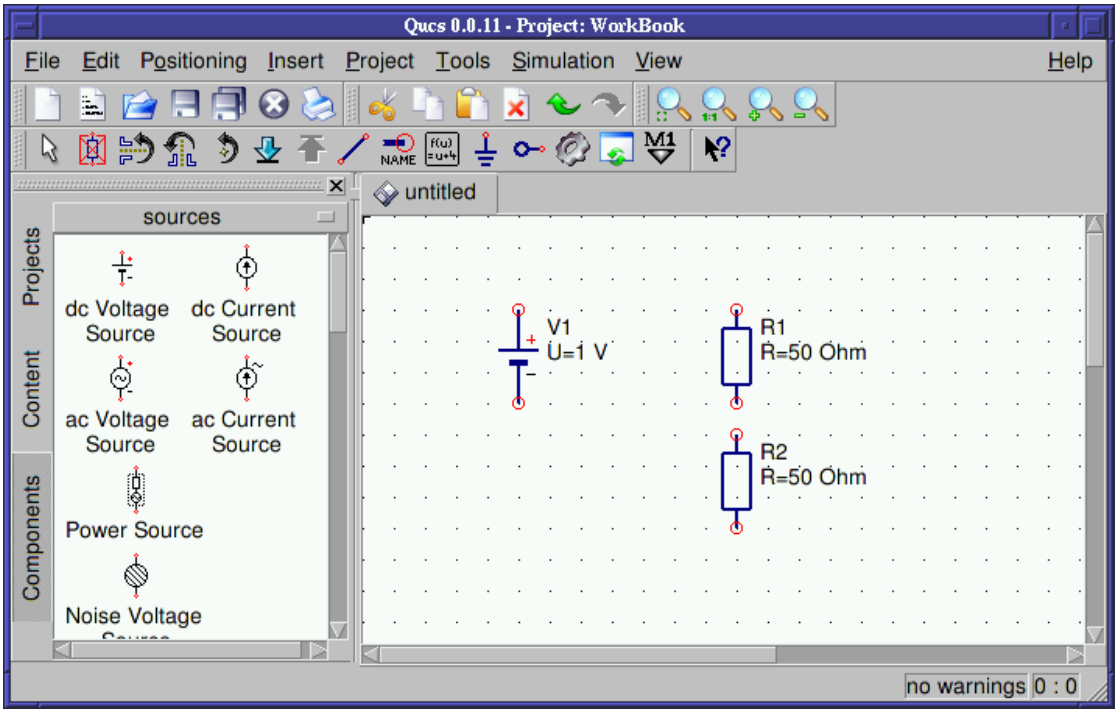

Figure 6: Components of the voltage divider place in the schematic area

Wiring components

Now you need to connect the components appropriately. This is done using the wiring tool. You enable the wiring mode either by clicking the wire icon or by pressing the Ctrl + E shortcut. Left clicking on the components' ports (small red circles) starts a wire, clicking on a second port finishes the wire. In order to change the orientation of the wire right click it. You can leave the wiring mode by the pressing Esc key.

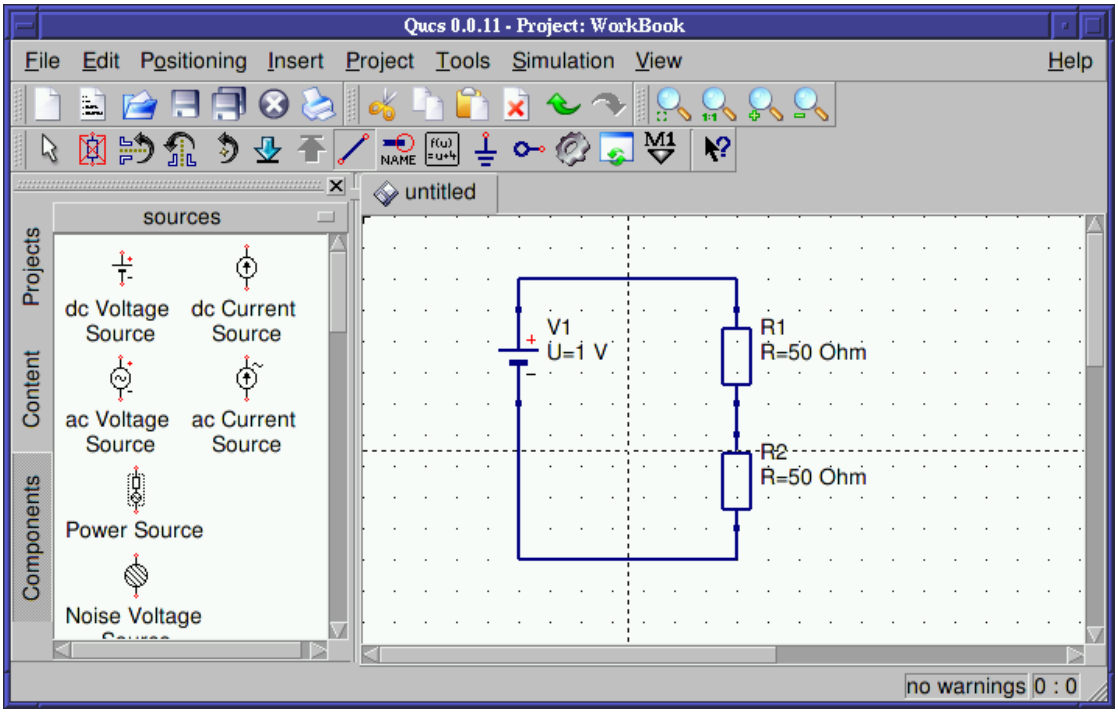

Figure 7: Components of the voltage divider appropriately wired

For any analogue simulation (including the DC simulation) there is a reference potential required (for the nodal analysis). The ground symbol can be found in the **Components** tab in the **lumped components** category. The user can also choose the ground symbol icon or simply press the Ctrl + G shortcut. In the given circuit in fig. 8 the ground symbol is placed at the negative terminal of the DC voltage source.

Placing simulation blocks

The type of simulation which is performed must also be placed on the schematic. You choose the "DC simulation" block which can be found in the **Components** tab in the **simulations** category.

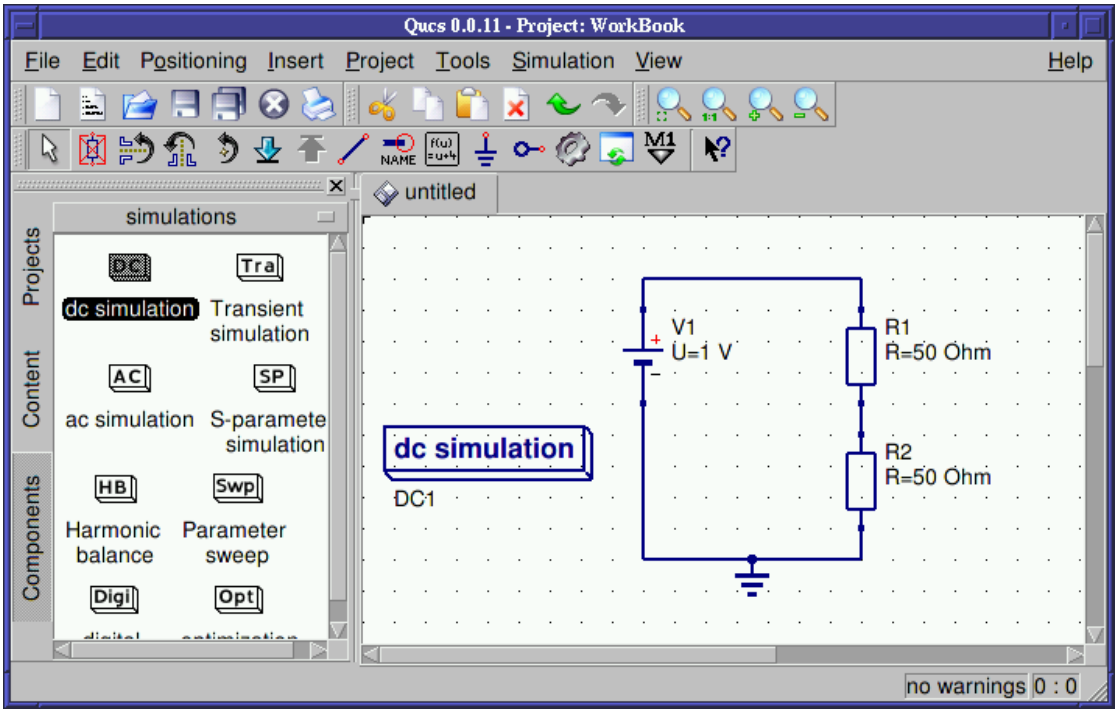

Figure 8: Ground symbol as well as DC simulation in place

Labelling wires

If you want the voltage between the two resistors (the divided voltage) be output in the dataset after simulation the user need to label the wire. This is done by double clicking the wire and given an appropriate name. Wire labelling can also be issued using the icon in the toolbar, by pressing the Ctrl + L shortcut or by choosing the **Insert** → **Wire Label** menu entry.

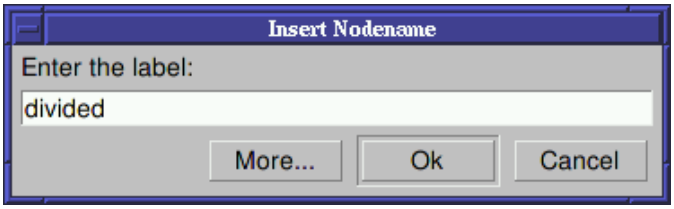

Figure 9: Node label dialog

The dialog is ended by pressing the Enter key of pressing the "Ok" button.

Now the complete schematic for the voltage divider is ready and can be saved. This can by achieved by choosing the **File** → **Save** menu entry, clicking the single disk icon or by pressing the Ctrl + S shortcut.

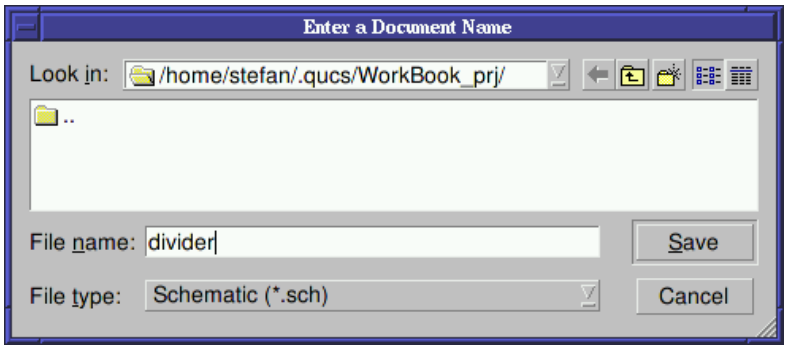

Figure 10: File save dialog

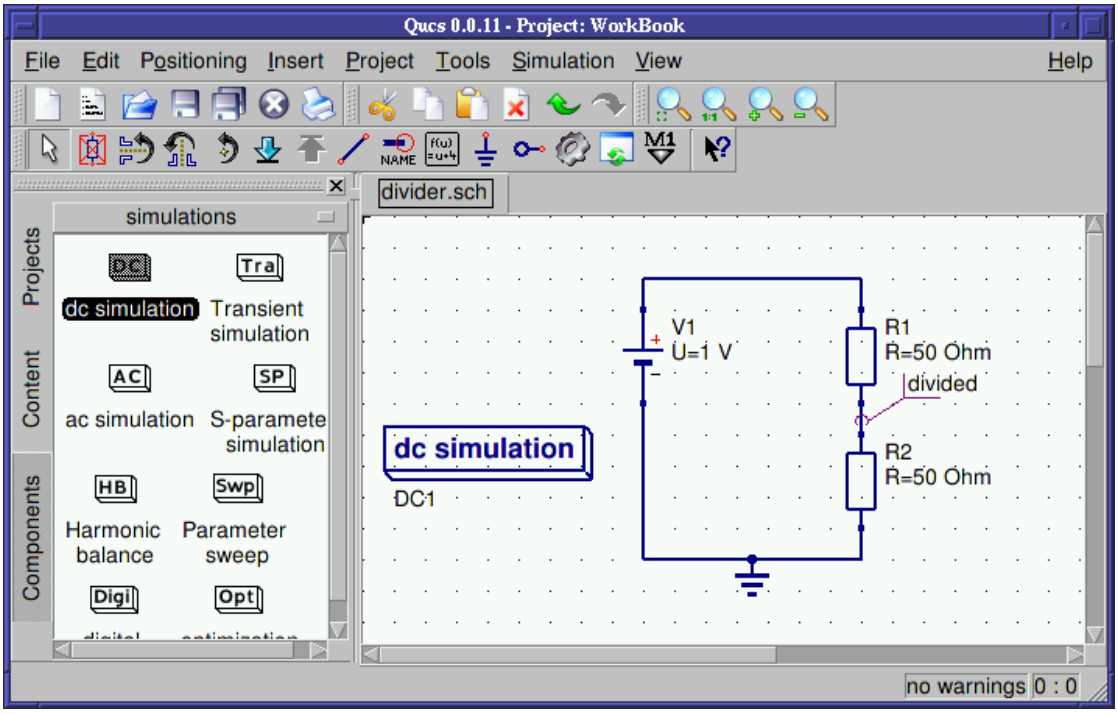

Figure 11: Final voltage divider schematic